



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	94
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk51dn512cmd10



7.1 Obtaining package dimensions.....	71	8.2 K51 pinouts.....	78
8 Pinout.....	72	9 Revision history.....	80
8.1 K51 signal multiplexing and pin assignments.....	72		

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK51 and MK51.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K51
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory

Table continues on the next page...

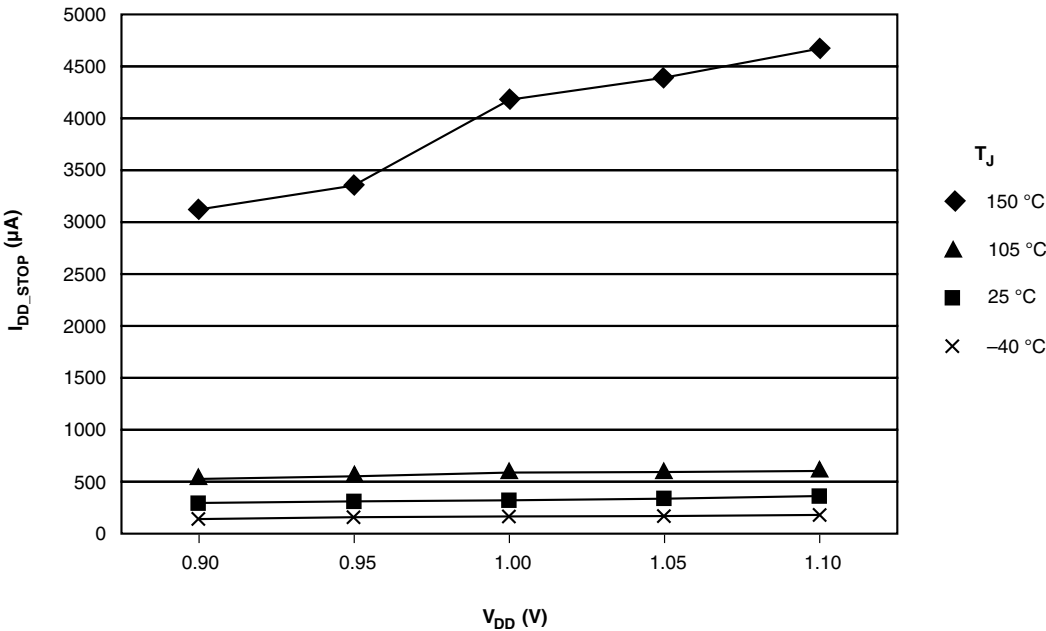
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	$^{\circ}C$
V_{DD}	3.3 V supply voltage	3.3	V

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H} V _{LVW2H} V _{LVW3H} V _{LVW4H}	Low-voltage warning thresholds — high range - Level 1 falling (LVWV=00) - Level 2 falling (LVWV=01) - Level 3 falling (LVWV=10) - Level 4 falling (LVWV=11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L} V _{LVW2L} V _{LVW3L} V _{LVW4L}	Low-voltage warning thresholds — low range - Level 1 falling (LVWV=00) - Level 2 falling (LVWV=01) - Level 3 falling (LVWV=10) - Level 4 falling (LVWV=11)	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	1
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

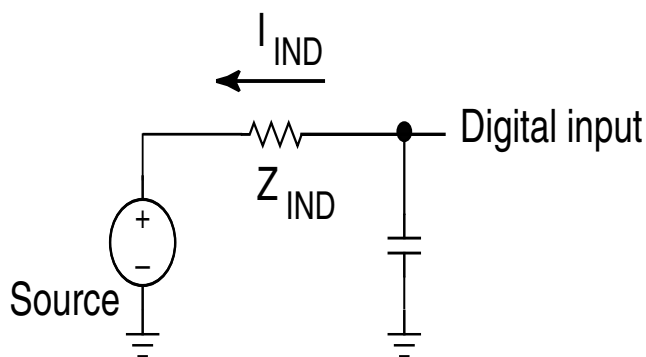
Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5\text{ V}$	—	1	50	μA	4, 5
Z_{IND}	Input impedance examples, digital pins • $V_{DD} = 3.6\text{ V}$ • $V_{DD} = 3.0\text{ V}$ • $V_{DD} = 2.5\text{ V}$ • $V_{DD} = 1.7\text{ V}$	— — — —	— — — —	48 55 57 85	$\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$	4, 7
R_{PU}	Internal pullup resistors	20	35	50	$\text{k}\Omega$	8
R_{PD}	Internal pulldown resistors	20	35	50	$\text{k}\Omega$	9

1. Typical values characterized at 25°C and $V_{DD} = 3.6\text{ V}$ unless otherwise noted.
2. Open drain outputs must be pulled to V_{DD} .
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
5. Internal pull-up/pull-down resistors disabled.
6. Characterized, not tested in production.
7. Examples calculated using V_{IL} relation, V_{DD} , and max I_{IND} : $Z_{IND} = V_{IL} / I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
8. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$
9. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$



5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

General

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 96\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	$1.71 \leq V_{DD} \leq 2.7V$	—	12	ns	
	$2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	
	Slew enabled				
	$1.71 \leq V_{DD} \leq 2.7V$	—	36	ns	
	$2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	85	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	°C/W	1

Table continues on the next page...

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

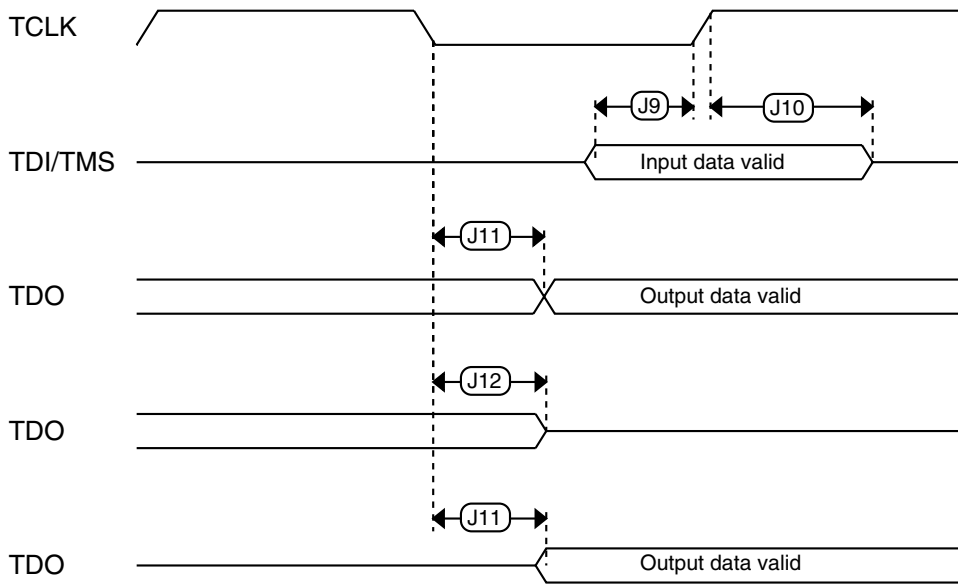


Figure 7. Test Access Port timing

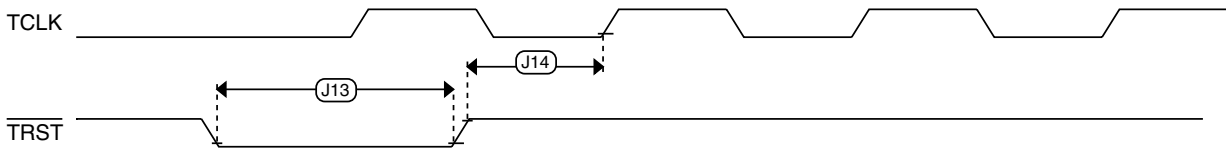


Figure 8. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

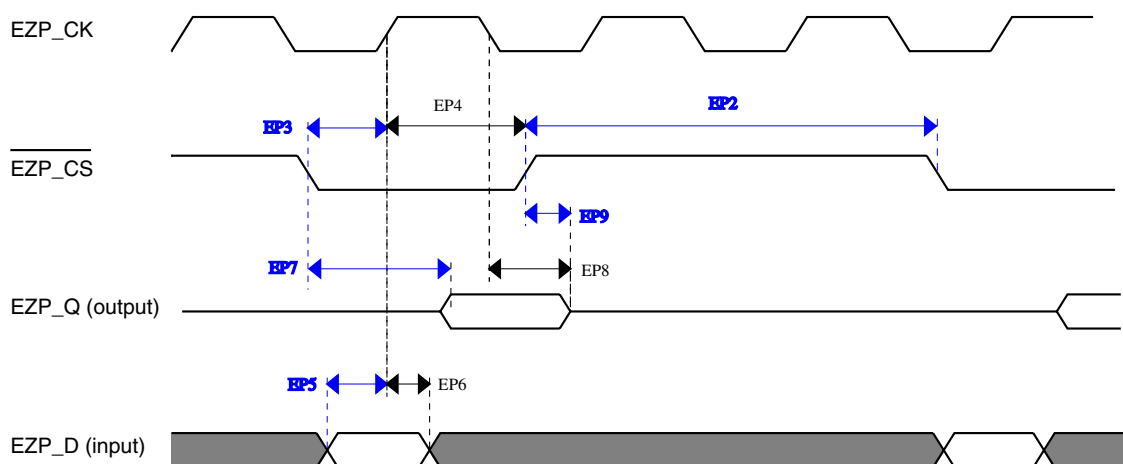
Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk256k}$	Read 1s Block execution time • 256 KB program/data flash	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program/data flash	—	122	985	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time • 512 bytes flash • 1 KB flash • 2 KB flash	—	2.4	—	ms	
$t_{pgmsec1k}$		—	4.7	—	ms	
$t_{pgmsec2k}$		—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	250	2000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

Table continues on the next page...

Table 24. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{\text{SYS}}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns


Figure 9. EzPort Timing Diagram

6.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

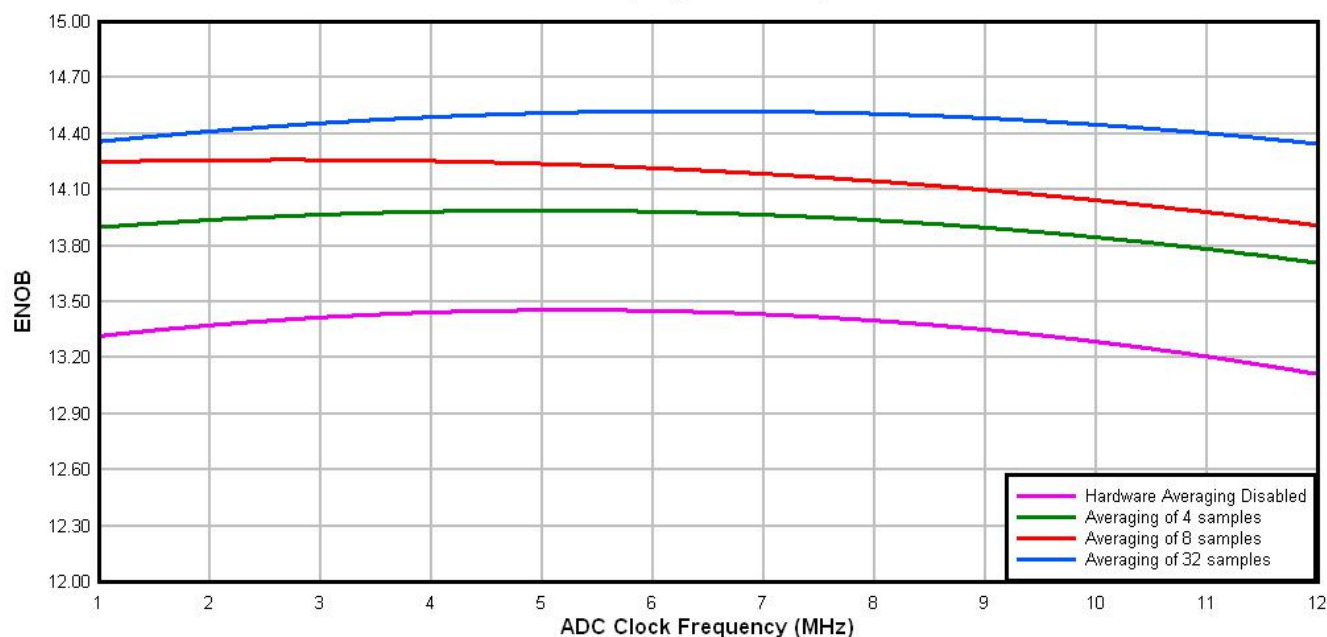
Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{IN} \times R_{AS}$		mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

Typical ADC 16-bit Differential ENOB vs ADC Clock
100Hz, 90% FS Sine Input

Figure 13. Typical ENOB vs. ADC_CLK for 16-bit differential mode

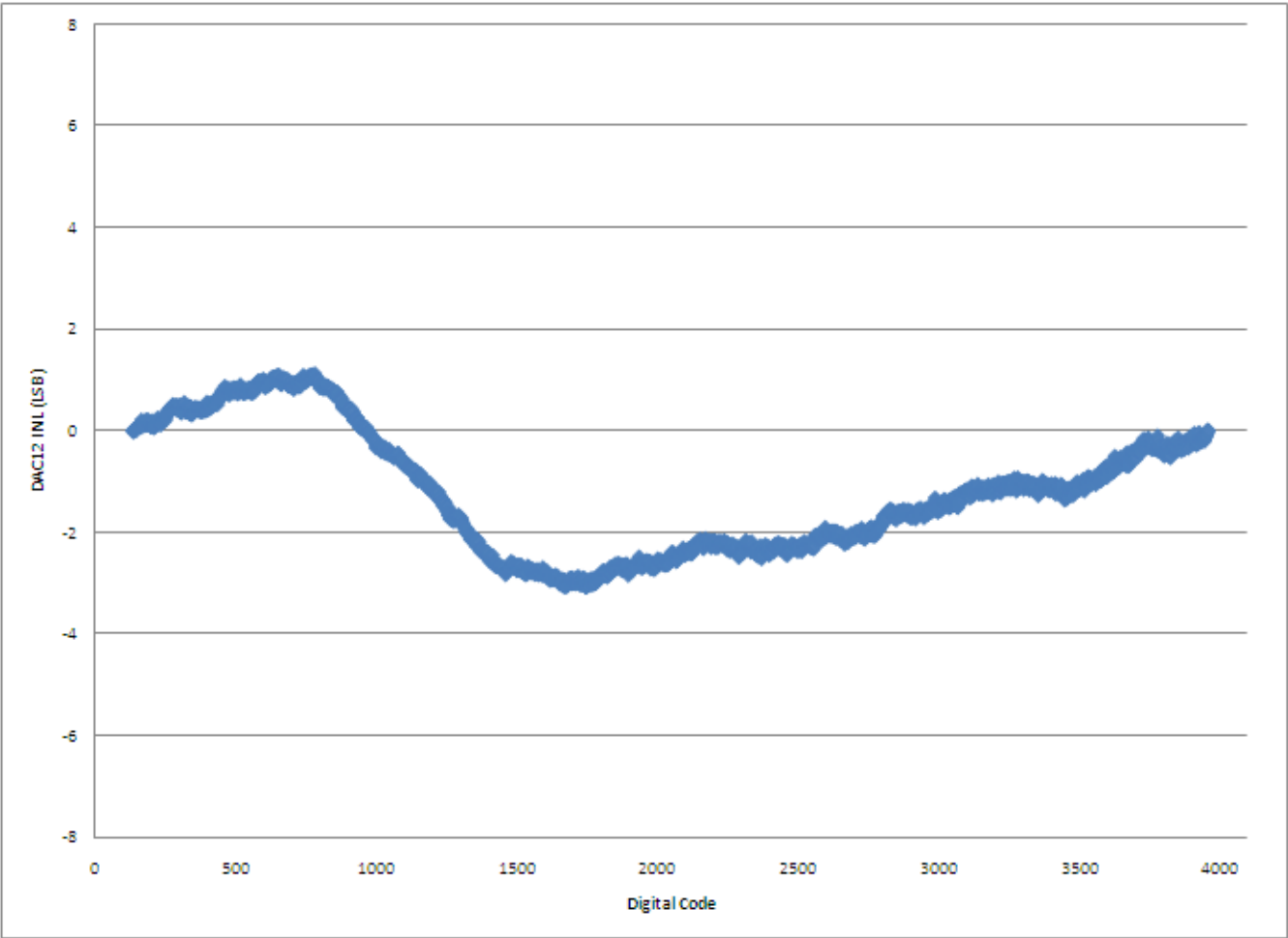


Figure 17. Typical INL error vs. digital code

6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 45. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

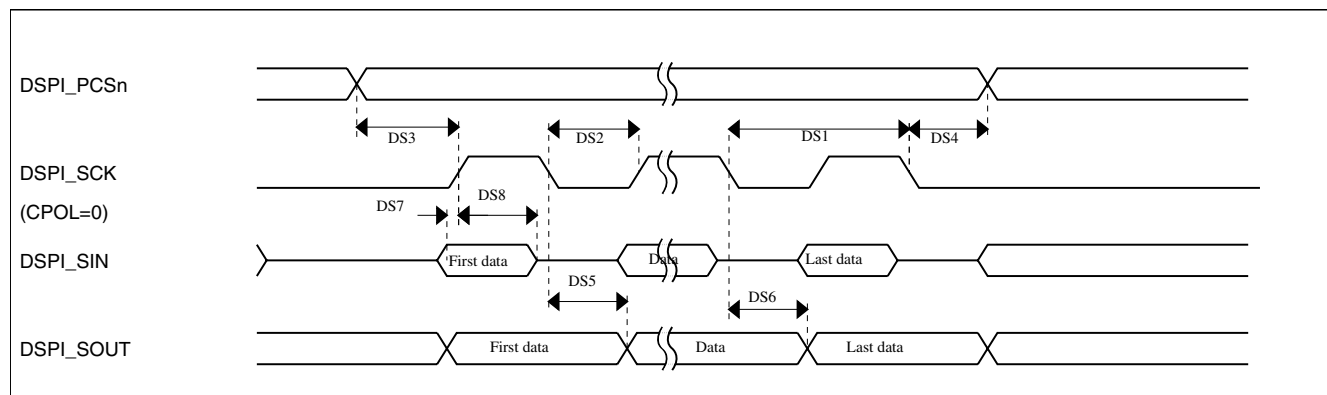


Figure 19. DSPI classic SPI timing — master mode

Table 46. Slave mode DSPI timing (limited voltage range)

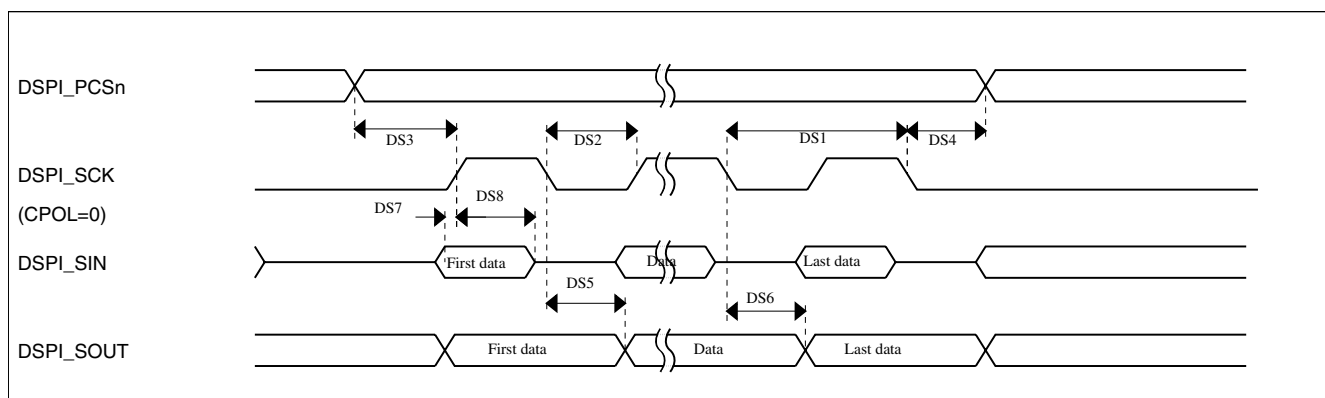
Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns

Table continues on the next page...

Table 47. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].


Figure 21. DSPI classic SPI timing — master mode
Table 48. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

Table 54. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

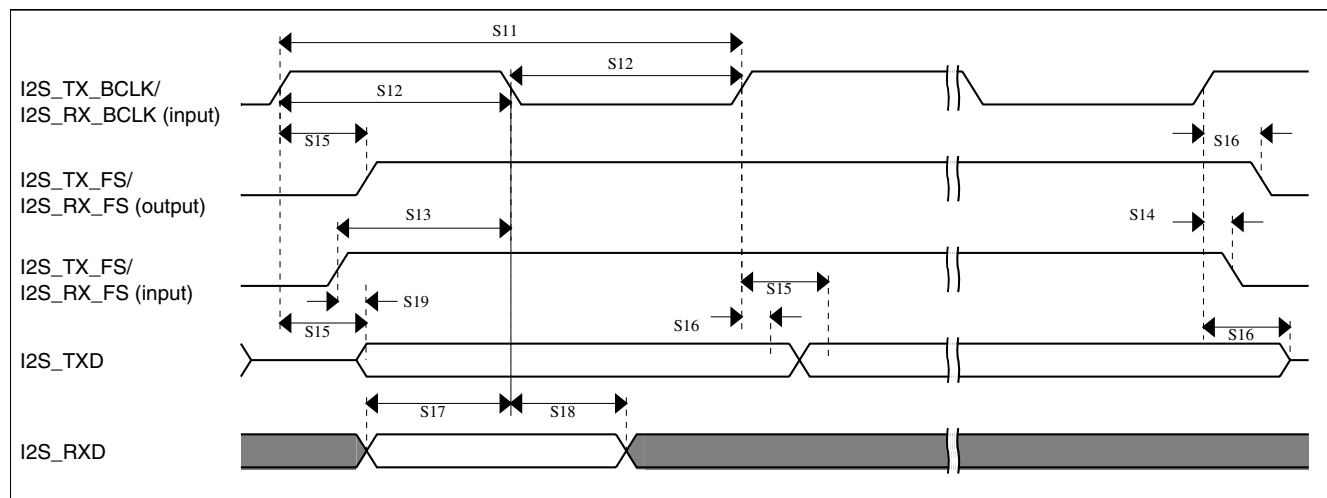


Figure 28. I2S/SAI timing — slave modes

6.8.9.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns

Table continues on the next page...

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

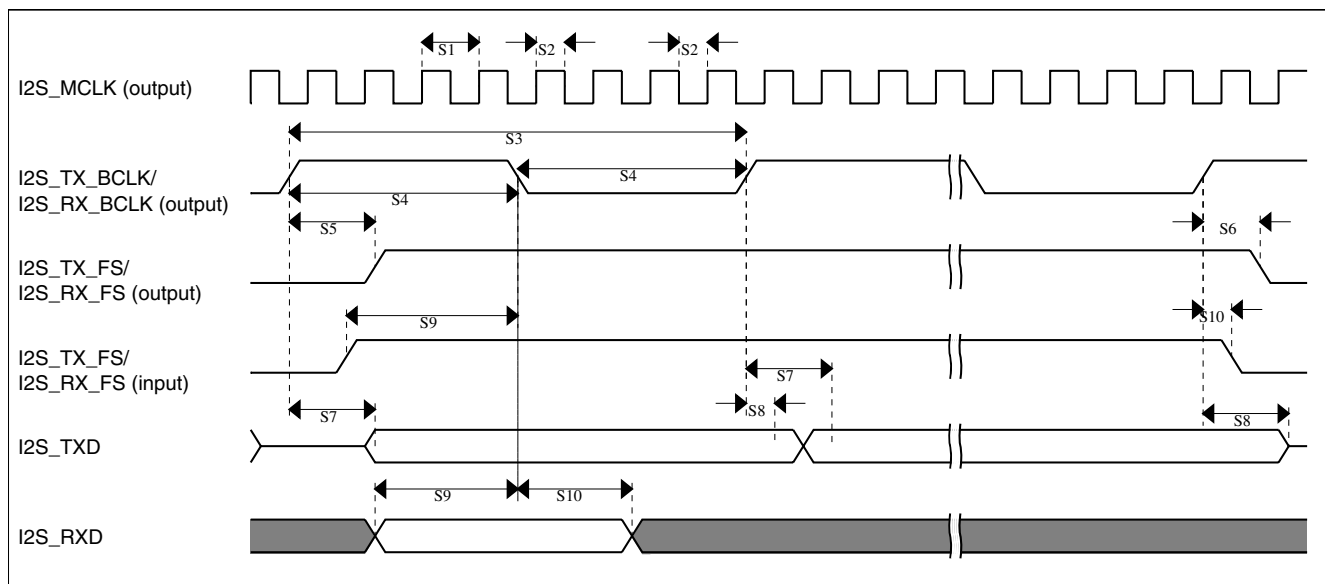


Figure 29. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

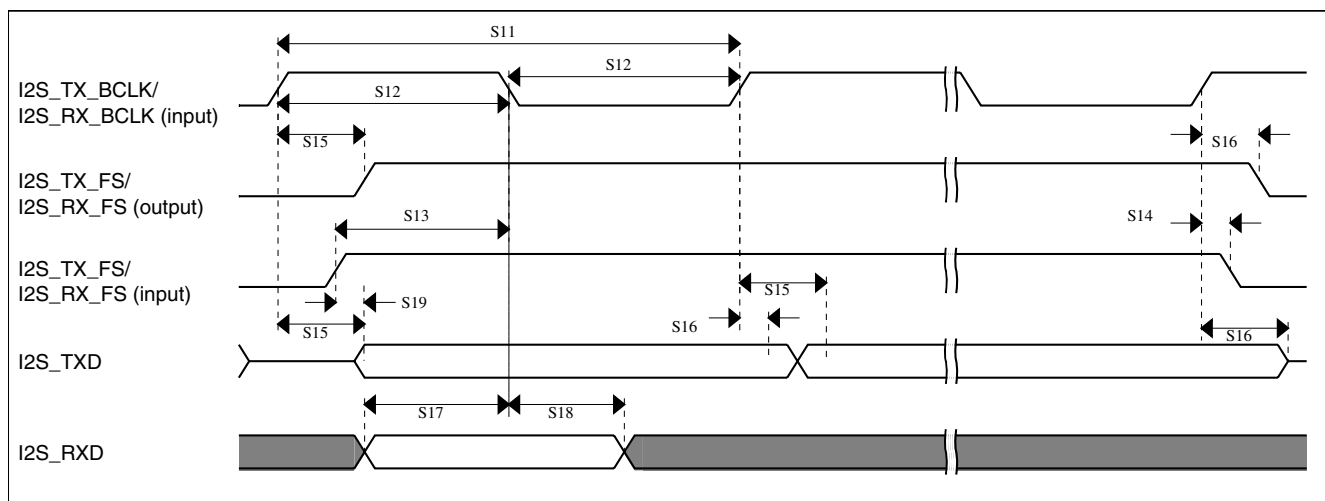


Figure 30. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 57. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f _{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C _{REF}	Internal reference capacitor	—	1	—	pF	
V _{DELTA}	Oscillator delta voltage	—	500	—	mV	2, 5
I _{REF}	Reference oscillator current source base current 2 μA setting (REFCHRG = 0) 32 μA setting (REFCHRG = 15)	—	2	3	μ A	2, 6
I _{ELE}	Electrode oscillator current source base current 2 μA setting (EXTCHRG = 0) 32 μA setting (EXTCHRG = 15)	—	2	3	μ A	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μ s	12
I _{TSI_RUN}	Current added in run mode	—	55	—	μ A	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μ A	13

8 Pinout

8.1 K51 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

For FlexBus applications, use only the CLKOUT signal on the PTA6 pin to ensure proper timing.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1	FB_AD27	I2C1_SDA	RTC_CLKOUT	
2	D2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0	FB_AD26	I2C1_SCL	SPI1_SIN	
3	D1	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK	FB_AD25			
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD	FB_AD24		SPI1_SOUT	
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b			
9	E1	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_ b	I2S0_MCLK	FB_ALE/ FB_CS1_b/ FB_TS_b		USB_SOF_ OUT	
10	F4	PTE7	DISABLED		PTE7		UART3_RTS_ b	I2S0_RXD0	FB_CS0_b			
11	F3	PTE8	DISABLED		PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS	FB_AD4			
12	F2	PTE9	DISABLED		PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_ BCLK	FB_AD3			
13	F1	PTE10	DISABLED		PTE10		UART5_CTS_ b	I2S0_TXD0	FB_AD2			
14	G4	PTE11	DISABLED		PTE11		UART5_RTS_ b	I2S0_TX_FS	FB_AD1			
15	G3	PTE12	DISABLED		PTE12			I2S0_TX_ BCLK	FB_AD0			
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								