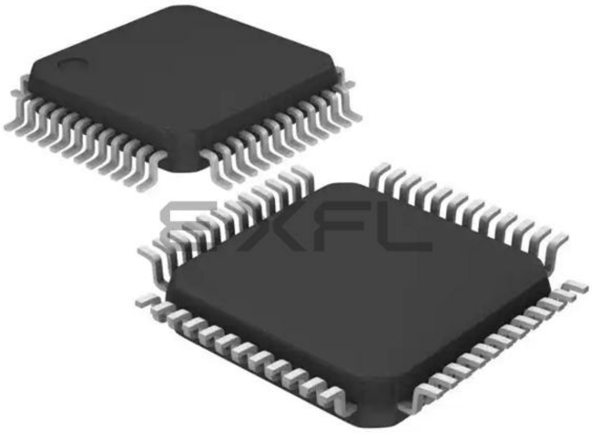
STMicroelectronics - STM8S105C4T6TR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105c4t6tr

Contents

4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

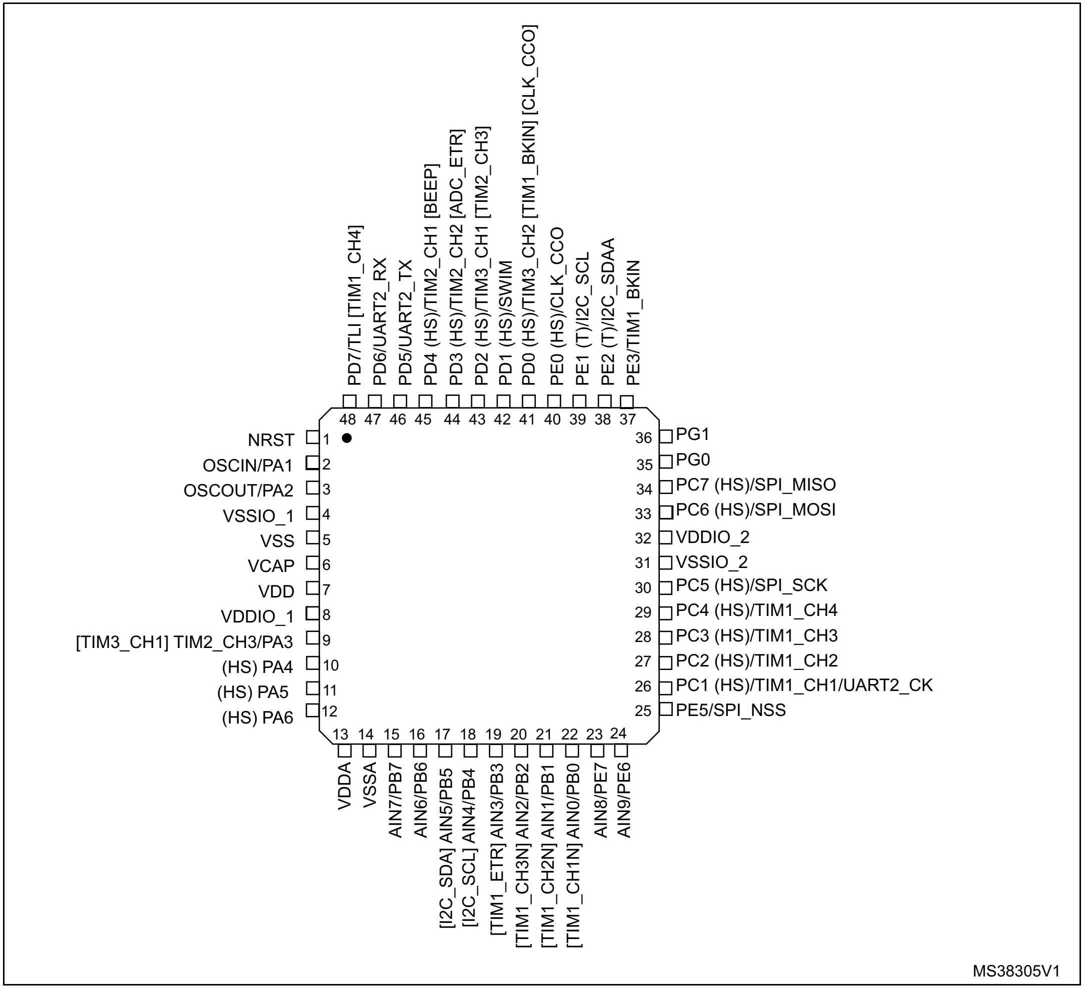
Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

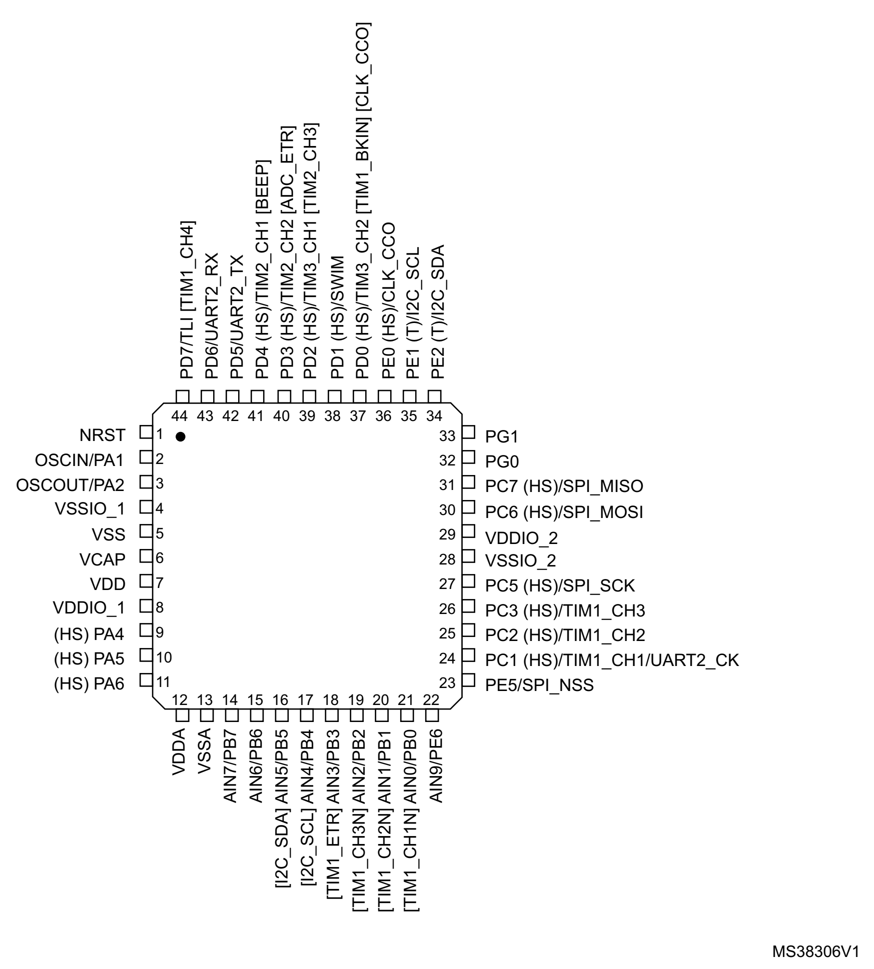
Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART2	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

Figure 3. LQFP48 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4. LQFP44 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	22	-	-	PE6/ AIN9	I/O	X	X	X	-	O1	X	X	Port E6	Analog input 9(3)	-
25	23	17	22	PE5/ SPI_NSS	I/O	X	X	X	-	O1	X	X	Port E5	SPI master/ slave select	-
26	24	18	23	PC1/ TIM1_CH1/ UART2_CK	I/O	X	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1/UART2 synchronous clock	-
27	25	19	24	PC2/ TIM1_CH2	I/O	X	X	X	HS	O3	X	X	Port C2	Timer 1- channel 2	-
28	26	20	25	PC3/ TIM1_CH3	I/O	X	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
29	-	21	26	PC4/ TIM1_CH4	I/O	X	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4	-
30	27	22	27	PC5/ SPI_SCK	I/O	X		X	HS	O3	X	X	Port C5	SPI clock	-
31	28	-	-	VSSIO_2	S	-	-	-	-	-	-	-	I/O ground		-
32	29	-	-	VDDIO_2	S	-	-	-	-	-	-	-	I/O power supply		-
33	30	23	28	PC6/ SPI_MOSI	I/O	X	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-
34	31	24	29	PC7/ SPI_ MISO	I/O	X	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
35	32	-	-	PG0	I/O	X	X	-	-	O1	X	X	Port G0	-	-
36	33	-	-	PG1	I/O	X	X	-	-	O1	X	X	Port G1	-	-
37	-	-	-	PE3/ TIM1_BKIN	I/O	X	X	X	-	O1	X	X	Port E3	Timer 1 - break input	-
38	34	-	-	PE2/ I 2C_ SDA	I/O	X	-	X	-	O1	T (4)	-	Port E2	I 2C data	-
39	35	-	-	PE1/ I2C_ SCL	I/O	X	-	X	-	O1	T (4)	-	Port E1	I 2C clock	-

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Typical current consumption

For typical current consumption measurements, VDD, VDDIO and VDDA are connected together in the configuration shown in the following figure.

Figure 8. Supply current measurement conditions

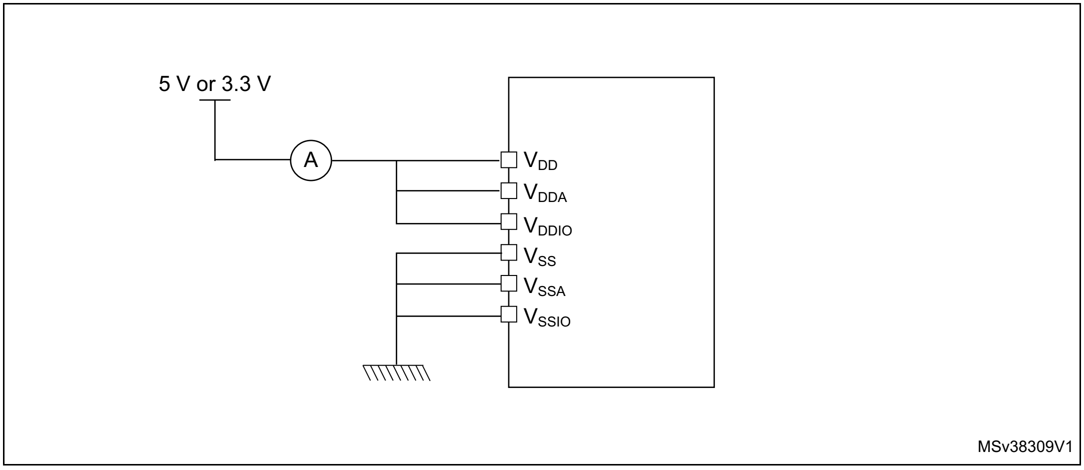


Table 39. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	1.0	V
	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.5(1)	
V_{OH}	Output high level with 2 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0(1)	

1. Data based on characterization results, not tested in production

Table 40. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.9	V
	Output low level with 4 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.1(1)	
		I_{IO}= 20 mA, V_{DD} = 5 V	-	1.6(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	3.8	-	
	Output high level with 4 pins sourced	I_{IO}= 10 mA, V_{DD} = 3.3 V	1.9(1)	-	
		I_{IO}= 20 mA, V_{DD} = 5 V	2.9(1)	-	

1. Data based on characterization results, not tested in production.

10.3.7 Typical output level curves

The following figures show the typical output level curves measured with the output on a single pin.

Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

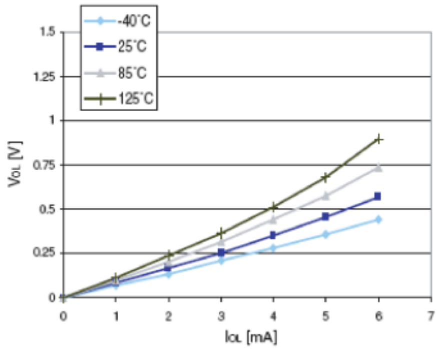


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

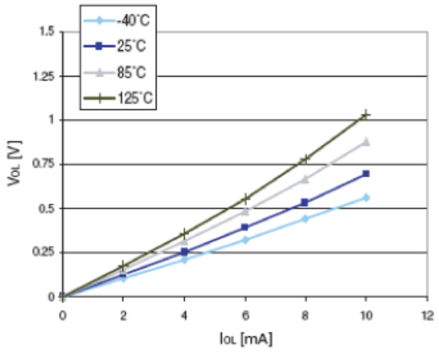
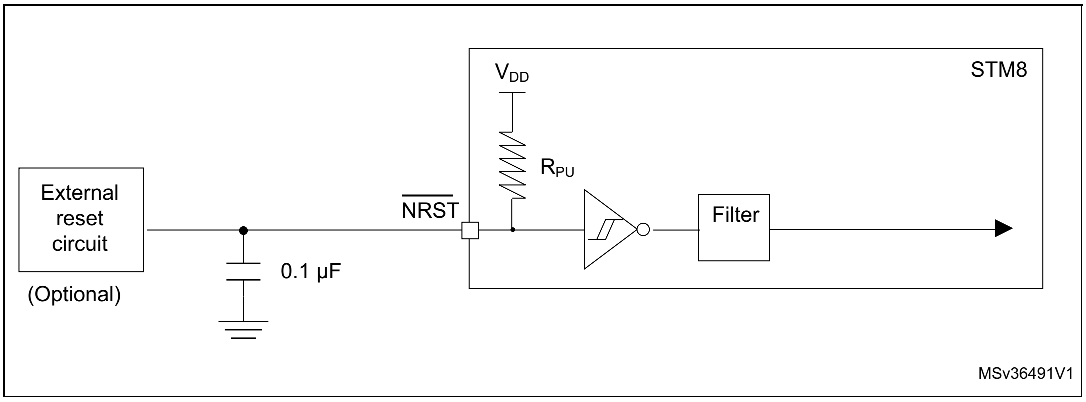


Figure 40. Recommended reset pin protection



10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions[(1)]	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	6	

10.3.11 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 44. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD}= 2.95 to 5.5 V	1	-	4	MHz
		V_{DD}= 4.5 to 5.5 V	1	-	6	
V_{DDA}	Analog supply	-	3.0	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5(1)	
V_{AIN}	Conversion voltage range(2)	-	V_{SSA}	-	V_{DDA}	V
		Devices with external V_{REF+}/V_{REF-}	V_{REF-}	-	V_{REF+}	
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(2)	Minimum sampling time	f_{ADC} = 4 MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
		-	14			$1/f_{ADC}$

1. Data guaranteed by design, not tested in production.

2. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 45. ADC accuracy with R_{AIN}< 10 kΩ, V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
$\lvert E_T \rvert$	Total unadjusted error[2]	f_{ADC} = 2 MHz	1.0	2.5	LSB
		f_{ADC} = 4 MHz	1.4	3.0	
		f_{ADC} = 6 MHz	1.6	3.5	
$\lvert E_O \rvert$	Offset error[2]	f_{ADC} = 2 MHz	0.6	2.0	
		f_{ADC} = 4 MHz	1.1	2.5	
		f_{ADC} = 6 MHz	1.2	2.5	
$\lvert E_G \rvert$	Gain error[2]	f_{ADC} = 2 MHz	0.2	2.0	
		f_{ADC} = 4 MHz	0.6	2.5	
		f_{ADC} = 6 MHz	0.8	2.5	
$\lvert E_D \rvert$	Differential linearity error[2]	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.8	1.5	
$\lvert E_L \rvert$	Integral linearity error[2]	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	
		f_{ADC} = 6 MHz	0.6	1.5	

1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
$\lvert E_T \rvert$	Total unadjusted error[2]	f_{ADC} = 2 MHz	1.1	2.0	LSB
		f_{ADC} = 4 MHz	1.6	2.5	
$\lvert E_O \rvert$	Offset error[2]	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	1.3	2.0	
$\lvert E_G \rvert$	Gain error[2]	f_{ADC} = 2 MHz	0.2	1.5	
		f_{ADC} = 4 MHz	0.5	2.0	
$\lvert E_D \rvert$	Differential linearity error[2]	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.0	
$\lvert E_L \rvert$	Integral linearity error[2]	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	

1. Data based on characterization results, not tested in production.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 5$ V, $T_A = 25$ °C, $f_{MASTER} = 16$ MHz (HSI clock), Conforms to IEC 1000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 5$ V, $T_A = 25$ °C, $f_{MASTER} = 16$ MHz (HSI clock), Conforms to IEC 1000-4-4	4/A(1)

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 18: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 56. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7x7 mm		°C/W
	Thermal resistance junction-ambient LQFP44 - 10x10 mm		
	Thermal resistance junction-ambient LQFP32 - 7x7 mm		
	Thermal resistance junction-ambient UFQFPN32 - 5x5 mm		
	Thermal resistance junction-ambient SDIP32 - 400 ml		

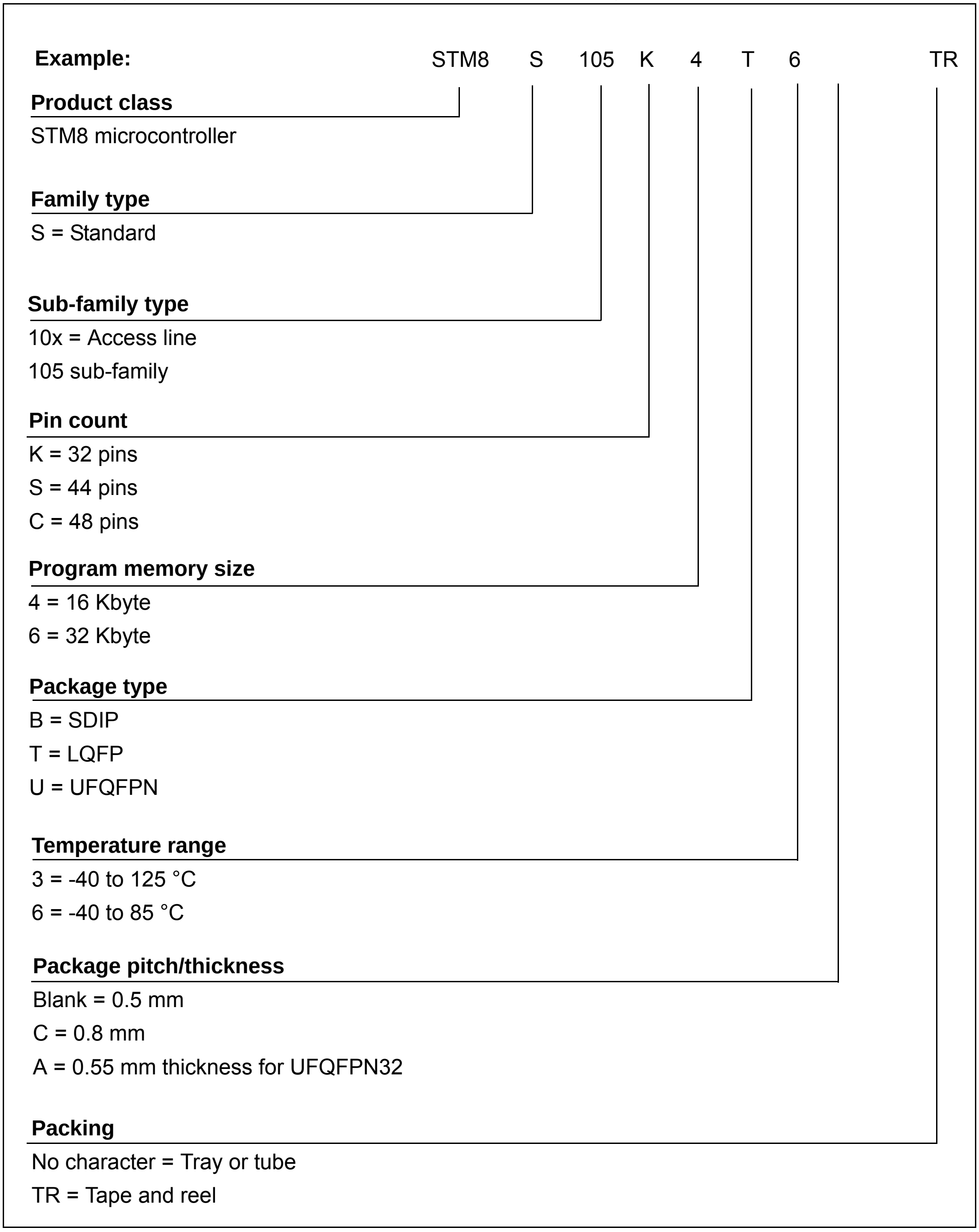
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

13 Ordering information

Figure 61. STM8S105x4/6 access line ordering information scheme(1)



Example: STM8 S 105 K 4 T 6 TR

Product class
STM8 microcontroller

Family type
S = Standard

Sub-family type
10x = Access line
105 sub-family

Pin count
K = 32 pins
S = 44 pins
C = 48 pins

Program memory size
4 = 16 Kbyte
6 = 32 Kbyte

Package type
B = SDIP
T = LQFP
U = UFQFPN

Temperature range
3 = -40 to 125 °C
6 = -40 to 85 °C

Package pitch/thickness
Blank = 0.5 mm
C = 0.8 mm
A = 0.55 mm thickness for UFQFPN32

Packing
No character = Tray or tube
TR = Tape and reel

1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set

OTP2 alternate function remapping

AFR0 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D3 alternate function = ADC_ETR
AFR1 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3
AFR2 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = CLK_CCO *Note: if both AFR2 and AFR3 are activated, AFR2 option has priority over AFR3.*
AFR3 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = TIM1_BKIN

AFR4 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D7 alternate function = TIM1_CH4
AFR5 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N.
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port B5 alternate function = I2C_SDA, port B4 alternate function = I2C_SCL
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D4 alternate function = BEEP.

OPT3 watchdog

WWDG_HALT (check only one option)	[ ] 0: No reset generated on halt if WWDG active[[ ] 1: Reset generated on halt if WWDG active
WWDG_HW (check only one option)	[ ] 0: WWDG activated by software [ ] 1: WWDG activated by hardware
IWDG_HW (check only one option)	[ ] 0: IWDG activated by software [ ] 1: IWDG activated by hardware
LSI_EN (check only one option)	[ ] 0: LSI clock is not available as CPU clock source [ ] 1: LSI clock is available as CPU clock source
HSITRIM (check only one option)	[ ] 0: 3-bit trimming supported in CLK_HSITRIMR register [ ] 1: 4-bit trimming supported in CLK_HSITRIMR register

OPT4 watchdog

PRSC (check only one option)	[ ] for 16 MHz to 128 kHz prescaler [ ] for 8 MHz to 128 kHz prescaler [ ] for 4 MHz to 128 kHz prescaler
CKAWUSEL (check only one option)	[ ] LSI clock source selected for AWU [ ] HSE clock with prescaler selected as clock source for AWU
EXTCLK (check only one option)	[ ] External crystal connected to OSCIN/OSCOUT [ ] External signal on OSCIN

15 Revision history

Table 57. Document revision history

Date	Revision	Changes
05-Jun-2018	1	Initial release.
23-Jun-2018	2	Corrected the number of high sink outputs to 9 in I/Os in *Features*. Updated part numbers in *STM8S105xx access line features*.
12-Aug-2008	3	Updated the part numbers in *STM8S105xx access line features*. USART renamed UART1, LINUART renamed UART2. Added *Table: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices.*
17-Sep-2008	4	Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM. Updated STM8S103 pinout section Added low and medium density Flash memory categories. Added Note 1 in *Section: Current characteristics.* Updated *Section: Option bytes.*
05-Feb-2009	5	Updated STM8S103 pinout. Updated number of High Sink I/Os in the pinout section. TSSOP20 pinout modified (PD4 moved to pin 1 etc.) Added WFQFN20 package Updated *Section: Option bytes.* Added *Section: Memory and register map.*
27-Feb-2009	6	Removed STM8S103x products (separate STM8S103 datasheet created). Updated *Section: Electrical characteristics.*