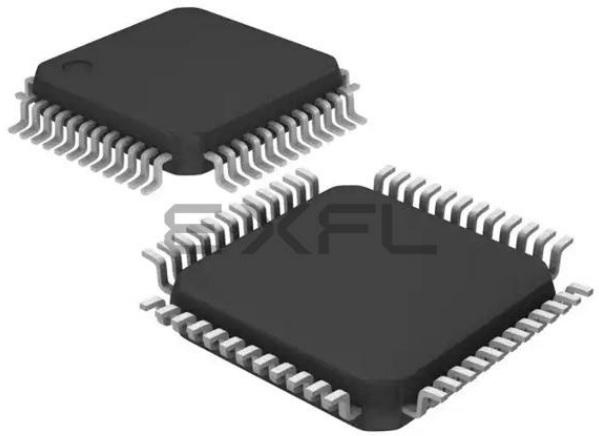

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105c6t3

List of figures

4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

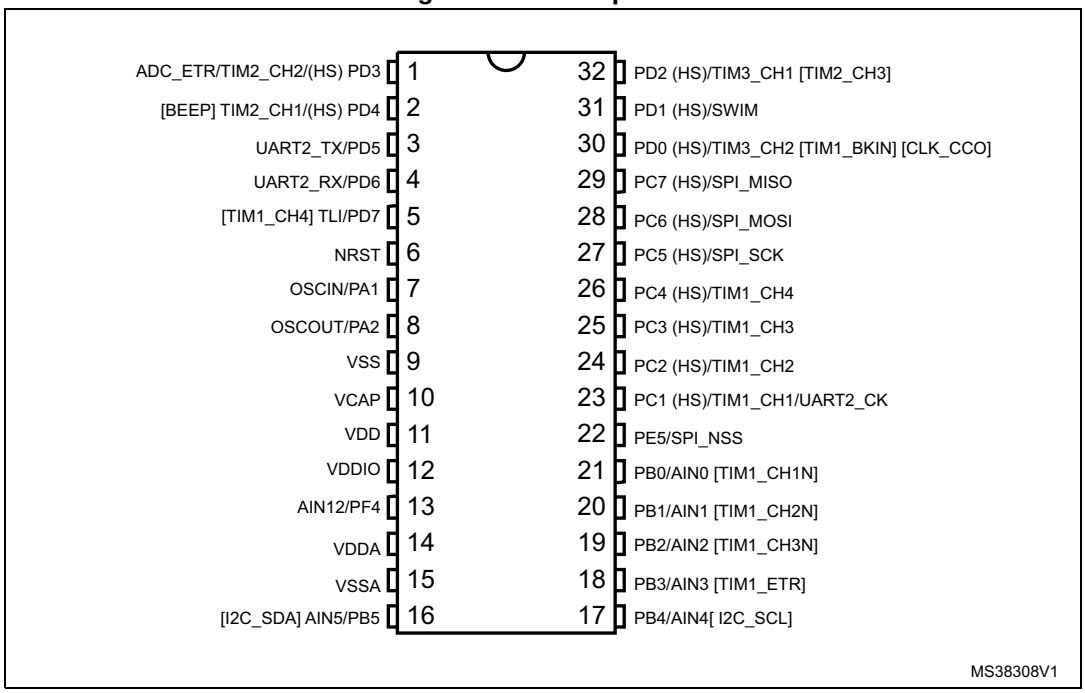
Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART2	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

5 Pinout and pin description

Table 4. Legend/abbreviations for pin description tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Figure 6. SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	6	NRST	I/O	-	**X**	-	-		-	-	Reset		-
2	2	2	7	PA1/ OSC IN	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
3	3	3	8	PA2/ OSC OUT	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
4	4	-	-	VSSIO_1	S	-	-	-	-	-	-	-	I/O ground		-
5	5	4	9	VSS	S	-	-	-	-	-	-	-	Digital ground		-
6	6	5	10	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
7	7	6	11	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	7	12	VDDIO_1	S	-	-	-	-	-	-	-	I/O power supply		-
9	-	-	-	PA3/ TIM2_CH3 [TIM3_CH1]	I/O	**X**	X	X	-	O1	X	X	Port A3	Timer 2 - channel 3	TIM3_ CH1 [AFR1]
10	9	-	-	PA4	I/O	**X**	X	X	HS	O3	X	X	Port A4	-	-
11	10	-	-	PA5	I/O	**X**	X	X	HS	O3	X	X	Port A5	-	-
12	11	-	-	PA6	I/O	**X**	X	X	HS	O3	X	X	Port A6	-	-
-	-	8	13	PF4/ AIN12(1)	I/O	**X**	X	-	-	O1	X	X	Port F4	Analog input 12(2)	-
13	12	9	14	VDDA	S	-	-	-	-	-	-	-	Analog power supply		-
14	13	10	15	VSSA	S	-	-	-	-	-	-	-	Analog ground		-
15	14	-	-	PB7/ AIN7	I/O	**X**	X	X	-	O1	X	X	Port B7	Analog input 7	-
16	15	-	-	PB6/ AIN6	I/O	**X**	X	X	-	O1	X	X	Port B6	Analog input 6	-
17	16	11	16	PB5/ AIN5 [I2C_ SDA]	I/O	**X**	X	X	-	O1	X	X	Port B5	Analog input 5	I 2C_SDA [AFR6]
18	17	12	17	PB4/ AIN4 [I2C_SCL]	I/O	**X**	X	X	-	O1	X	X	Port B4	Analog input 4	I2C_SCL [AFR6]
19	18	13	18	PB3/ AIN3 [TIM1_ETR]	I/O	**X**	X	X	-	O1	X	X	Port B3	Analog input 3	TIM1_ET R [AFR5]
20	19	14	19	PB2/ AIN2 [TIM1_CH3N]	I/O	**X**	X	X	-	O1	X	X	Port B2	Analog input 2	TIM1_CH 3N [AFR5]
21	20	15	20	PB1/ AIN1 [TIM1_CH2N]	I/O	**X**	X	X	-	O1	X	X	Port B1	Analog input 1	TIM1_CH 2N [AFR5]
22	21	16	21	PB0/ AIN0 [TIM1_CH1N]	I/O	**X**	X	X	-	O1	X	X	Port B0	Analog input 0	TIM1_CH 1N [AFR5]
23	-	-	-	PE7/ AIN8	I/O	**X**	X	X	-	O1	X	X	Port E7	Analog input 8	-

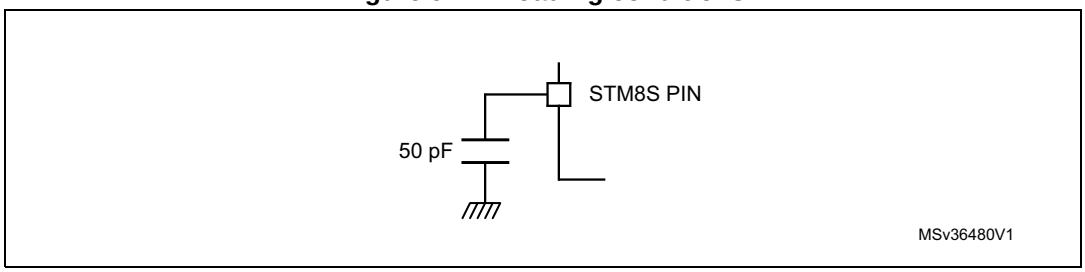
Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

10.1.5 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

Figure 9. Pin loading conditions



10.1.6 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage

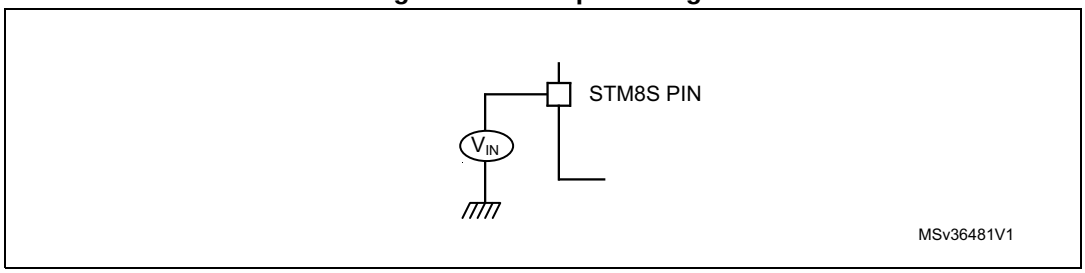


Table 19. Operating conditions at power-up/power-down (continued)

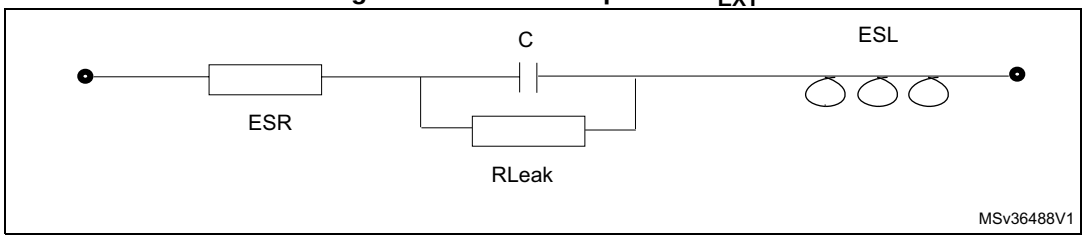
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.65	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 18*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 10: Pin input voltage*.

Total current consumption in run mode

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.2	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	7.7	-	mA
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc. (16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 39. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	1.0	V
	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.5(1)	
V_{OH}	Output high level with 2 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0(1)	

1. Data based on characterization results, not tested in production

Table 40. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.9	V
	Output low level with 4 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.1(1)	
		I_{IO}= 20 mA, V_{DD} = 5 V	-	1.6(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	3.8	-	
	Output high level with 4 pins sourced	I_{IO}= 10 mA, V_{DD} = 3.3 V	1.9(1)	-	
		I_{IO}= 20 mA, V_{DD} = 5 V	2.9(1)	-	

1. Data based on characterization results, not tested in production.

10.3.7 Typical output level curves

The following figures show the typical output level curves measured with the output on a single pin.

Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

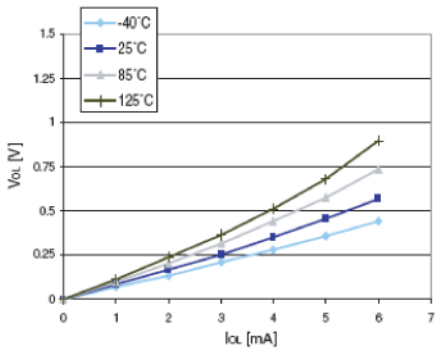


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

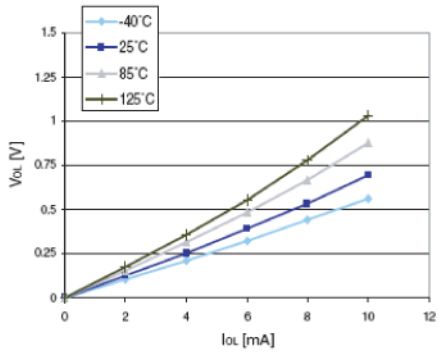
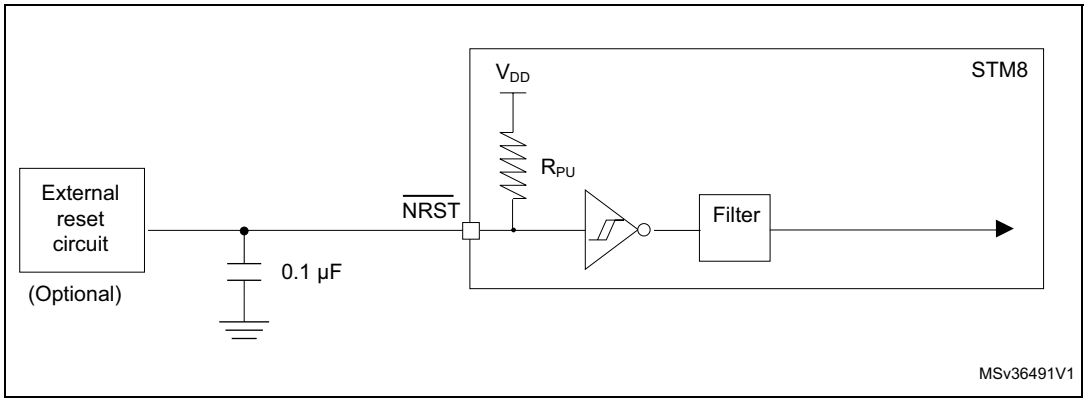


Figure 40. Recommended reset pin protection



10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	6	

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

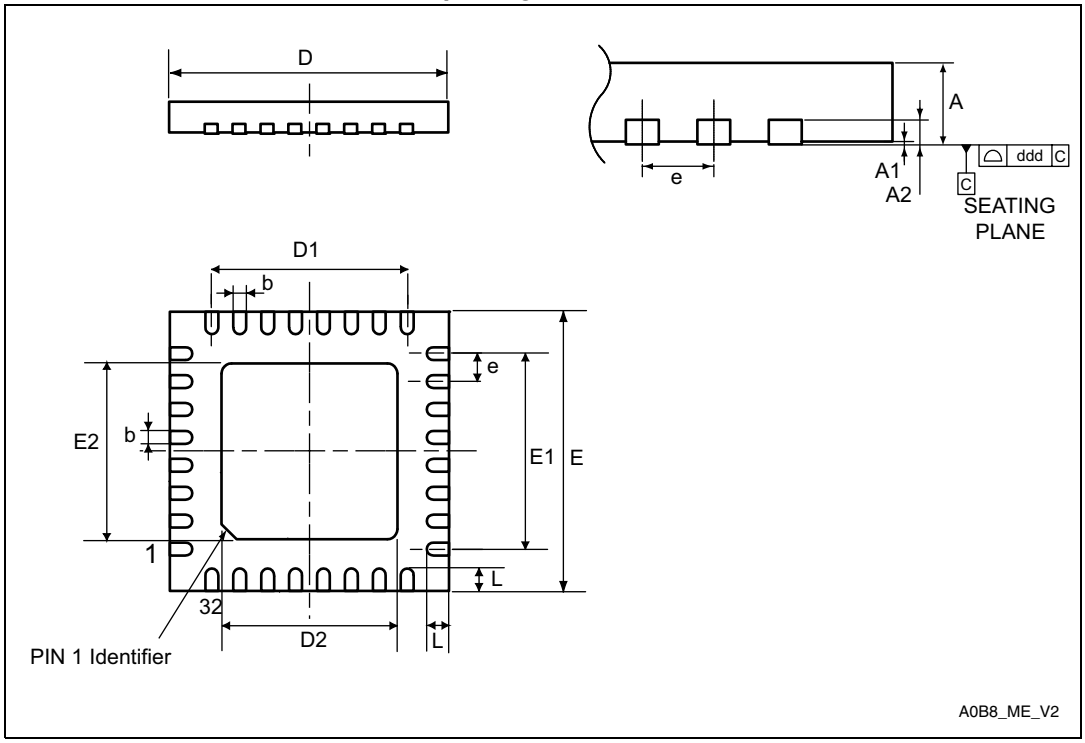
Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	
		$T_A = 125$ °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11.4 UFQFPN32 package information

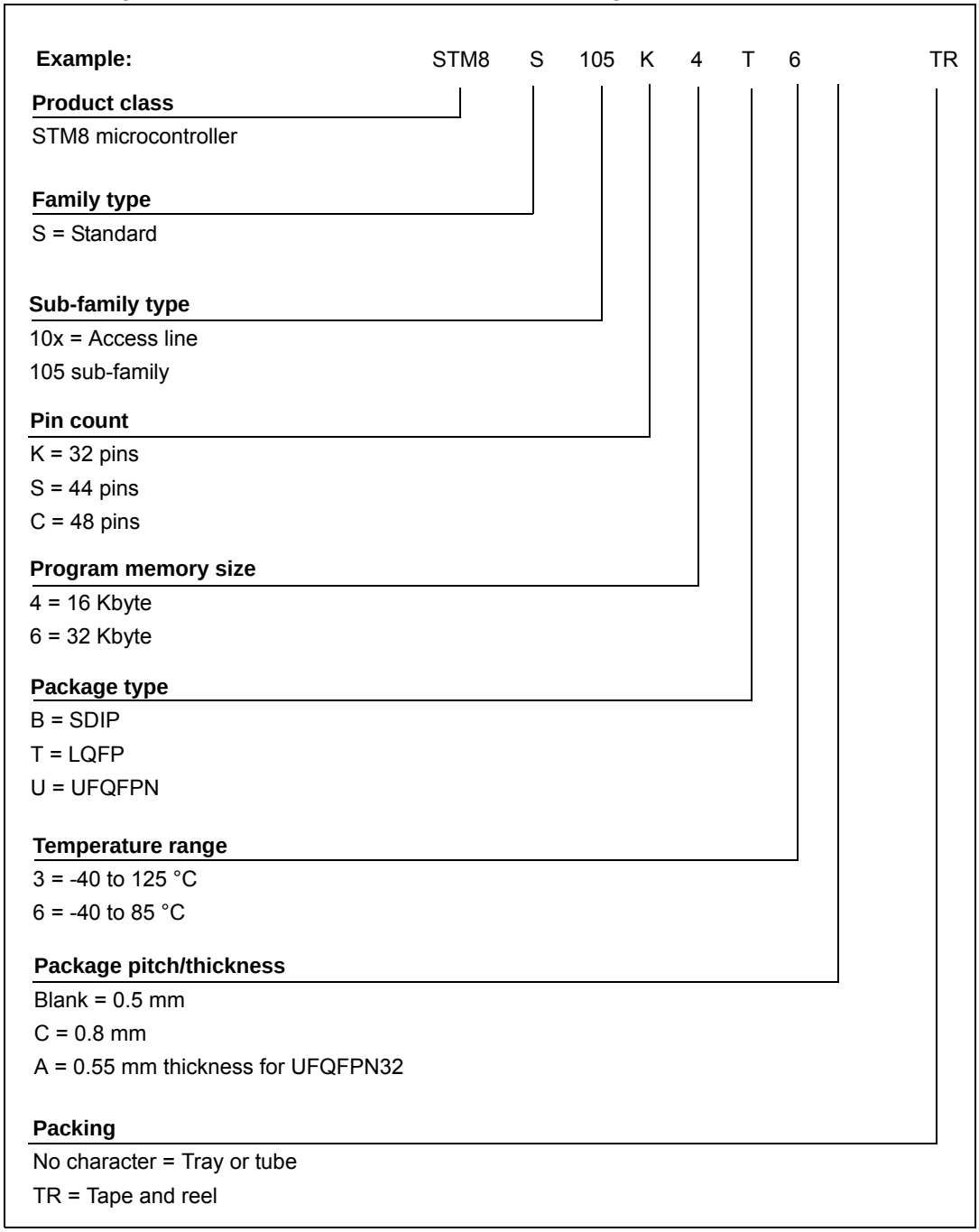
Figure 56. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

13 Ordering information

Figure 61. STM8S105x4/6 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

OTP7 is reserved

OTPBL bootloader option byte (check only one option)

Refer to the UM0560 (STM8L/S bootloader manual) for more details.

[ ] Disable (00h)

[ ] Enable (55h)

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

15 Revision history

Table 57. Document revision history

Date	Revision	Changes
05-Jun-2018	1	Initial release.
23-Jun-2018	2	Corrected the number of high sink outputs to 9 in I/Os in *Features*. Updated part numbers in *STM8S105xx access line features*.
12-Aug-2008	3	Updated the part numbers in *STM8S105xx access line features*. USART renamed UART1, LINUART renamed UART2. Added *Table: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices.*
17-Sep-2008	4	Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM. Updated STM8S103 pinout section Added low and medium density Flash memory categories. Added Note 1 in *Section: Current characteristics.* Updated *Section: Option bytes.*
05-Feb-2009	5	Updated STM8S103 pinout. Updated number of High Sink I/Os in the pinout section. TSSOP20 pinout modified (PD4 moved to pin 1 etc.) Added WFQFN20 package Updated *Section: Option bytes.* Added *Section: Memory and register map.*
27-Feb-2009	6	Removed STM8S103x products (separate STM8S103 datasheet created). Updated *Section: Electrical characteristics.*

Table 57. Document revision history (continued)

Date	Revision	Changes
21-Apr-2010	9	Added UFQFPN32 package silhouette to the title page. In Features: added unique ID. *Section: Clock controller:* updated bit positions for TIM2 and TIM3. *Section: Beeper:* added information about availability of the beeper output port through option bit AFR7. *Section: Analog-to-digital converter (ADC1)*: added a note concerning additional AIN12 analog input. *Section: STM8S105 pinouts and pin description*: added UFQFPN32 package details; updated default alternate function of PB2/AIN2[TIM1_CH3N] pin in the "Pin description for STM8S105 microcontrollers" table. *Section: Option bytes:* added description of STM8L bootloader option bytes to the option byte description table. Added *Section: Unique ID* *Section: Operating conditions*: added introductory text; removed low power dissipation condition for TA, replaced "CEXT" by "VCAP", and added ESR and ESL data in table "general operating conditions". *Section: Total current consumption in halt mode*: replaced max value of IDD(H) at 85 °C from 20 µA to 25 µA for the condition "Flash in powerdown mode, HSI clock after wakeup in the table "total current consumption in halt mode at VDD = 5 V. *Section: Low power mode wakeup times*: added first condition (0 to 16 MHz) for the $t_{WU(WFI)}$ parameter in the table "wakeup times". *Section: Internal clock sources and timing characteristics*: In the *table: HSI oscillator characteristics*, replaced min and max values of ACCHSI factory calibrated parameter and removed footnote 4 concerning further characterization of results. *Section: Functional EMS (electromagnetic susceptibility)*: IEC 1000 replaced with IEC 61000. *Section: Designing hardened software to avoid noise problems:* IEC 1000 replaced with IEC 61000. *Section: Electromagnetic interference (EMI)*: SAE J 1752/3 replaced with IEC61967-2. *Section: Thermal characteristics:* Replaced the thermal resistance junction ambient temperature of LQFP32 7X7 mm from 59 °C to 60 °C in the thermal characteristics table. Added *Section: 32-lead UFQFPN package mechanical data.* Added *Section STM8S105 FASTROM microcontroller option list.*