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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105c6t3tr

6.2.3 CPU/SWIM/debug module/interrupt controller registers 42

7 Interrupt vector mapping 44

8 Option byte 46

8.1 Alternate function remapping bits 49

9 Unique ID 50

10 Electrical characteristics 51

10.1 Parameter conditions 51

10.1.1 Minimum and maximum values 51

10.1.2 Typical values 51

10.1.3 Typical curves 51

10.1.4 Typical current consumption 51

10.1.5 Loading capacitor 52

10.1.6 Pin input voltage 52

10.2 Absolute maximum ratings 53

10.3 Operating conditions 54

10.3.1 VCAP external capacitor 57

10.3.2 Supply current characteristics 57

10.3.3 External clock sources and timing characteristics 66

10.3.4 Internal clock sources and timing characteristics 69

10.3.5 Memory characteristics 72

10.3.6 I/O port pin characteristics 73

10.3.7 Typical output level curves 75

10.3.8 Reset pin characteristics 78

10.3.9 SPI serial peripheral interface 80

10.3.10 I^2C interface characteristics 84

10.3.11 10-bit ADC characteristics 85

10.3.12 EMC characteristics 88

11 Package information 91

11.1 LQFP48 package information 91

11.2 LQFP44 package information 94

11.3 LQFP32 package information 98

11.4 UFQFPN32 package information 101

4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

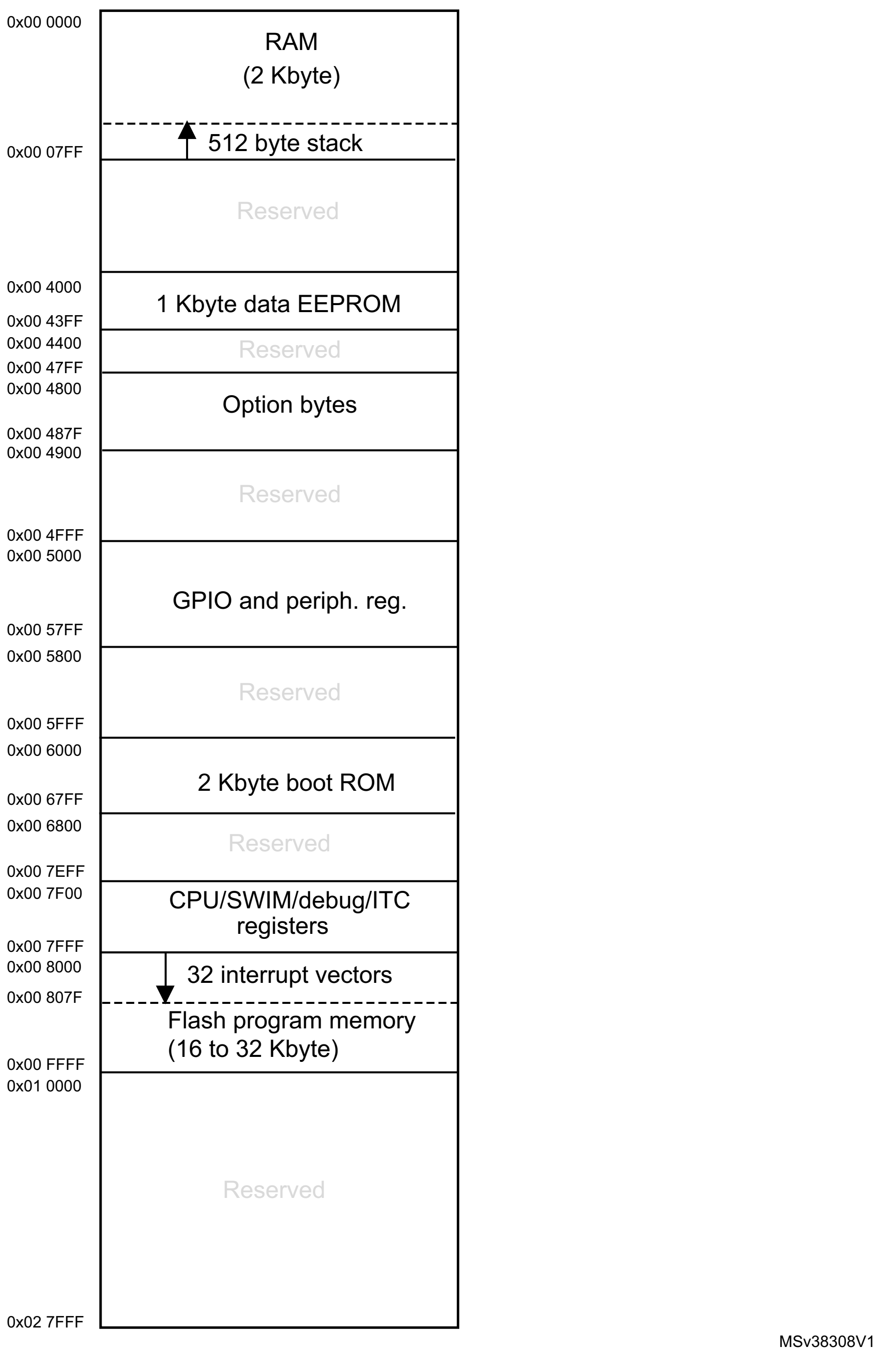
Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

6 Memory and register map

6.1 Memory map

Figure 7. Memory map



The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX[(2)]
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF

Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only.

Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
20	UART2	Tx complete	-	-	0x00 8058
21	UART2	Receive register DATA FULL	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	680	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	320	400	
			Power down mode	HSE crystal osc. (16 MHz)	630	-	-	
			Power down mode	LSI RC osc. (128 kHz)	140	270	350	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	120	220	
			Power down mode	LSI RC osc. (128 kHz)	10	60	150	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 26. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	62	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	6.5	25	80	

1. Data based on characterization results, not tested in production.

Table 27. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	20	80	

1. Data based on characterization results, not tested in production.

Figure 14. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

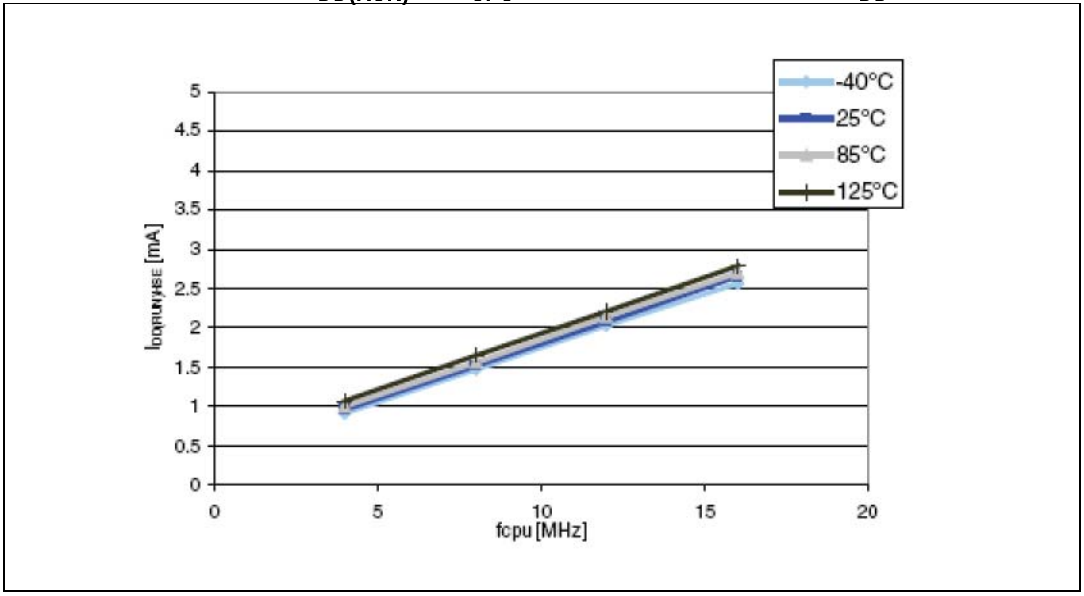
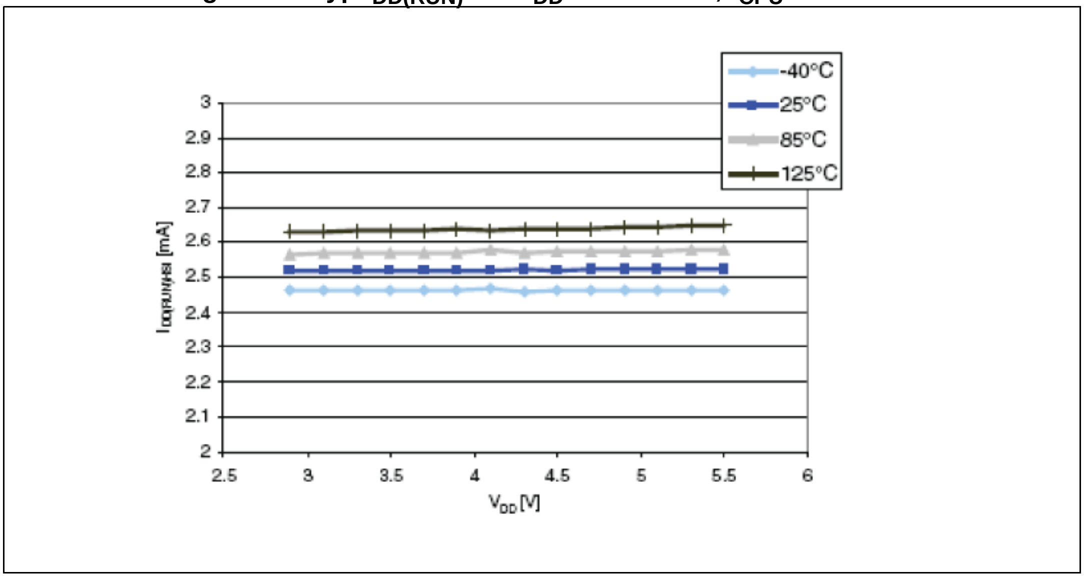


Figure 15. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 31. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Data based on characterization results, not tested in production.

Figure 19. HSE external clock source

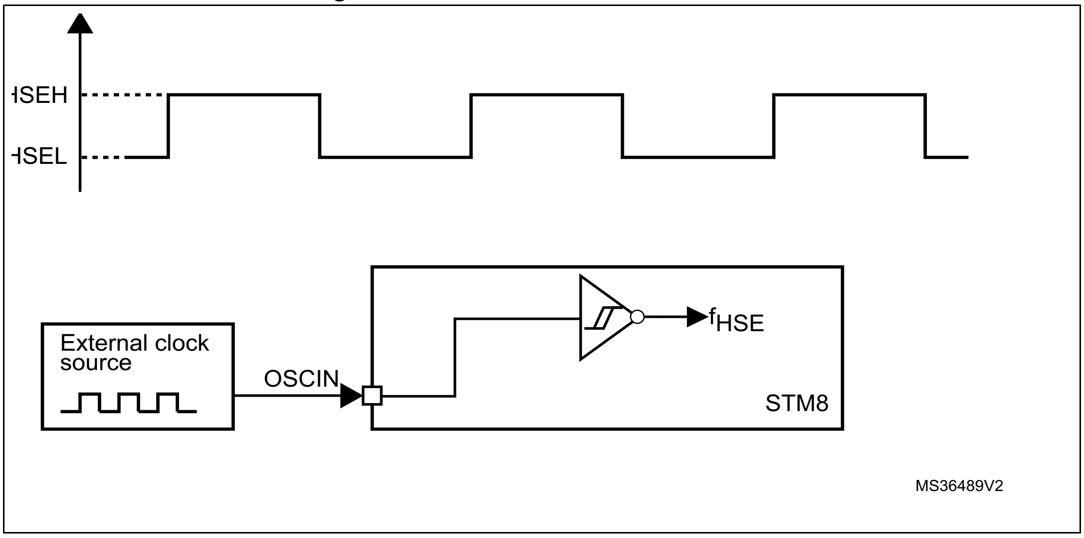
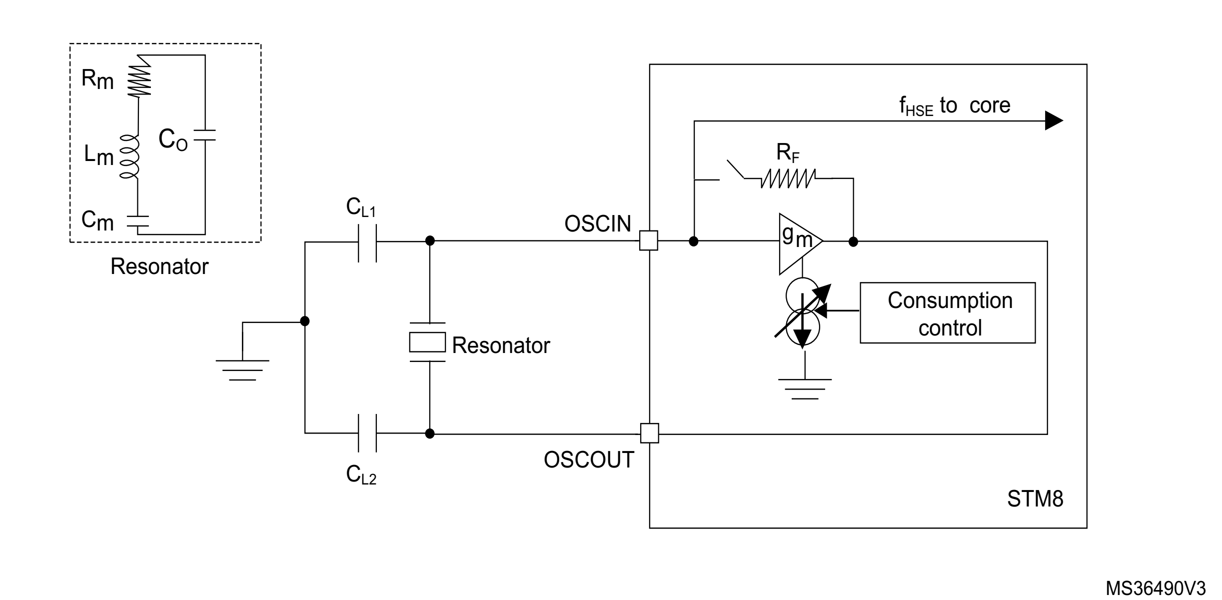


Figure 20. HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

Figure 24. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

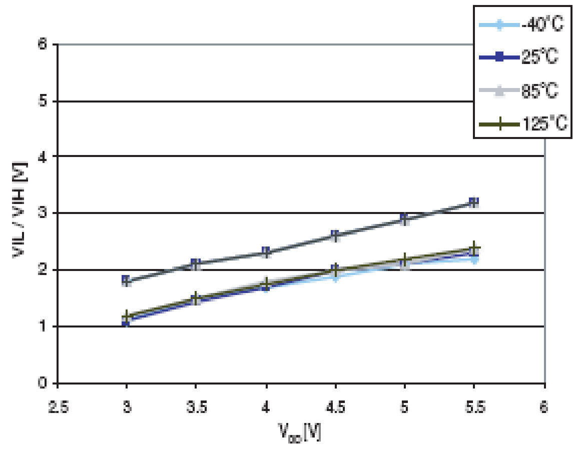


Figure 25. Typical pull-up current vs V_{DD} @ 4 temperatures

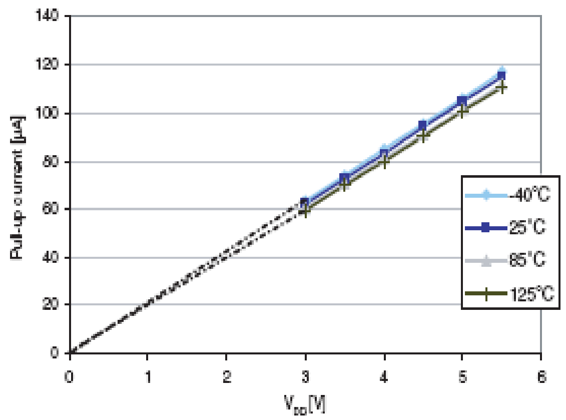


Figure 26. Typical pull-up resistance vs VDD @ 4 temperatures

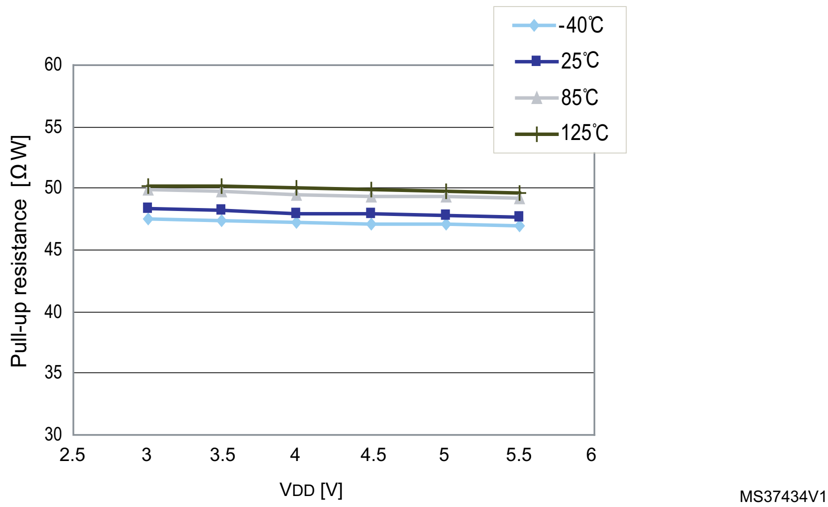


Table 38. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0[1]	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.4	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.0[1]	-	

1. Data based on characterization results, not tested in production

10.3.8 Reset pin characteristics

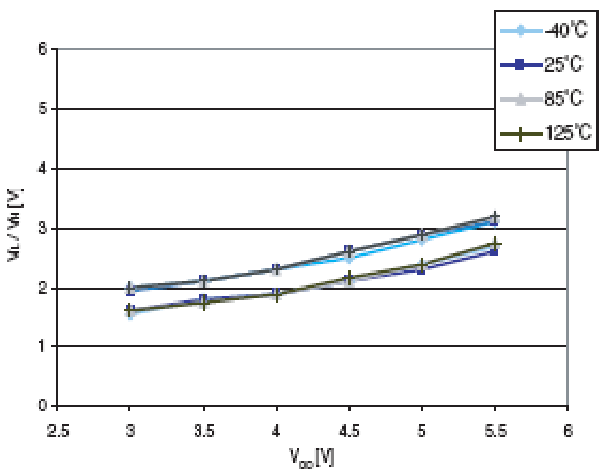
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

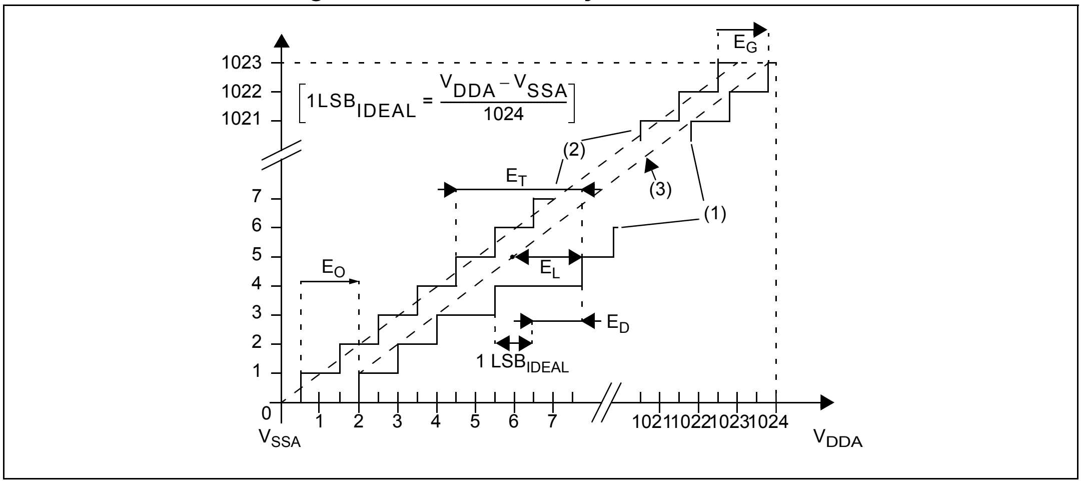
1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

Figure 37. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures



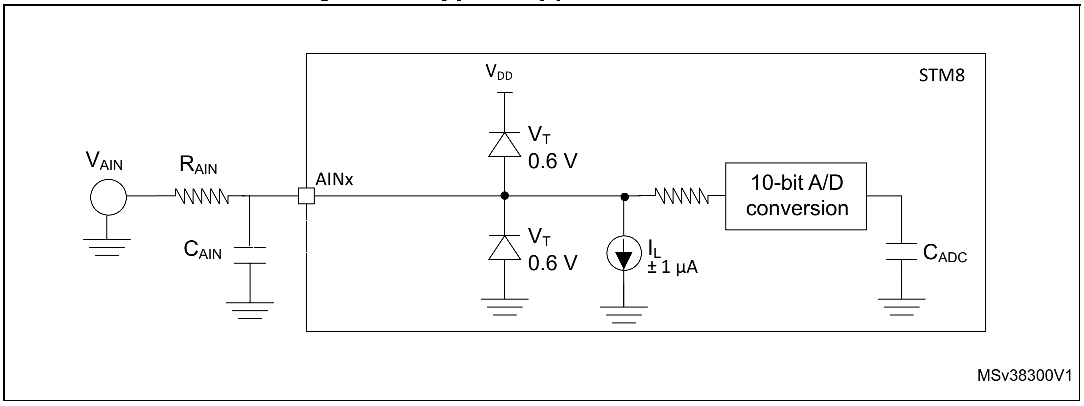
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Figure 45. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
E_O = Offset error: deviation between the first actual transition and the first ideal one.
E_G = Gain error: deviation between the last ideal transition and the last actual one.
E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 46. Typical application with ADC



1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 47. EMS data

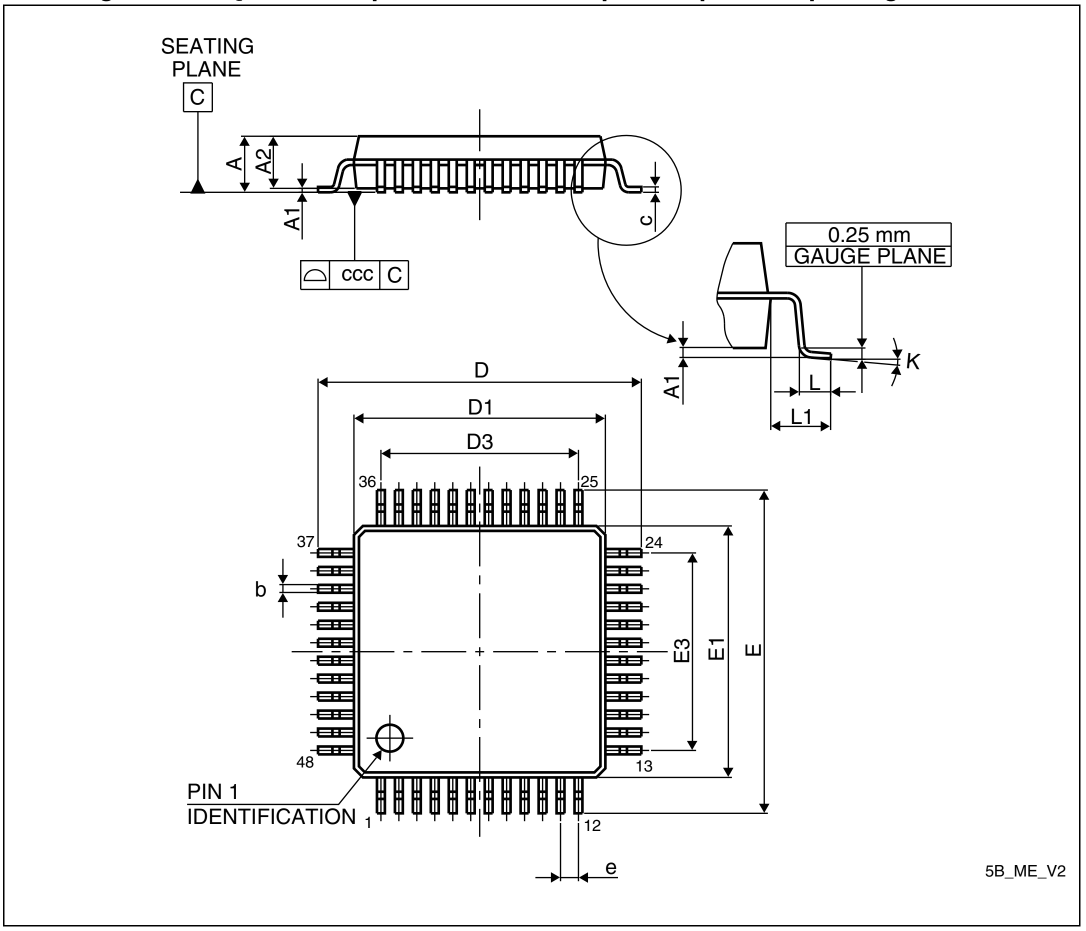
Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A(1)

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 LQFP48 package information

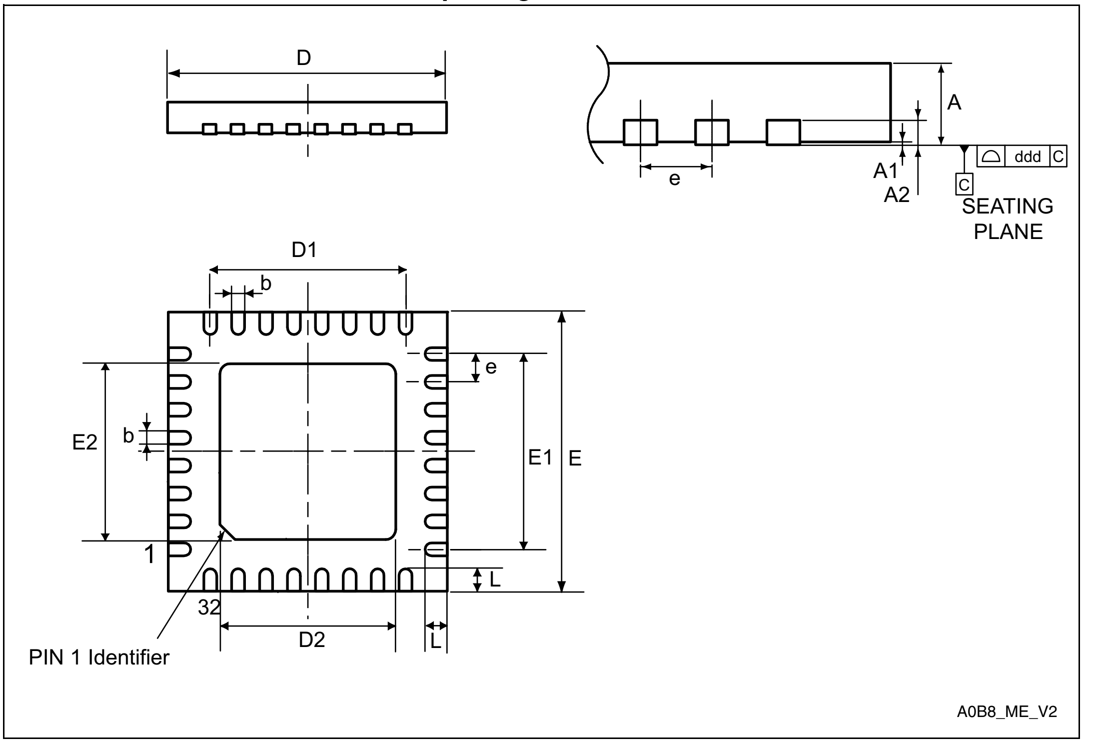
Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

11.4 UFQFPN32 package information

Figure 56. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

11.5 SDIP32 package information

Figure 59. SDIP32 package outline

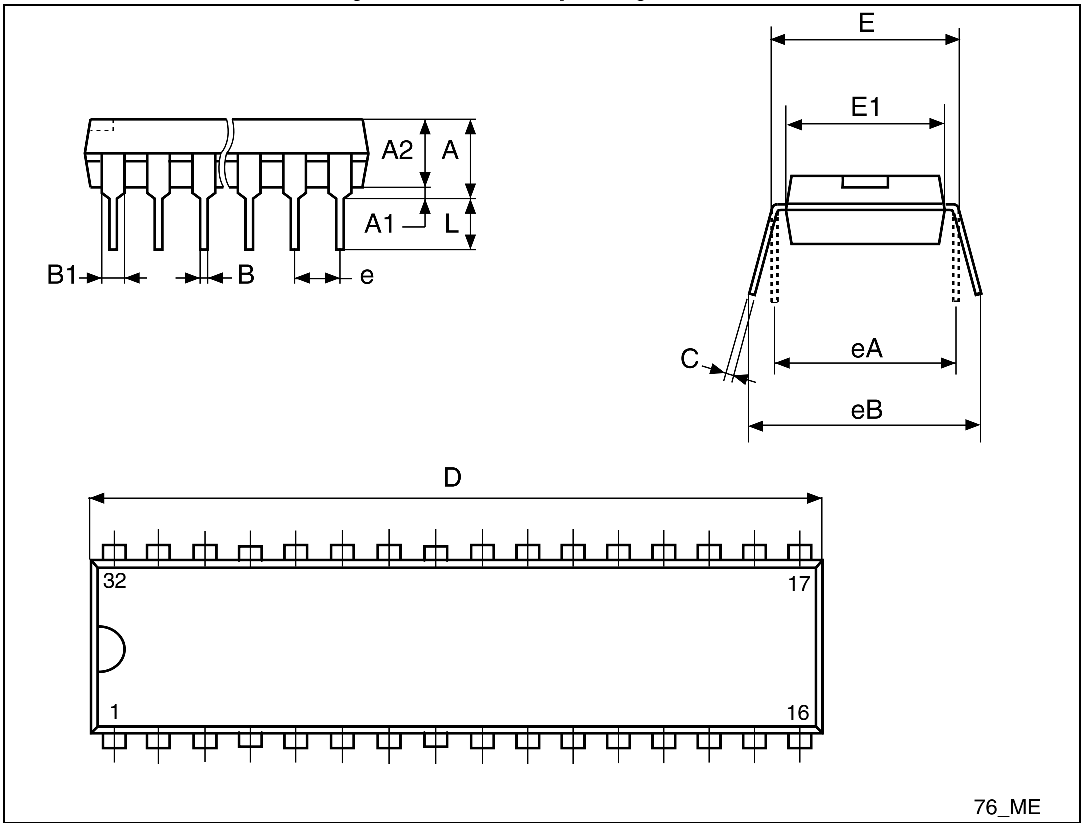


Table 55. SDIP32 package mechanical data

Dim.	mm			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

OTP7 is reserved

OTPBL bootloader option byte (check only one option)

Refer to the UM0560 (STM8L/S bootloader manual) for more details.

[ ] Disable (00h)

[ ] Enable (55h)

Comments:	....
Supply operating range in the application:	....
Notes:	....
Date:	....
Signature:	....

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

Table 57. Document revision history (continued)

Date	Revision	Changes
07-Feb-2014	13	UART2_CK mapped to correct pin (pin 24) in *Figure: LQFP 44-pin pinout.* Reserved area updated in *Table: Option bytes.* Package Information updated in *Table: 32-lead ultra thin fine pitch quad flat no-lead package mechanical data.*
01-Jul-2015	14	Added: – *Figure 49: LQFP48 marking example (package top view)*, – *Figure 52: LQFP44 marking example (package top view)*, – *Figure 55: LQFP32 marking example (package top view)*, – *Figure 58: UFQFPN32 marking example (package top view)*, – *Figure 60: SDIP32 marking example (package top view)*. Updated: – *Figure 41: SPI timing diagram where slave mode and CPHA = 0*, – the standard for EMI data in *Table 48: EMI data*.
23-Sep-2015	15	Added the footnotes related to *Figure 56: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*.