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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105c6t6tr

Table 1. STM8S105x4/6 access line features

Device	STM8S105C6	STM8S105C4	STM8S105S6	STM8S105S4	STM8S105K6	STM8S105K4
Pin count	48	48	44	44	32	32
Maximum number of GPIOs	38	38	34	34	25	25
Ext. Interrupt pins	35	35	31	31	23	23
Timer CAPCOM channels	9	9	8	8	8	8
Timer complementary outputs	3	3	3	3	3	3
A/D Converter channels	10	10	9	9	7	7
High sink I/Os	16	16	15	15	12	12
Medium density Flash Program memory (byte)	32K	16K	32K	16K	32K	16K
Data EEPROM (bytes)	1024	1024	1024	1024	1024	1024
RAM (bytes)	2K	2K	2K	2K	2K	2K
Peripheral set	Advanced control timer (TIM1), General-purpose timers (TIM2 and TIM3), Basic timer (TIM4) SPI, I2C, UART, Window WDG, Independent WDG, ADC					

4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

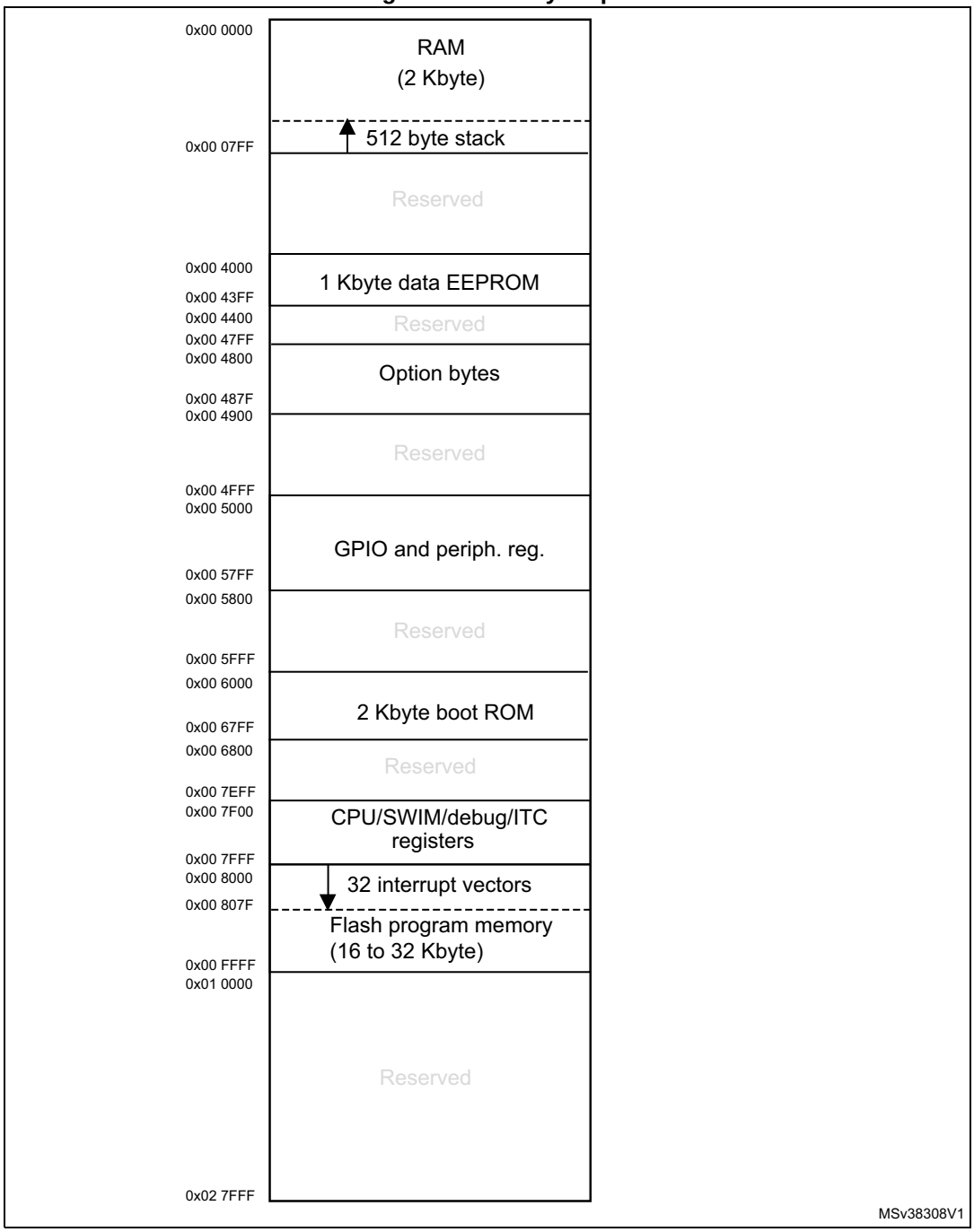
Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

6 Memory and register map

6.1 Memory map

Figure 7. Memory map



The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C Own address register low	0x00
0x00 5214		I2C_OARH	I2C Own address register high	0x00
0x00 5215		Reserved		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x0X
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230 to 0x00 523F	Reserved area (6 byte)			
0x00 5240	UART2	UART2_SR	UART2 status register	0xC0
0x00 5241		UART2_DR	UART2 data register	0xXX
0x00 5242		UART2_BRR1	UART2 baud rate register 1	0x00
0x00 5243		UART2_BRR2	UART2 baud rate register 2	0x00
0x00 5244		UART2_CR1	UART2 control register 1	0x00
0x00 5245		UART2_CR2	UART2 control register 2	0x00
0x00 5246		UART2_CR3	UART2 control register 3	0x00
0x00 5247		UART2_CR4	UART2 control register 4	0x00
0x00 5248		UART2_CR5	UART2 control register 5	0x00
0x00 5249		UART2_CR6	UART2 control register 6	0x00
0x00 524A		UART2_GTR	UART2 guard time register	0x00
0x00 524B		UART2_PSCR	UART2 prescaler register	0x00
0x00 524C to 0x00 524F	Reserved area (4 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00

10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 16. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
ΣI_{IO}	Total output current sourced (sum of all I/O and control pins) for devices with two V_{DDIO} pins(3)	200	
	Total output current sourced (sum of all I/O and control pins) for devices with one V_{DDIO} pin(3)	100	
	Total output current sunk (sum of all I/O and control pins) for devices with two V_{SSIO} pins(3)	160	
	Total output current sunk (sum of all I/O and control pins) for devices with one V_{SSIO} pin(3)	80	
$I_{INJ(PIN)}$ (4) (5)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(6)	±4	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(6)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 30. Peripheral current consumption

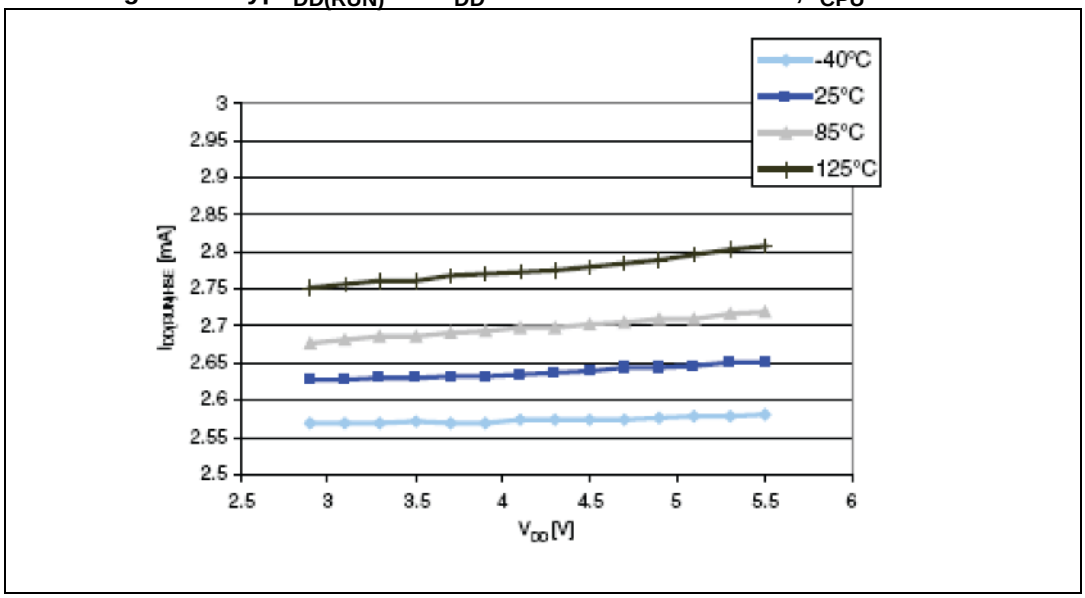
Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	230	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	115	
$I_{DD(TIM3)}$	TIM3 supply current(1)	90	
$I_{DD(TIM4)}$	TIM4 supply current(1)	30	
$I_{DD(UART2)}$	UART2 supply current (2)	110	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	955	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)(3)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Low speed internal RC oscillator (LSI)

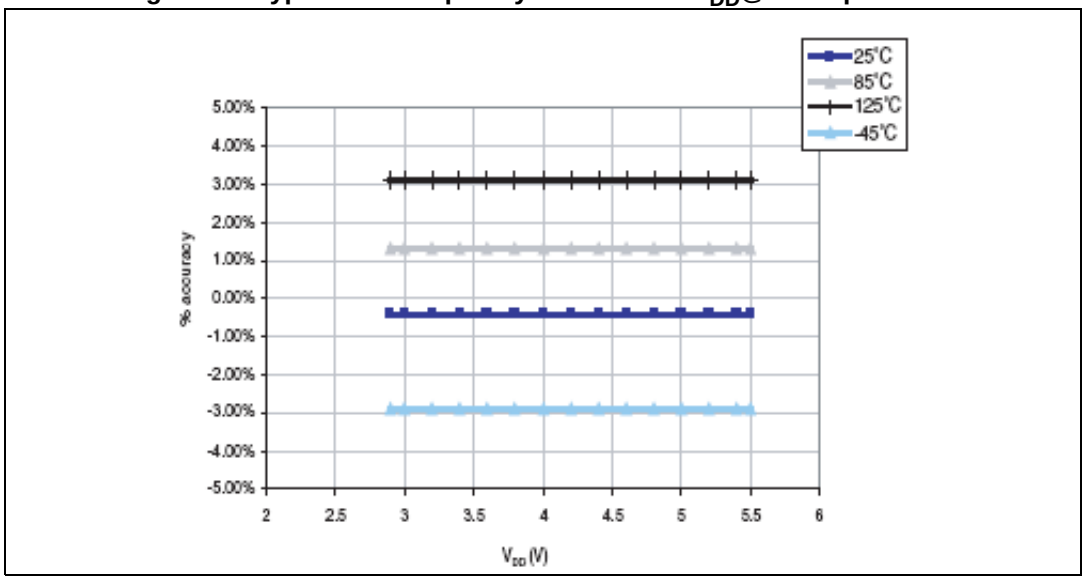
Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110	128	150	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs
IDD(LSI)	LSI oscillator power consumption	-	-	5	-	µA

1. Guaranteed by design, not tested in production.

Figure 23. Typical LSI frequency variation vs V_{DD}@ 4 temperatures



10.3.5 Memory characteristics

RAM and hardware registers

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Section 10.3: Operating conditions* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

Table 36. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU}≤ 16 MHz	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/128 byte)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 byte)	-	-	3	3.33	
t_{erase}	Erase time for 1 block (128 byte)	-	-	3	3.33	
N_{RW}	Erase/write cycles (program memory)(2)	T_A = +85 °C	10k	-	-	cycle
	Erase/write cycles (data memory)(2)	T_A = +125 °C	300k	1M	-	
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at T_A= +55 °C	T_{RET} = 55 °C	20	-	-	year
	Data retention (data memory) after 300k erase/write cycles at T_A= +125°C	T_{RET} = 85 °C	1	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 byte)	-	-	2	-	mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Figure 24. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

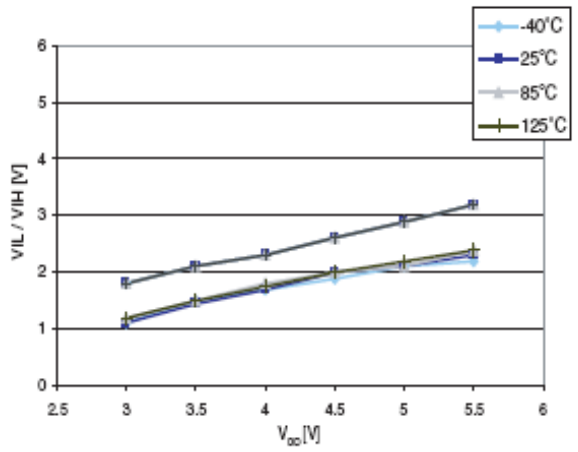


Figure 25. Typical pull-up current vs V_{DD} @ 4 temperatures

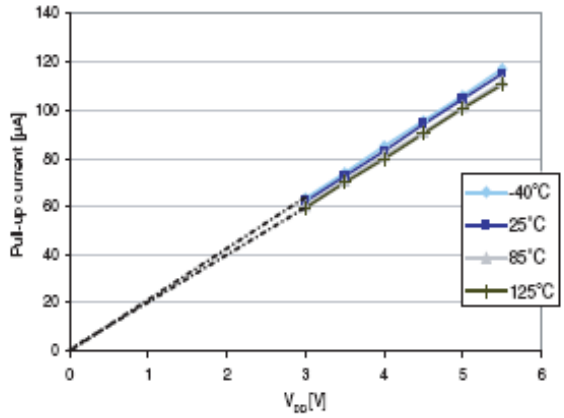


Figure 26. Typical pull-up resistance vs VDD @ 4 temperatures

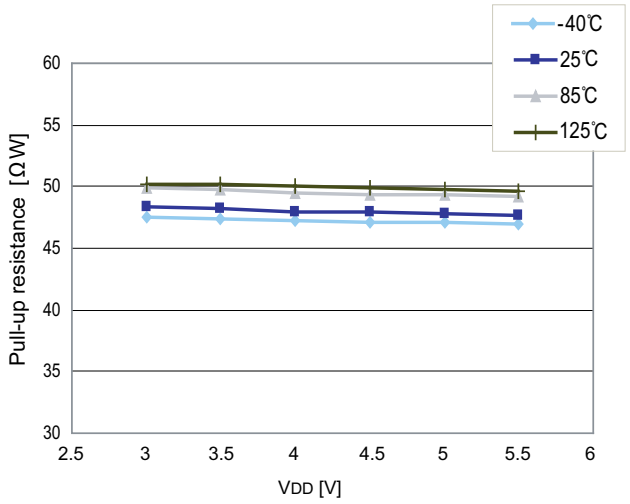


Table 38. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.4	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.0(1)	-	

1. Data based on characterization results, not tested in production

Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

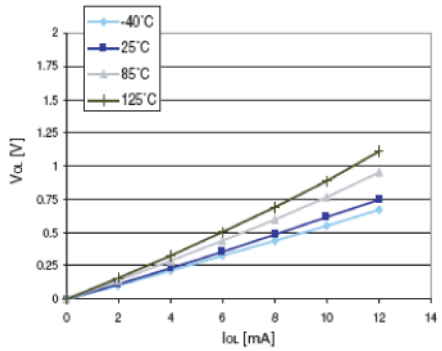


Figure 30. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

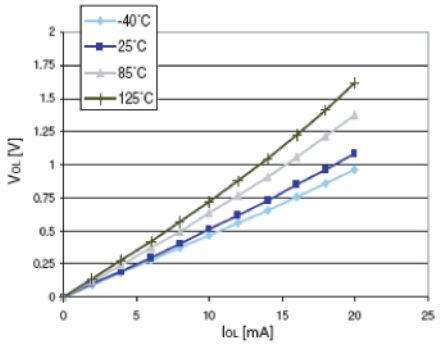


Figure 31. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

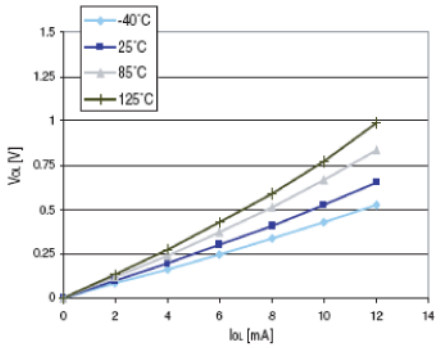
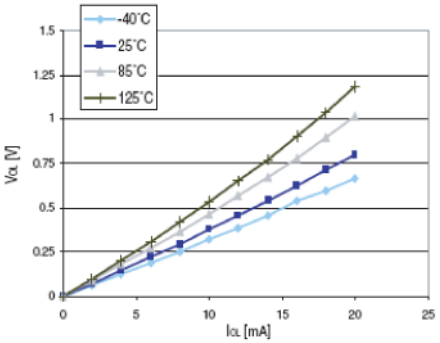


Figure 32. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)



10.3.8 Reset pin characteristics

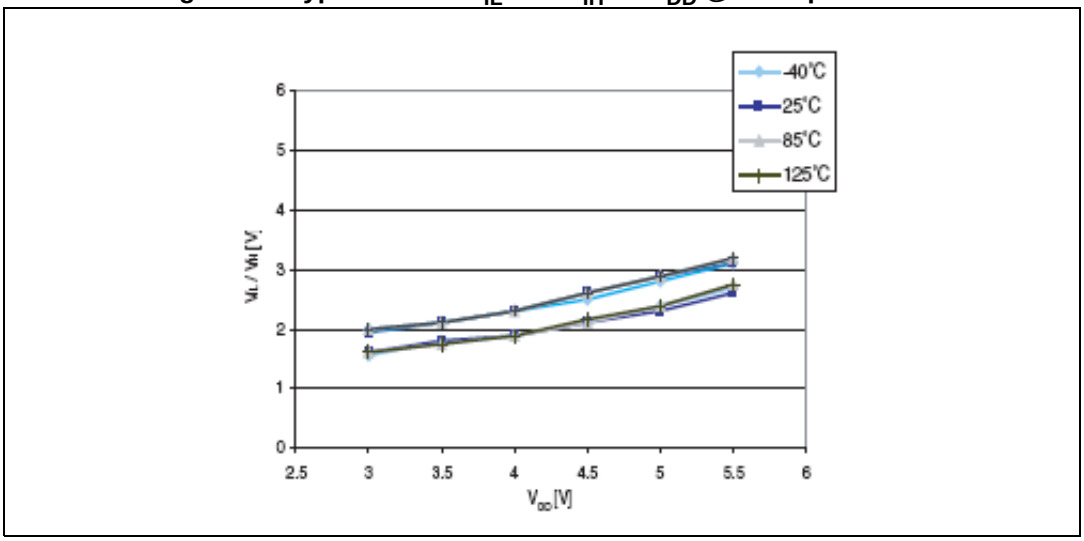
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

Figure 37. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures



10.3.10 I²C interface characteristics

Table 43. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 44. Typical application with I²C bus and timing diagram

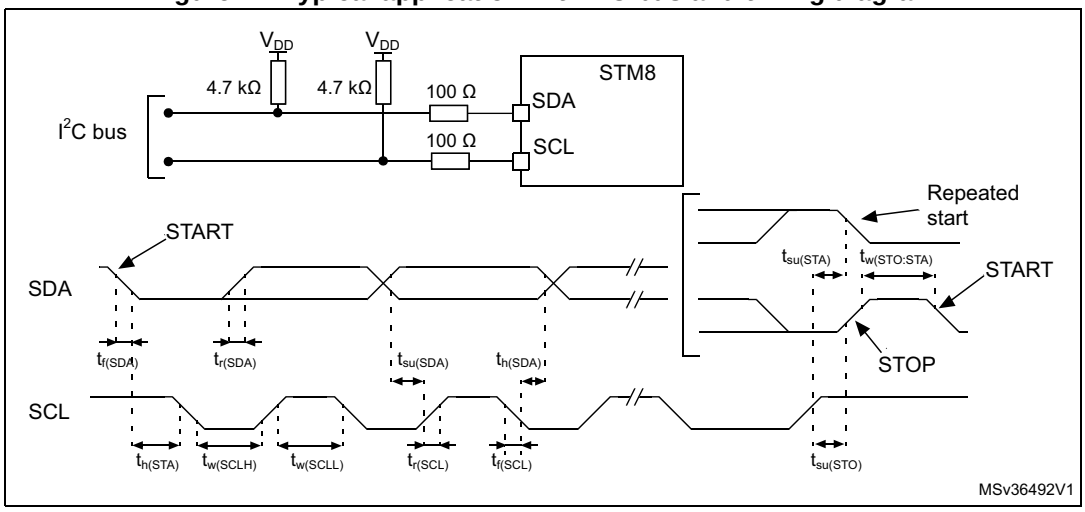
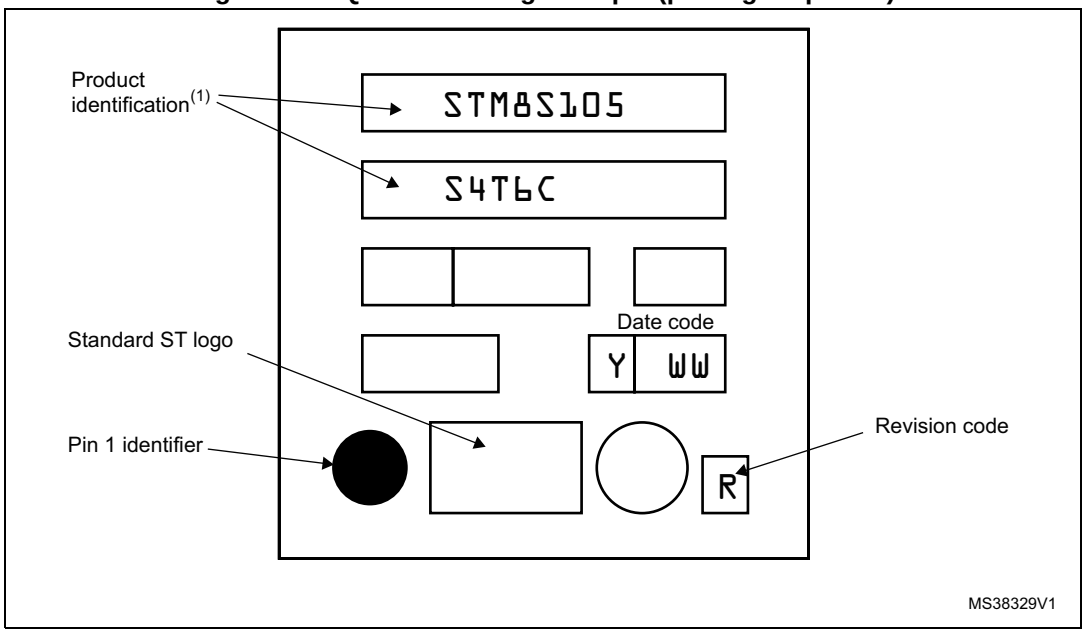


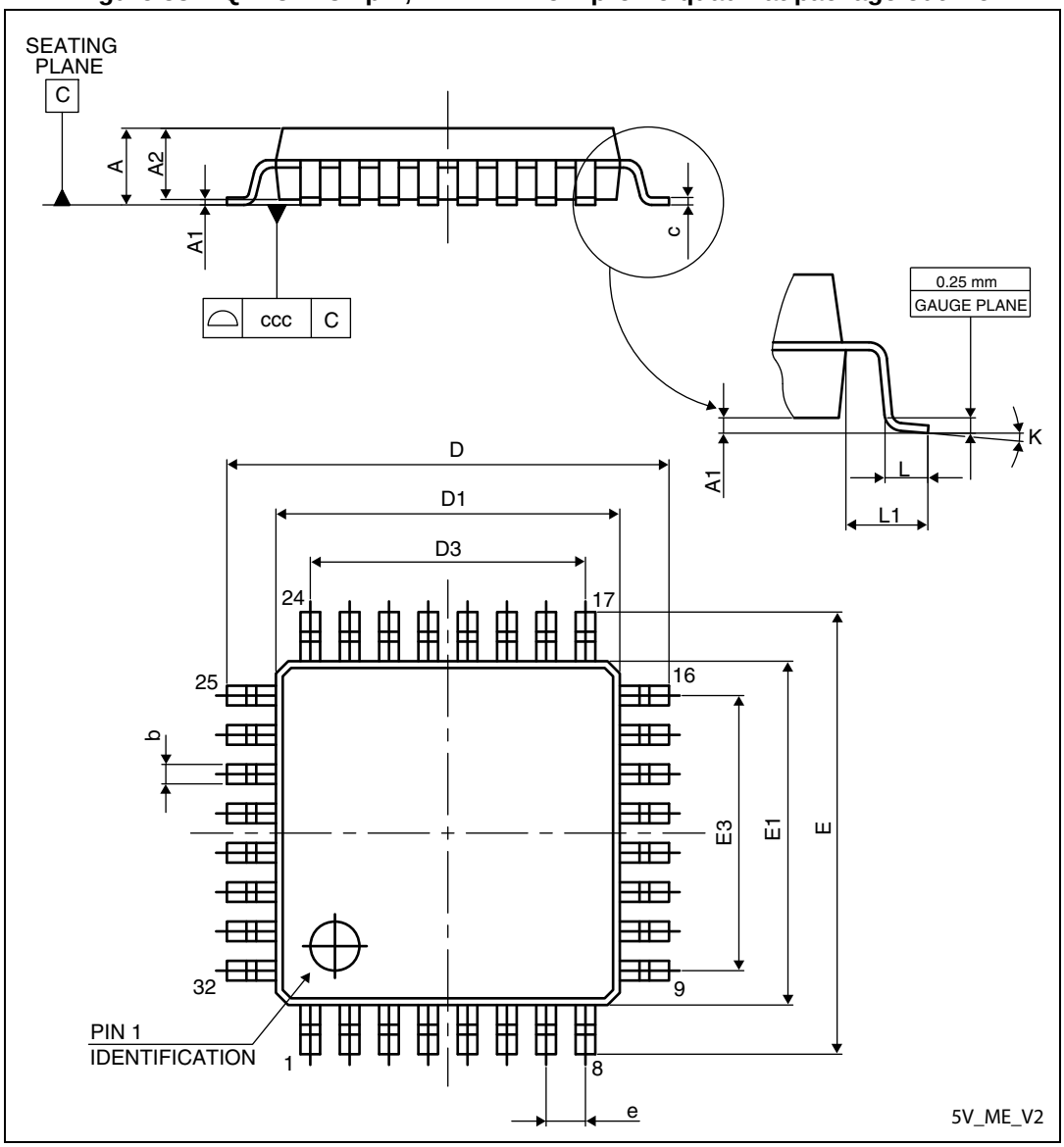
Figure 52. LQFP44 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11.3 LQFP32 package information

Figure 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 55. SDIP32 package mechanical data (continued)

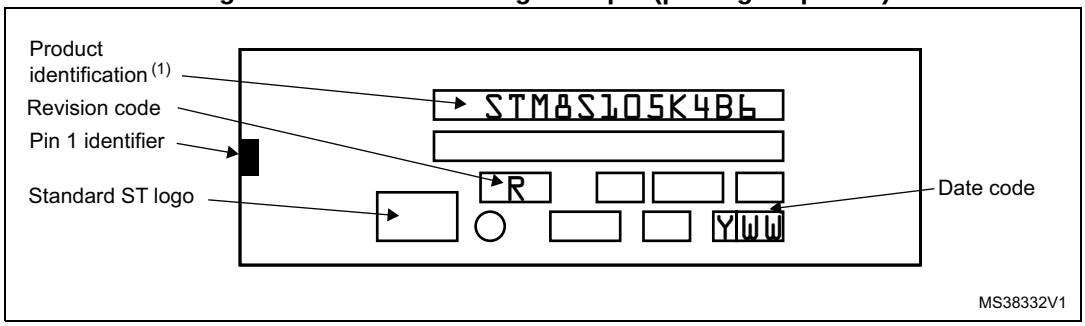
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eB	-	-	12.700	-	-	0.5000
L	2.540	3.048	3.810	0.1000	0.1200	0.1500

1. Values in inches are converted from mm and rounded to 4 decimal digits

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 60. SDIP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 57. Document revision history (continued)

Date	Revision	Changes
21-Sep-2010	10	*Table: Legend/Abbreviations for pinout tables:* updated "reset state"; removed "HS", (T), and "[ ]". *Section: Pin description for STM8S105 microcontrollers:* added footnotes to the PF4 and PD1 pins. *Table: I/O port hardware register map:* changed reset status of Px_IDR from 0x00 to 0xXX. *Table: General hardware register map*: Standardized all address and reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, UART2_DR, and ADC_DRx registers; replaced reserved address "0x00 5248" with the UART2_CR5. *Section: Recommended reset pin protection*: replaced 0.01 µF with 0.1 µF Updated *Figure: Typical application with I2C bus and timing diagram*. Updated *Table: ADC accuracy with RAIN < 10 kohm , VDDA = 5 V* footnote 1 in and Table: ADC accuracy with RAIN < 10 kohm RAIN, VDDA = 3.3 V. *Section: STM8S105 FASTROM microcontroller option list*: removed bits 6 and 7 from OPT1 user boot code area (UBC); added "disable" to 00h and "enable" to 55h of OPTBL bootloader option byte. *Section: VFQFPN Package Mechanical data*: replaced note 1 and added note 2.
04-Apr-2012	11	Removed VFQFPN32 package. Modified *Section: Description*. Remove weak pull-up input for PE1 and PE2 in *Table: Pin description for STM8S105 microcontrollers* Updated *Table: Interrupt mapping* for TIM2 and TIM4. Updated notes related to VCAP in xm-replace_text General operating conditions. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Section: I/O static characteristics*. Updated typical and maximum values of RPU in *Table: I/O static characteristics* and *Table: RST pin characteristics*. Changed SCK input to SCK output in *Table: SPI serial peripheral interface.* Added Θ_{JA} for UFQFPN32 and SDIP32 in *Table: Thermal characteristics*, and updated *Section: Selecting the product temperature range*
28-Jun-2012	12	Added UFQFPN package thickness in *Figure: STM8S105xx access line ordering information scheme*