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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	32-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k4b6

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

4.6   Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.

- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.

- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.

- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7   Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1.   Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.

2.   Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

Figure 6. SDIP32 pinout
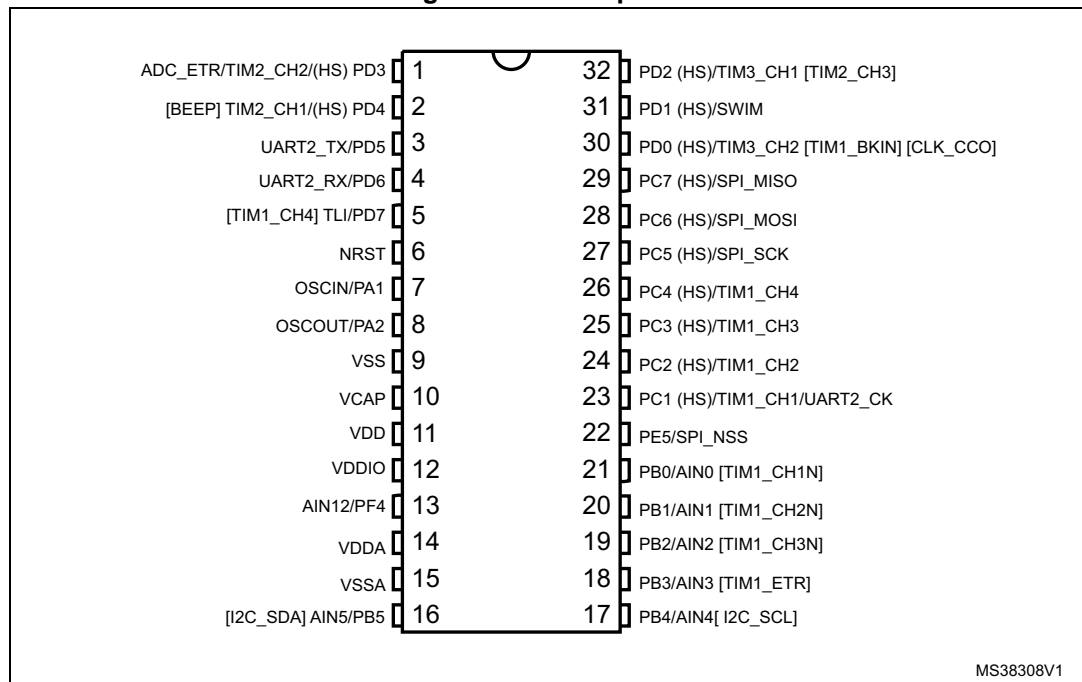
1. (HS) high sink capability.

2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).

3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	6	NRST	I/O	-	**X**	-	-		-	-	Reset		-
2	2	2	7	PA1/ OSC IN	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
3	3	3	8	PA2/ OSC OUT	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
4	4	-	-	VSSIO_1	S	-	-	-	-	-	-	-	I/O ground		-
5	5	4	9	VSS	S	-	-	-	-	-	-	-	Digital ground		-
6	6	5	10	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input				Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	22	-	-	PE6/ AIN9	I/O	**X**	X	X	-	O1	X	X	Port E6	Analog input 9[3]	-
25	23	17	22	PE5/ SPI_NSS	I/O	**X**	X	X	-	O1	X	X	Port E5	SPI master/ slave select	-
26	24	18	23	PC1/ TIM1_CH1/ UART2_CK	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1/UART2 synchronous clock	-
27	25	19	24	PC2/ TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1- channel 2	-
28	26	20	25	PC3/ TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
29	-	21	26	PC4/ TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4	-
30	27	22	27	PC5/ SPI_SCK	I/O	**X**		X	HS	O3	X	X	Port C5	SPI clock	-
31	28	-	-	VSSIO_2	S	-	-	-	-	-	-	-	I/O ground		-
32	29	-	-	VDDIO_2	S	-	-	-	-	-	-	-	I/O power supply		-
33	30	23	28	PC6/ SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-
34	31	24	29	PC7/ SPI_ MISO	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
35	32	-	-	PG0	I/O	**X**	X	-	-	O1	X	X	Port G0	-	-
36	33	-	-	PG1	I/O	**X**	X	-	-	O1	X	X	Port G1	-	-
37	-	-	-	PE3/ TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	Port E3	Timer 1 - break input	-
38	34	-	-	PE2/ I 2C_ SDA	I/O	**X**	-	X	-	O1	T (4)	-	Port E2	I 2C data	-
39	35	-	-	PE1/ I2C_ SCL	I/O	**X**	-	X	-	O1	T (4)	-	Port E1	I 2C clock	-

6 Memory and register map

6.1 Memory map

Figure 7. Memory map
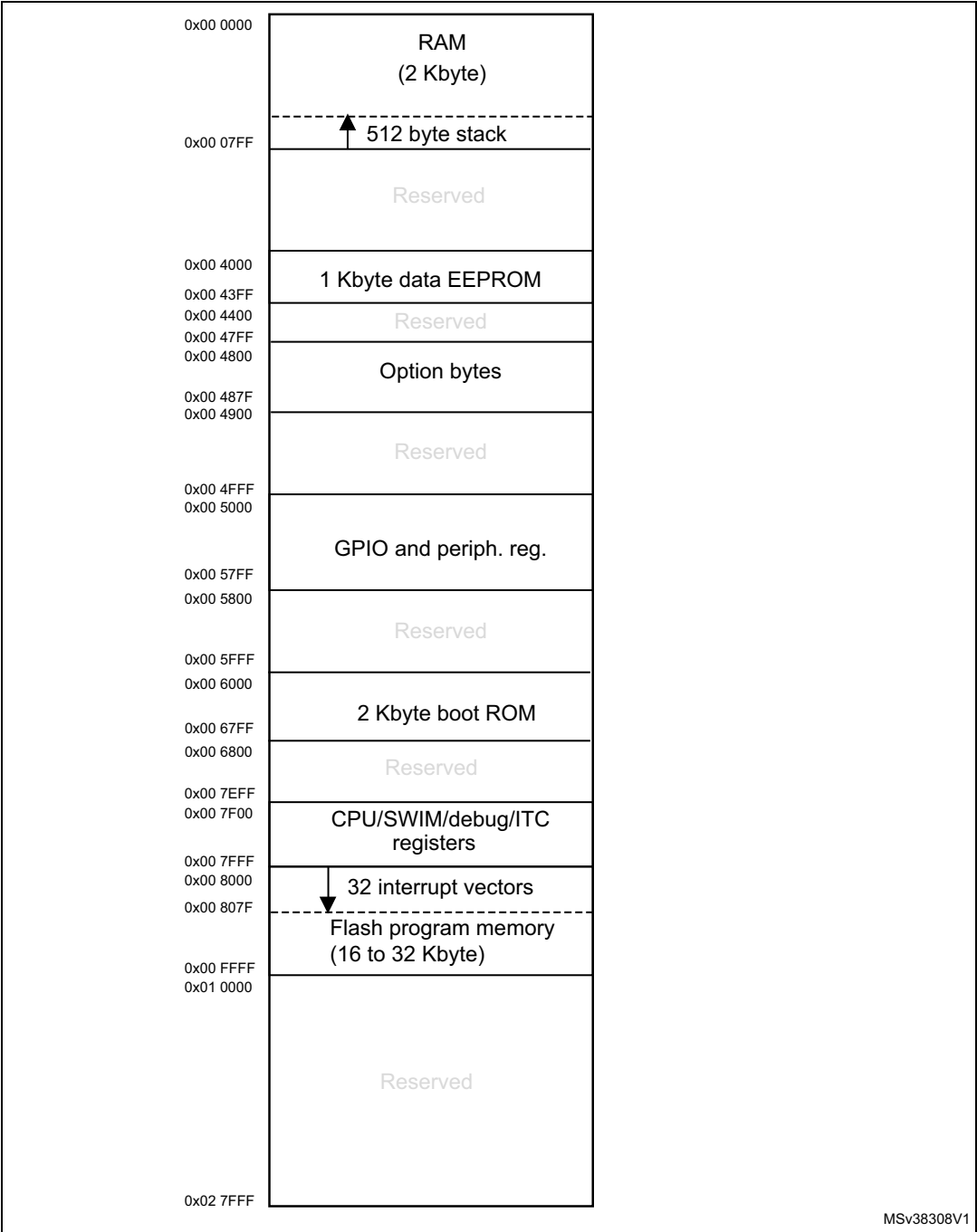
The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

6.2.2 General hardware register map

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX[1]
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

9   Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x48CD	X co-ordinate on the wafer	U_ID[7:0]							
0x48CE		U_ID[15:8]							
0x48CF	Y co-ordinate on the wafer	U_ID[23:16]							
0x48D0		U_ID[31:24]							
0x48D1	Wafer number	U_ID[39:32]							
0x48D2	Lot number	U_ID[47:40]							
0x48D3		U_ID[55:48]							
0x48D4		U_ID[63:56]							
0x48D5		U_ID[71:64]							
0x48D6		U_ID[79:72]							
0x48D7		U_ID[87:80]							
0x48D8		U_ID[95:88]							

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\ °C$, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\ °C$, $V_{DD} = 5.0\ V$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Typical current consumption

For typical current consumption measurements, VDD, VDDIO and VDDA are connected together in the configuration shown in the following figure.
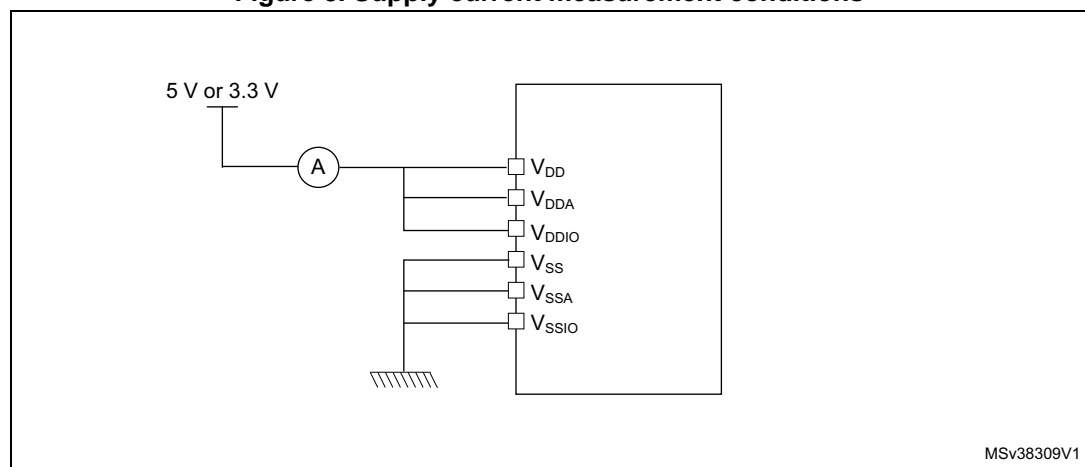
Figure 8. Supply current measurement conditions

Table 25. Total current consumption in active halt mode at V$_{DD}$ = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C[1]	Max at 85 °C[1]	Unit
		Main voltage regulator (MVR)[2]	Flash mode[3]	Clock source				
I$_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	680	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	320	400	
			Power down mode	HSE crystal osc. (16 MHz)	630	-	-	
			Power down mode	LSI RC osc. (128 kHz)	140	270	350	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	120	220	
			Power down mode	LSI RC osc. (128 kHz)	10	60	150	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

**Table 26. Total current consumption in halt mode at V$_{DD}$ = 5 V**

Symbol	Parameter	Conditions	Typ	Max at 85 °C[1]	Max at 85 °C[1]	Unit
I$_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	62	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	6.5	25	80	

1. Data based on characterization results, not tested in production.

Table 27. Total current consumption in halt mode at V$_{DD}$ = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C[1]	Max at 85 °C[1]	Unit
I$_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	20	80	

1. Data based on characterization results, not tested in production.

Figure 14. Typ I$_{DD(RUN)}$ vs. f$_{CPU}$ HSE user external clock, V$_{DD}$ = 5 V
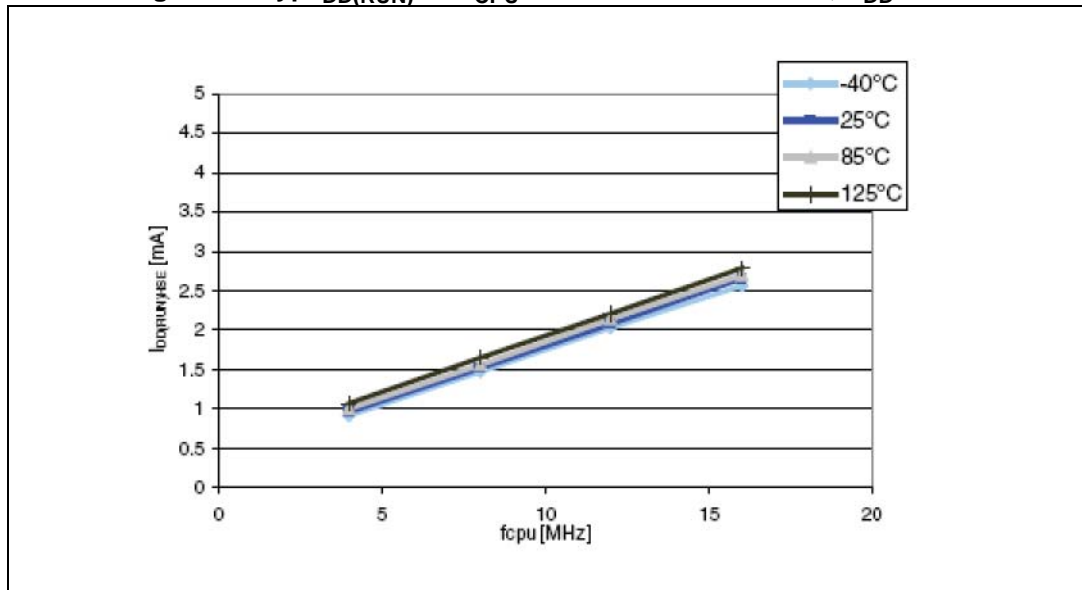
Figure 15. Typ I$_{DD(RUN)}$ vs. V$_{DD}$ HSI RC osc, f$_{CPU}$ = 16 MHz
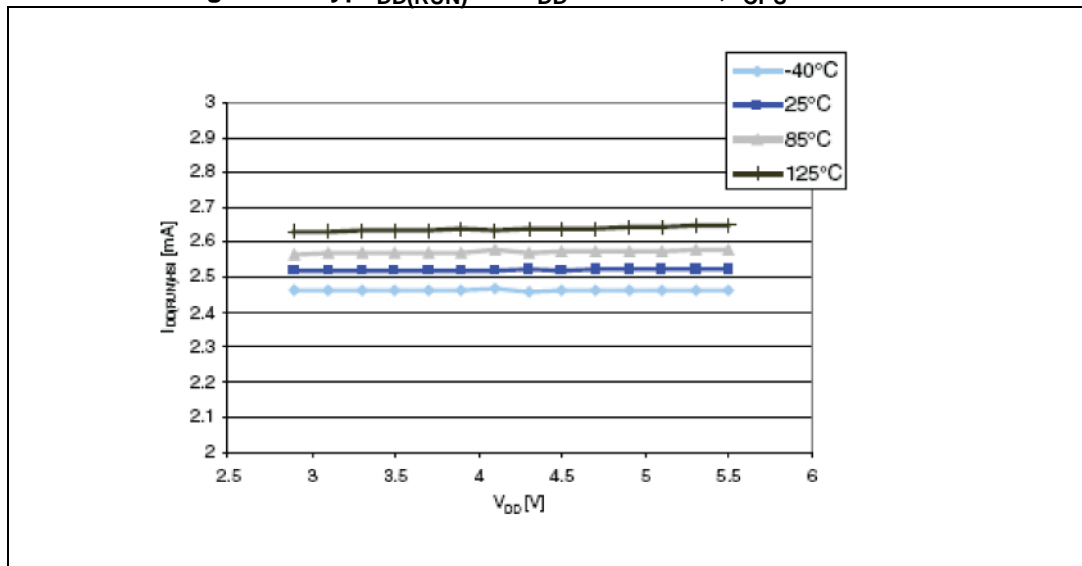
HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance[2]	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)[3]	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)[3]	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.

2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details

3. Data based on characterization results, not tested in production.

4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	$V_{DD} = 5$ V	-0.3 V	-	$0.3 \times V_{DD}$	V
V_{IH}	Input high level voltage		$0.7 \times V_{DD}$	-	$V_{DD} + 0.3$ V	
V_{hys}	Hysteresis[1]		-	700	-	mV
R_{pu}	Pull-up resistor	$V_{DD} = 5$ V, $V_{IN} = V_{SS}$	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35[2]	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125[2]	
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 20 pF	-	-	20[2]	ns
		Standard and high sink I/Os Load = 20 pF	-	-	50[2]	
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1[3]	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250[3]	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1[3]	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

2. Data guaranteed by design.

3. Data based on characterization results, not tested in production

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	2/B[1]
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A[1]

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 50. Electrical sensitivities

| Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	$T_A = 25 °C$	A
		$T_A = 85 °C$	
		$T_A = 125 °C$	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 LQFP48 package information

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.
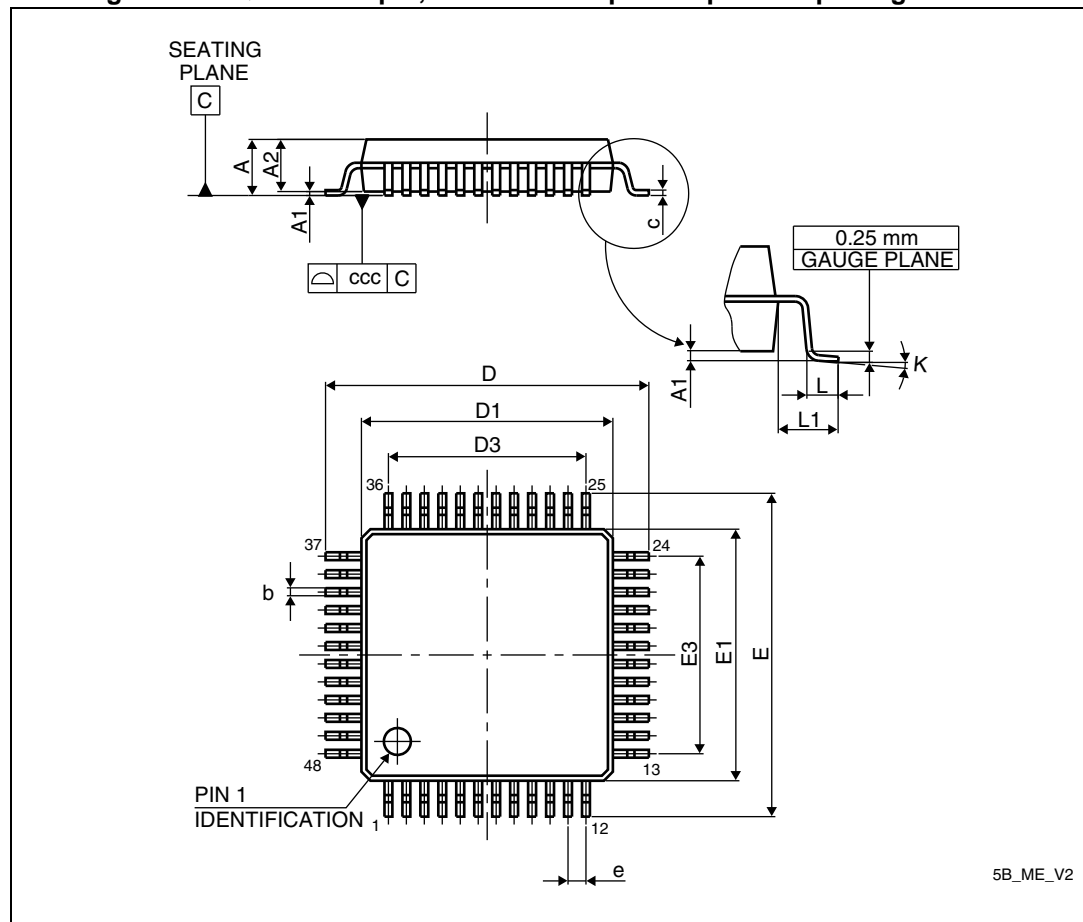
Table 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set

OTP2 alternate function remapping

AFR0 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D3 alternate function = ADC_ETR
AFR1 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3
AFR2 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = CLK_CCO *Note: if both AFR2 and AFR3 are activated, AFR2 option has priority over AFR3.*
AFR3 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = TIM1_BKIN

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.