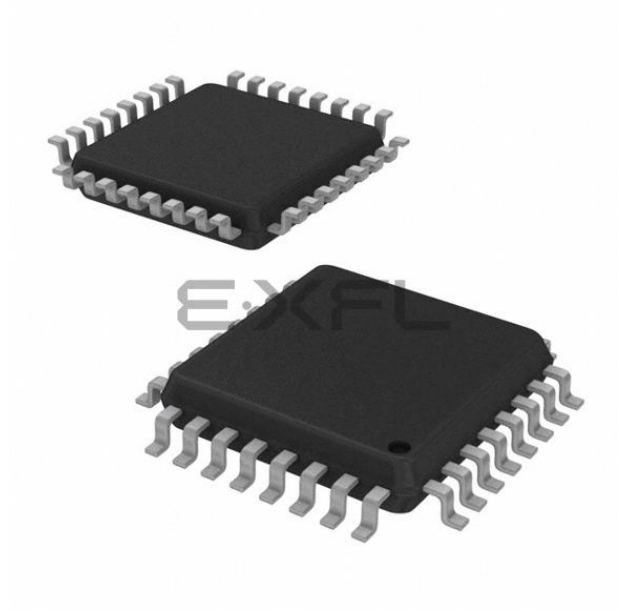

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k4t3ctr

Contents

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

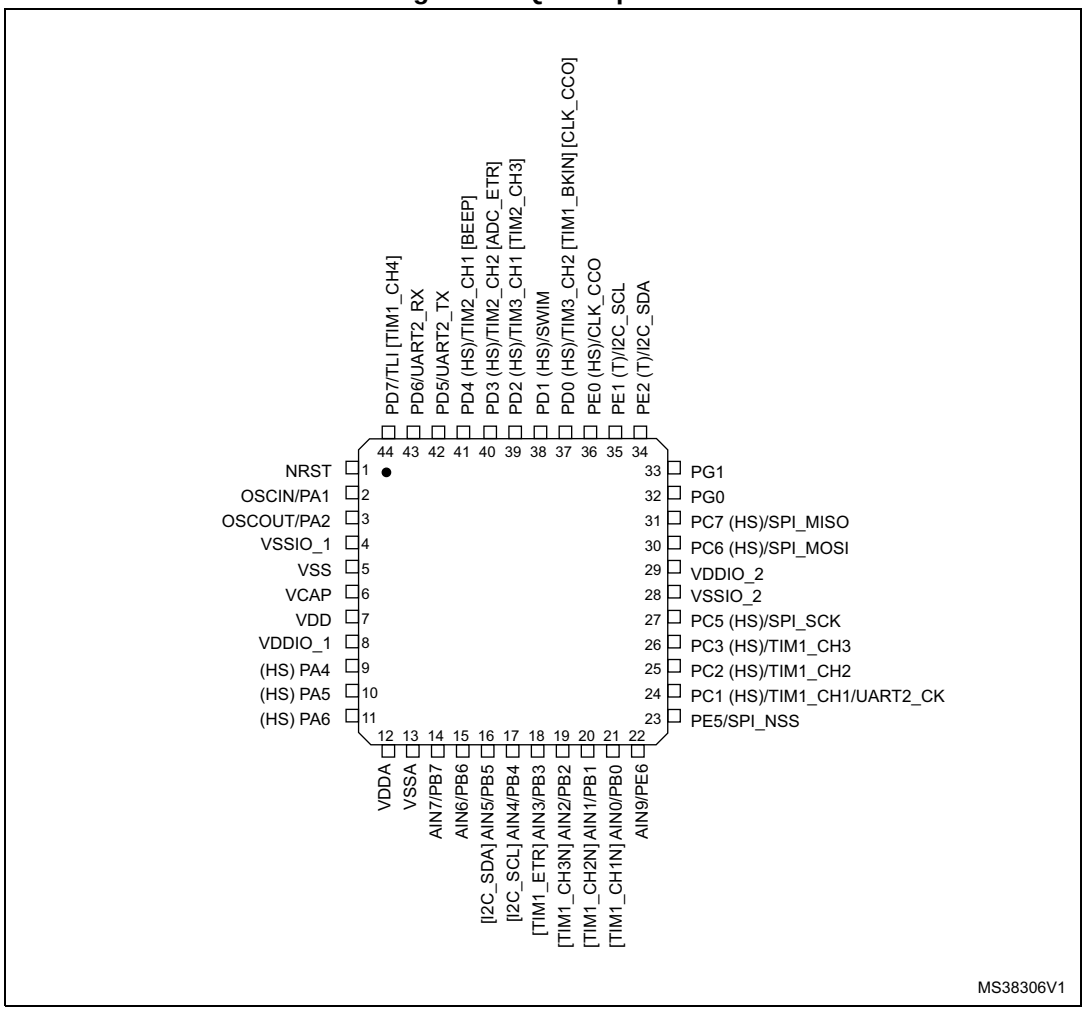
This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Figure 4. LQFP44 pinout

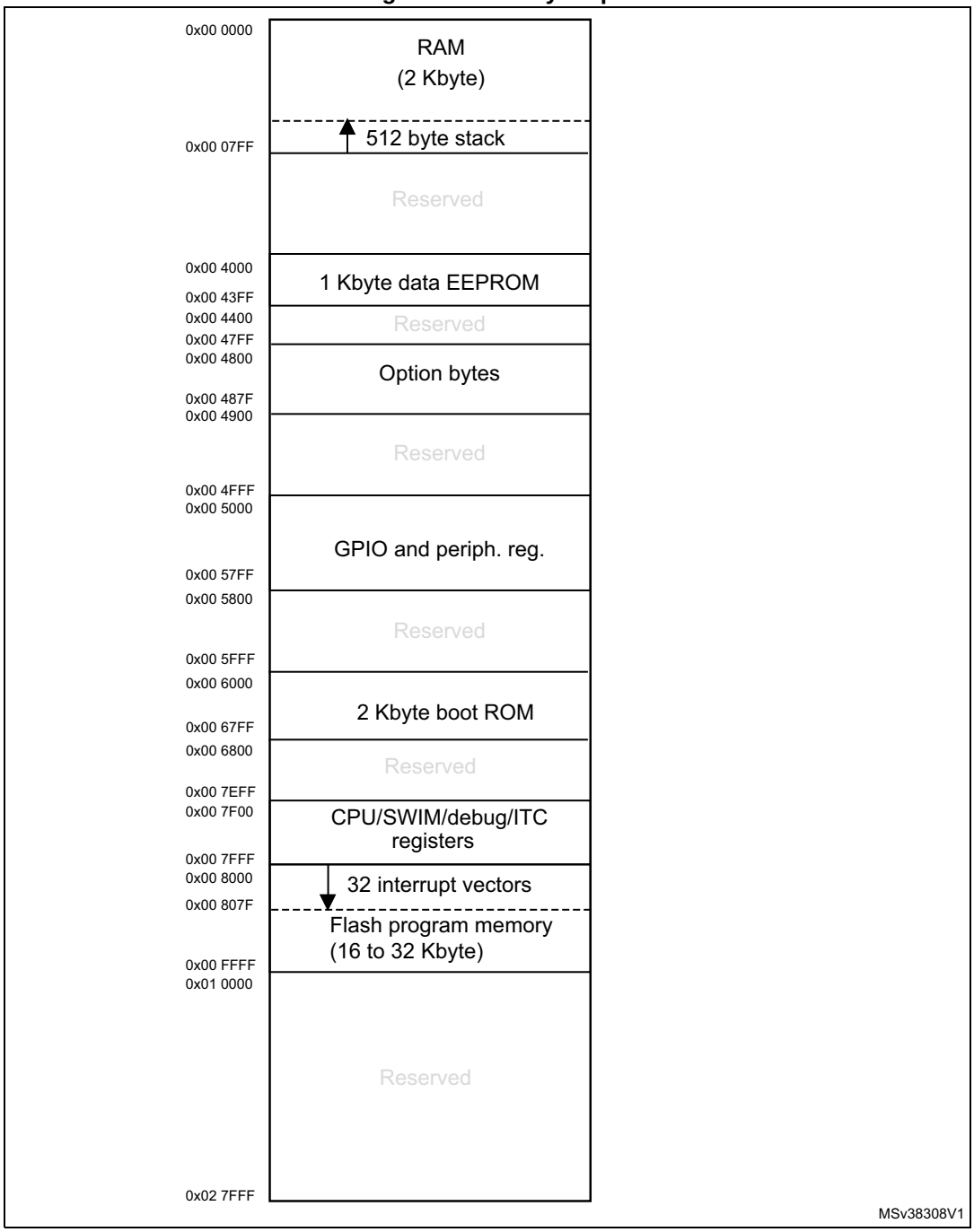


1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

6 Memory and register map

6.1 Memory map

Figure 7. Memory map



The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

6.2.2 General hardware register map

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved	-	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM2	TIM2 update/ overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/ compare	-	-	0x00 8040
15	TIM3	TIM3 update/ overflow	-	-	0x00 8044
16	TIM3	TIM3 capture/ compare	-	-	0x00 8048
17	Reserved	-	-	-	0x00 804C
18	Reserved	-	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054

8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified ‘on the fly’ by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF
0x480B	Reserved	OPT6	Reserved								0x00
0x480C		NOPT6	Reserved								0xFF
0x480D	Reserved	OPT7	Reserved								0x00
0x480E		NOPT7	Reserved								0xFF
0x480F	Reserved	-	Reserved								-
0x48FD		-	Reserved								-

Table 19. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.65	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.8	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	7.3	-	mA
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc. (16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.15	-	mA
			HSE user ext. clock (16 MHz)	1.55	2.0	
			HSI RC osc. (16 MHz)	1.5	1.9	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	1.3	-	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.7	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 42. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$[2]	NSS setup time	Slave mode	4 * t_{MASTER}	-	
$t_{h(NSS)}$[2]	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$[2] $t_{su(SI)}$[2]	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$[2] $t_{h(SI)}$[2]	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$[2][3]	Data output access time	Slave mode	-	3* t_{MASTER}	
$t_{dis(SO)}$[2][4]	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$[2]	Data output valid time	Slave mode (after enable edge)	-	73	
$t_{v(MO)}$[2]	Data output valid time	Master mode (after enable edge)	-	36	
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	28	-	
$t_{h(MO)}$[2]		Master mode (after enable edge)	12	-	

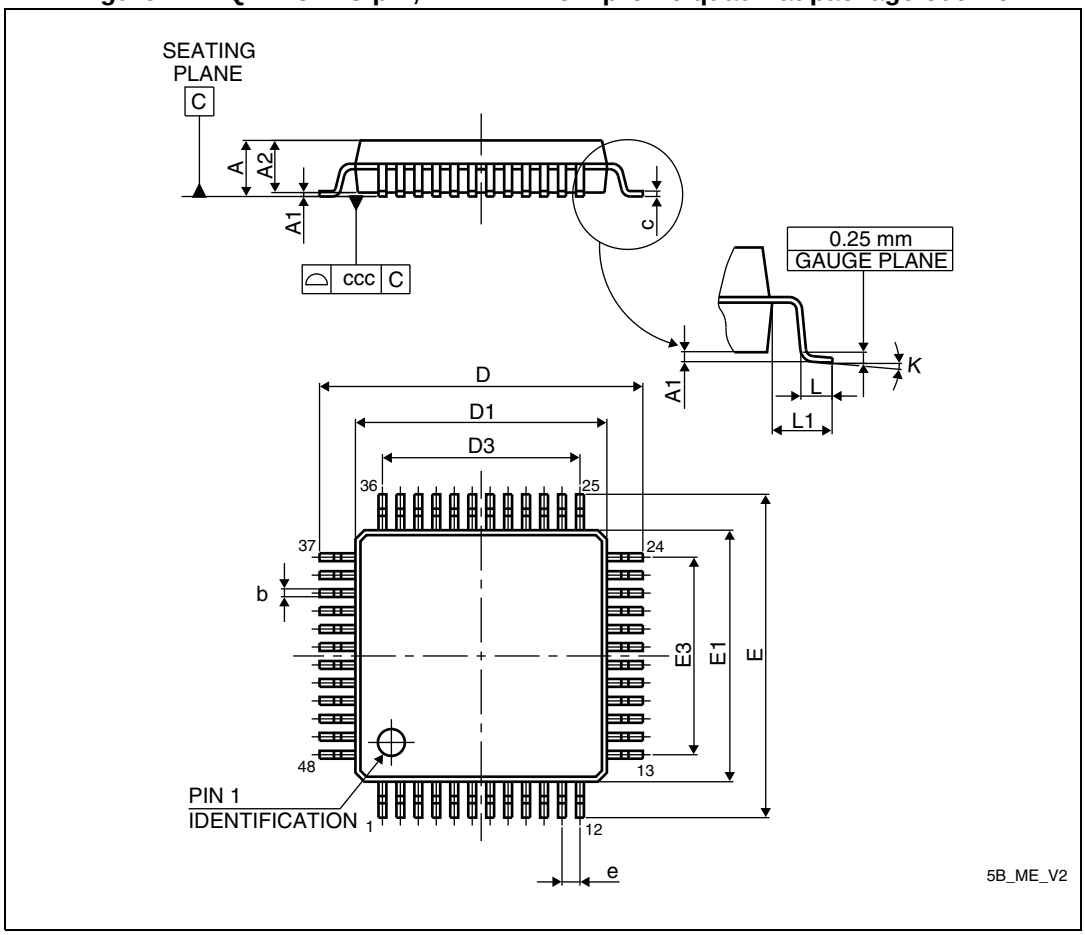
1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

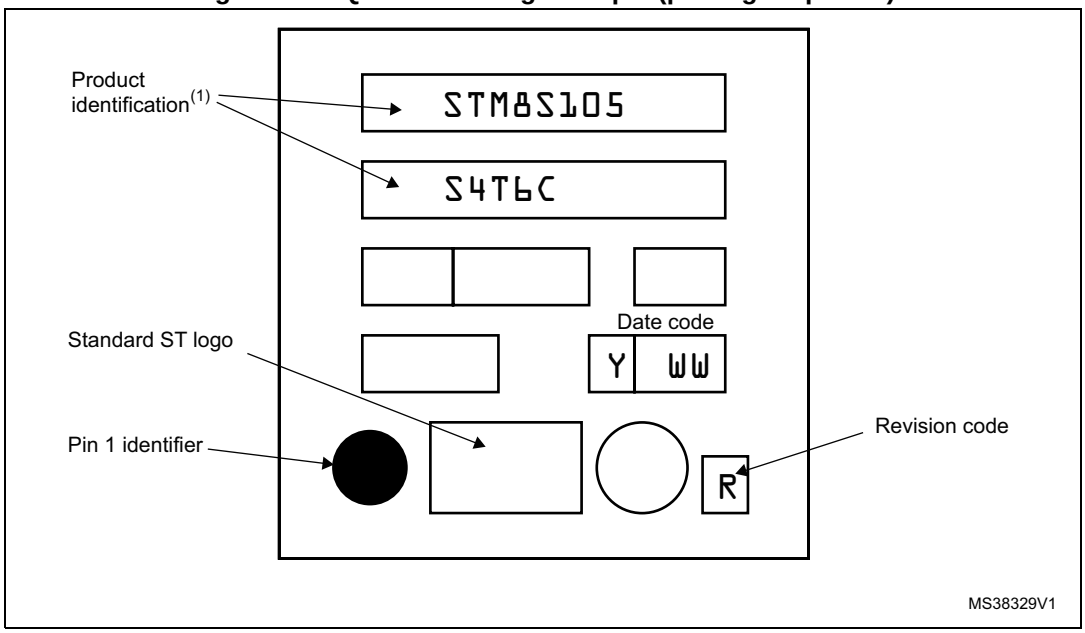
11.1 LQFP48 package information

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 52. LQFP44 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.5 SDIP32 package information

Figure 59. SDIP32 package outline

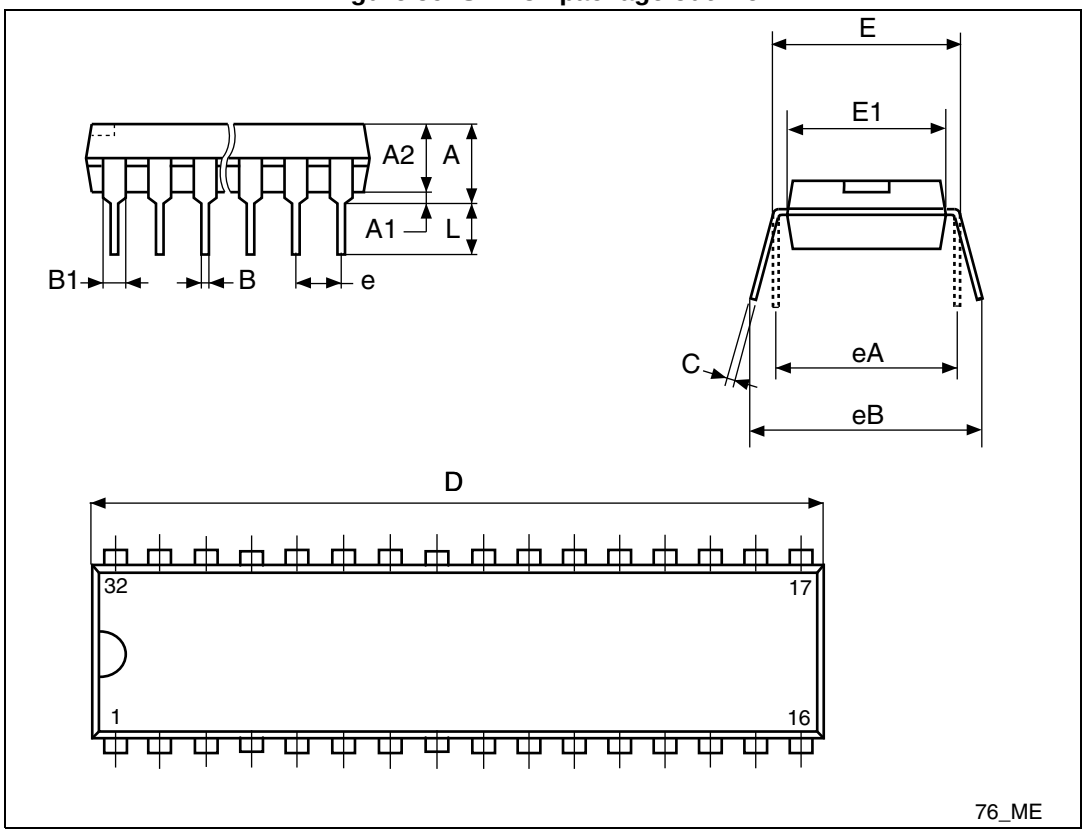
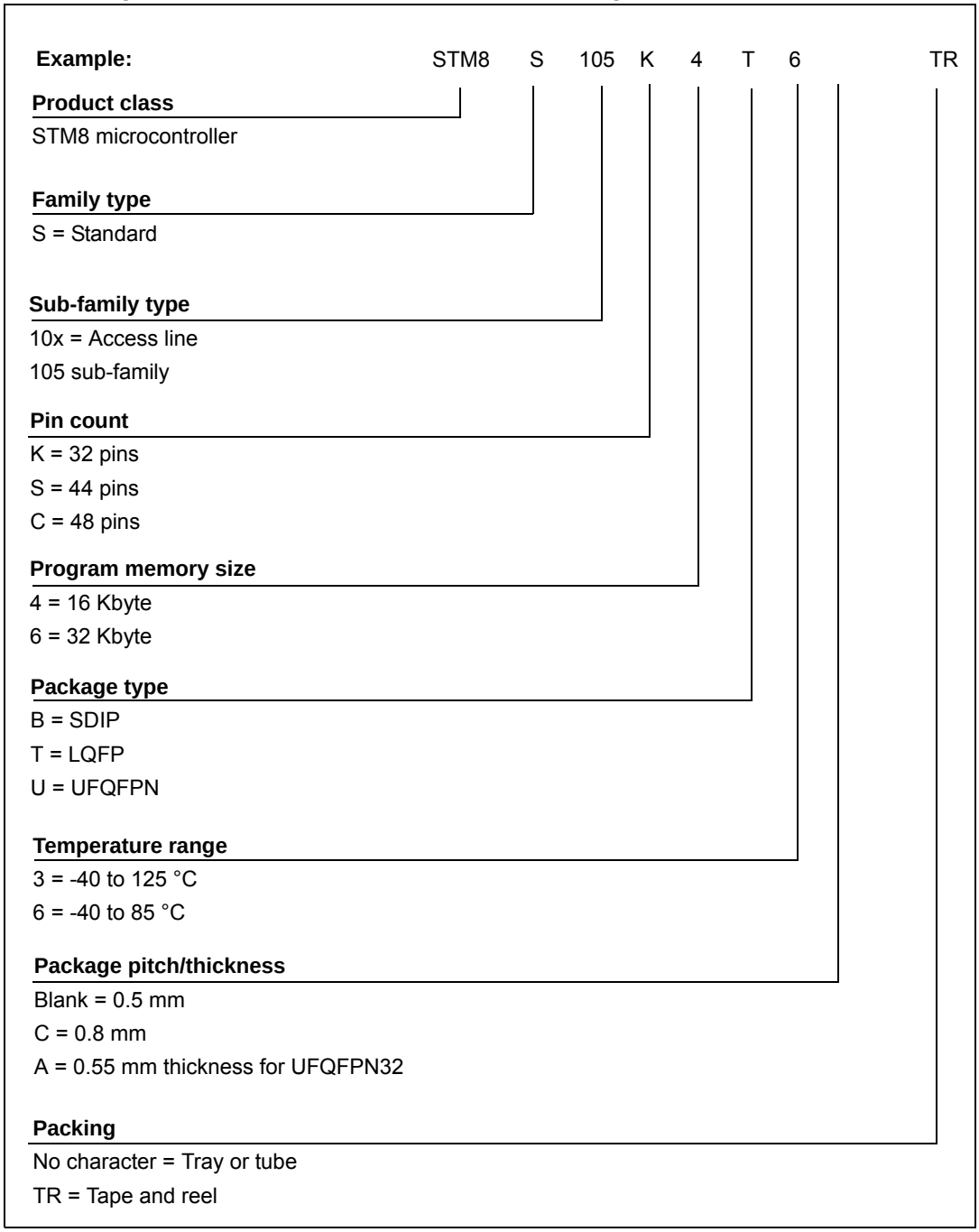


Table 55. SDIP32 package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

13 Ordering information

Figure 61. STM8S105x4/6 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set

OTP2 alternate function remapping

AFR0 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D3 alternate function = ADC_ETR
AFR1 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3
AFR2 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = CLK_CCO *Note: if both AFR2 and AFR3 are activated, AFR2 option has priority over AFR3.*
AFR3 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = TIM1_BKIN

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for the STM8 programming.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 57. Document revision history (continued)

Date	Revision	Changes
07-Feb-2014	13	UART2_CK mapped to correct pin (pin 24) in *Figure: LQFP 44-pin pinout.* Reserved area updated in *Table: Option bytes.* Package Information updated in *Table: 32-lead ultra thin fine pitch quad flat no-lead package mechanical data.*
01-Jul-2015	14	Added: – *Figure 49: LQFP48 marking example (package top view)*, – *Figure 52: LQFP44 marking example (package top view)*, – *Figure 55: LQFP32 marking example (package top view)*, – *Figure 58: UFQFPN32 marking example (package top view)*, – *Figure 60: SDIP32 marking example (package top view)*. Updated: – *Figure 41: SPI timing diagram where slave mode and CPHA = 0*, – the standard for EMI data in *Table 48: EMI data*.
23-Sep-2015	15	Added the footnotes related to *Figure 56: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*.