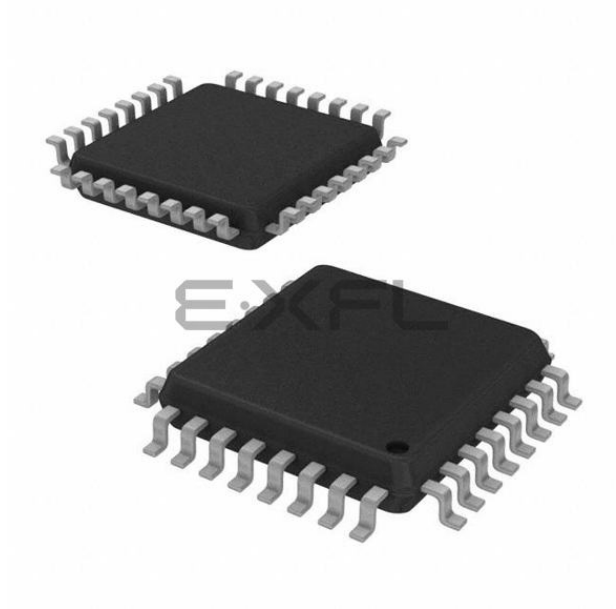


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.95V ~ 5.5V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k4t6c |

# Contents

The IWDG time base spans from 60 µs to 1 s.

## 4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

## 4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

## 4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

## 4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

# 5 Pinout and pin description

**Table 4. Legend/abbreviations for pin description tables**

| | | |
|---|---|---|
| **Type** | I= Input, O = Output, S = Power supply | |
| **Level** | Input | CM = CMOS |
| | Output | HS = High sink |
| **Output speed** | O1 = Slow (up to 2 MHz)<br>O2 = Fast (up to 10 MHz)<br>O3 = Fast/slow programmability with slow as default state after reset<br>O4 = Fast/slow programmability with fast as default state after reset | |
| **Port and control configuration** | Input | float = floating,<br>wpu = weak pull-up |
| | Output | T = True open drain,<br>OD = Open drain,<br>PP = Push pull |
| **Reset state** | Bold **X** (pin state after internal reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release. | |

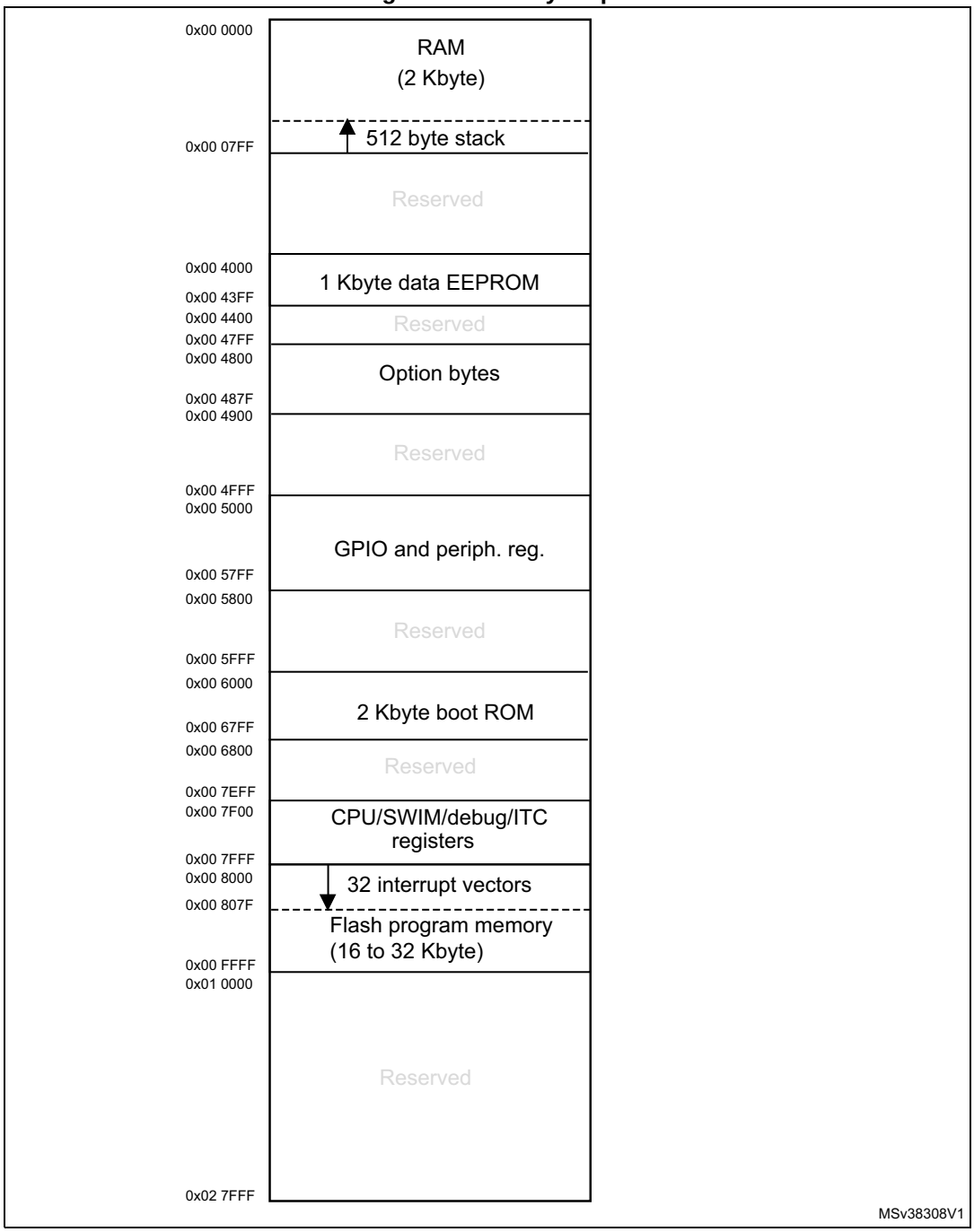
**Table 5. STM8S105x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP44 | LQFP32/UFQFPN32 | SDIP32 | | | Floating | wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 7 | 7 | 6 | 11 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 8 | 8 | 7 | 12 | VDDIO_1 | S | - | - | - | - | - | - | - | I/O power supply | | - |
| 9 | - | - | - | PA3/ TIM2_CH3 [TIM3_CH1] | I/O | **X** | X | X | - | O1 | X | X | Port A3 | Timer 2 - channel 3 | TIM3_ CH1 [AFR1] |
| 10 | 9 | - | - | PA4 | I/O | **X** | X | X | HS | O3 | X | X | Port A4 | - | - |
| 11 | 10 | - | - | PA5 | I/O | **X** | X | X | HS | O3 | X | X | Port A5 | - | - |
| 12 | 11 | - | - | PA6 | I/O | **X** | X | X | HS | O3 | X | X | Port A6 | - | - |
| - | - | 8 | 13 | PF4/ AIN12(1) | I/O | **X** | X | - | - | O1 | X | X | Port F4 | Analog input 12(2) | - |
| 13 | 12 | 9 | 14 | VDDA | S | - | - | - | - | - | - | - | Analog power supply | | - |
| 14 | 13 | 10 | 15 | VSSA | S | - | - | - | - | - | - | - | Analog ground | | - |
| 15 | 14 | - | - | PB7/ AIN7 | I/O | **X** | X | X | - | O1 | X | X | Port B7 | Analog input 7 | - |
| 16 | 15 | - | - | PB6/ AIN6 | I/O | **X** | X | X | - | O1 | X | X | Port B6 | Analog input 6 | - |
| 17 | 16 | 11 | 16 | PB5/ AIN5 [I2C_ SDA] | I/O | **X** | X | X | - | O1 | X | X | Port B5 | Analog input 5 | I 2C_SDA [AFR6] |
| 18 | 17 | 12 | 17 | PB4/ AIN4 [I2C_SCL] | I/O | **X** | X | X | - | O1 | X | X | Port B4 | Analog input 4 | I2C_SCL [AFR6] |
| 19 | 18 | 13 | 18 | PB3/ AIN3 [TIM1_ETR] | I/O | **X** | X | X | - | O1 | X | X | Port B3 | Analog input 3 | TIM1_ET R [AFR5] |
| 20 | 19 | 14 | 19 | PB2/ AIN2 [TIM1_CH3N] | I/O | **X** | X | X | - | O1 | X | X | Port B2 | Analog input 2 | TIM1_CH 3N [AFR5] |
| 21 | 20 | 15 | 20 | PB1/ AIN1 [TIM1_CH2N] | I/O | **X** | X | X | - | O1 | X | X | Port B1 | Analog input 1 | TIM1_CH 2N [AFR5] |
| 22 | 21 | 16 | 21 | PB0/ AIN0 [TIM1_CH1N] | I/O | **X** | X | X | - | O1 | X | X | Port B0 | Analog input 0 | TIM1_CH 1N [AFR5] |
| 23 | - | - | - | PE7/ AIN8 | I/O | **X** | X | X | - | O1 | X | X | Port E7 | Analog input 8 | - |

# 6 Memory and register map

## 6.1 Memory map

**Figure 7. Memory map**




The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

### 6.2.2 General hardware register map

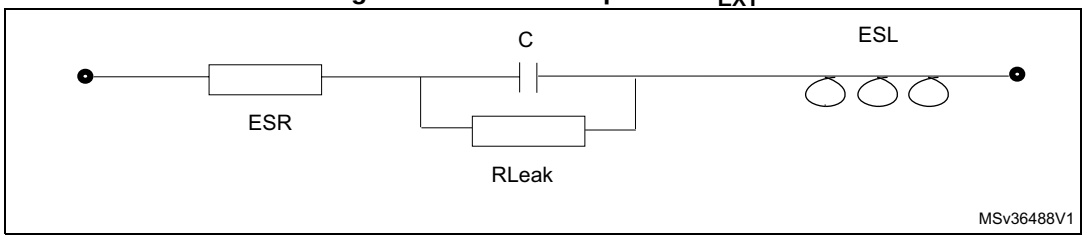
**Table 8. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5050 to 0x00 5059 | Reserved area (10 byte) | | | |
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH _FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH _NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH _IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5060 to 0x00 5061 | Reserved area (2 byte) | | | |
| 0x00 5062 | Flash | FLASH _PUKR | Flash program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH _DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 byte) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 byte) | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX(1) |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 byte) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |

### 10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor $C_{EXT}$ to the $V_{CAP}$ pin. $C_{EXT}$ is specified in *Table 18*. Care should be taken to limit the series inductance to less than 15 nH.

**Figure 12. External capacitor $C_{EXT}$**




1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

### 10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 10: Pin input voltage*.

#### Total current consumption in run mode

**Table 20. Total current consumption with code execution in run mode at $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(RUN)}$ | Supply current in Run mode, code executed from RAM | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 3.2 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 2.6 | 3.2 | |
| | | | HSI RC osc. (16 MHz) | 2.5 | 3.2 | |
| | | $f_{CPU} = f_{MASTER}$ /128 = 125 kHz | HSE user ext. clock (16 MHz) | 1.6 | 2.2 | |
| | | | HSI RC osc. (16 MHz) | 1.3 | 2.0 | |
| | | $f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.75 | - | |
| | | $f_{CPU} = f_{MASTER}$ = 128 kHz | LSI RC osc. (128 kHz) | 0.55 | - | |
| $I_{DD(RUN)}$ | Supply current in Run mode, code executed from Flash | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 7.7 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 7.0 | 8.0 | |
| | | | HSI RC osc. (16 MHz) | 7.0 | 8.0 | |
| | | $f_{CPU} = f_{MASTER}$ = 2 MHz | HSI RC osc. (16 MHz/8)(2) | 1.5 | - | |
| | | $f_{CPU} = f_{MASTER}$ /128 = 125 kHz | HSI RC osc. (16 MHz) | 1.35 | 2.0 | |
| | | $f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.75 | - | |
| | | $f_{CPU} = f_{MASTER}$ = 128 kHz | LSI RC osc. (128 kHz) | 0.6 | - | |

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

## 10.3.6 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 37. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | $V_{DD}$ = 5 V | -0.3 V | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage | | 0.7 x $V_{DD}$ | - | $V_{DD}$ + 0.3 V | |
| $V_{hys}$ | Hysteresis(1) | | - | 700 | - | mV |
| $R_{pu}$ | Pull-up resistor | $V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$ | 30 | 55 | 80 | kΩ |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 35(2) | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125(2) | |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 20 pF | - | - | 20(2) | ns |
| | | Standard and high sink I/Os Load = 20 pF | - | - | 50(2) | |
| $I_{lkg}$ | Digital input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1(3) | µA |
| $I_{lkg\ ana}$ | Analog input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±250(3) | nA |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O | Injection current ±4 mA | - | - | ±1(3) | µA |

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Data based on characterization results, not tested in production

**Figure 33. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (standard ports)**

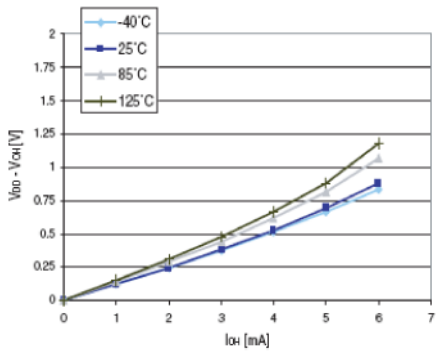



**Figure 34. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (standard ports)**

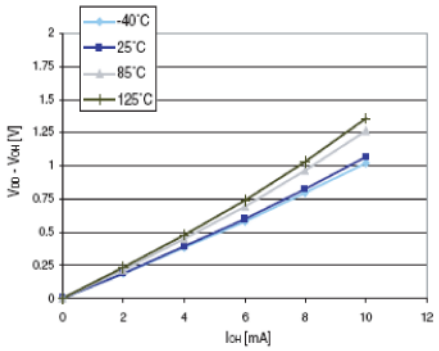



**Figure 35. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

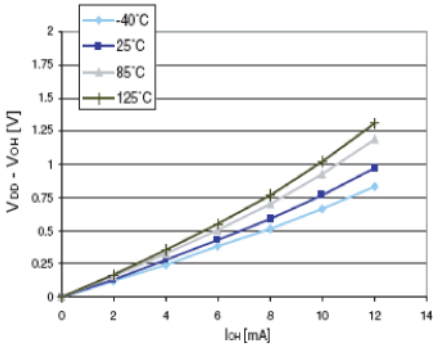
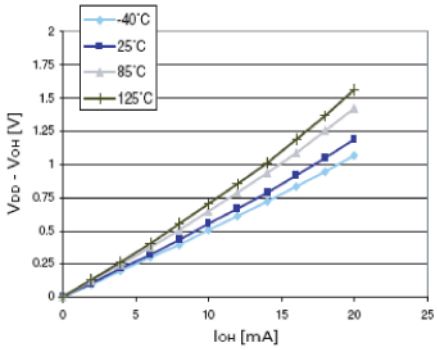



**Figure 36. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (high sink ports)**



### 10.3.8 Reset pin characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 41. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage(1) | - | -0.3 | - | 0.3 x $V_{DD}$ | V |
| $V_{IH(NRST)}$ | NRST input high level voltage(1) | $I_{OL}$= 2 mA | 0.7 x $V_{DD}$ | - | $V_{DD}$+ 0.3 | |
| $V_{OL(NRST)}$ | NRST output low level voltage(1) | $I_{OL}$= 3 mA | - | - | 0.5 | |
| $R_{PU(NRST)}$ | NRST pull-up resistor(2) | - | 30 | 55 | 80 | kΩ |
| $t_{IFP(NRST)}$ | NRST input filtered pulse(3) | - | - | - | 75 | ns |
| $t_{INFP(NRST)}$ | NRST Input not filtered pulse(3) | - | 500 | - | - | |
| $t_{OP(NRST)}$ | NRST output pulse(3) | - | 20 | - | - | µs |

1. Data based on characterization results, not tested in production.
2. The $R_{PU}$ pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

**Figure 37. Typical NRST $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ 4 temperatures**

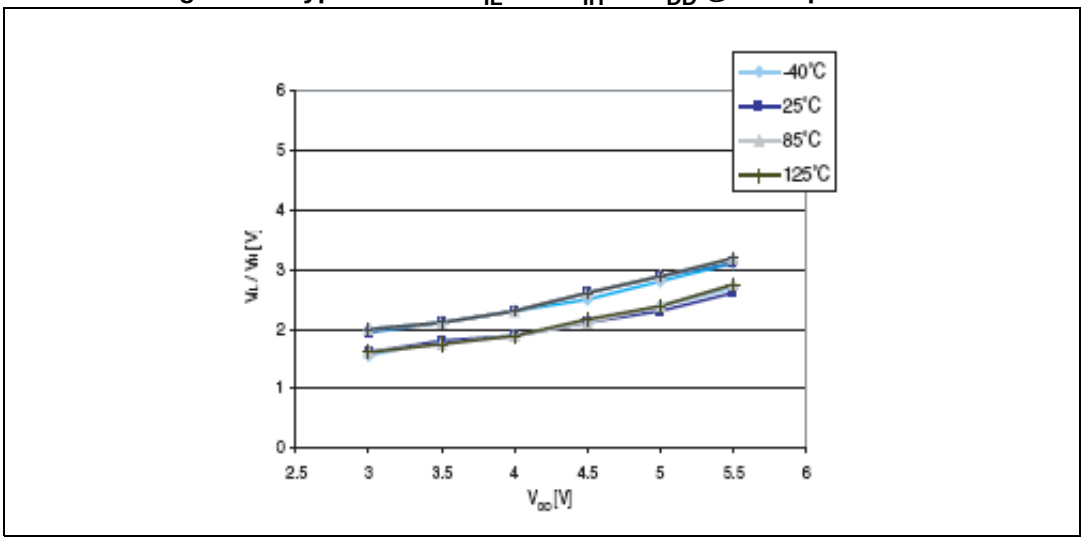
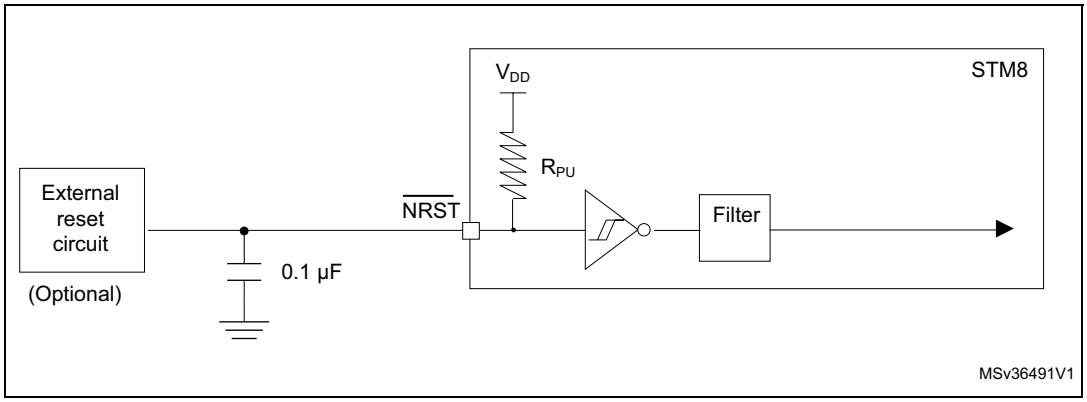


**Figure 40. Recommended reset pin protection**




### 10.3.9 SPI serial peripheral interface

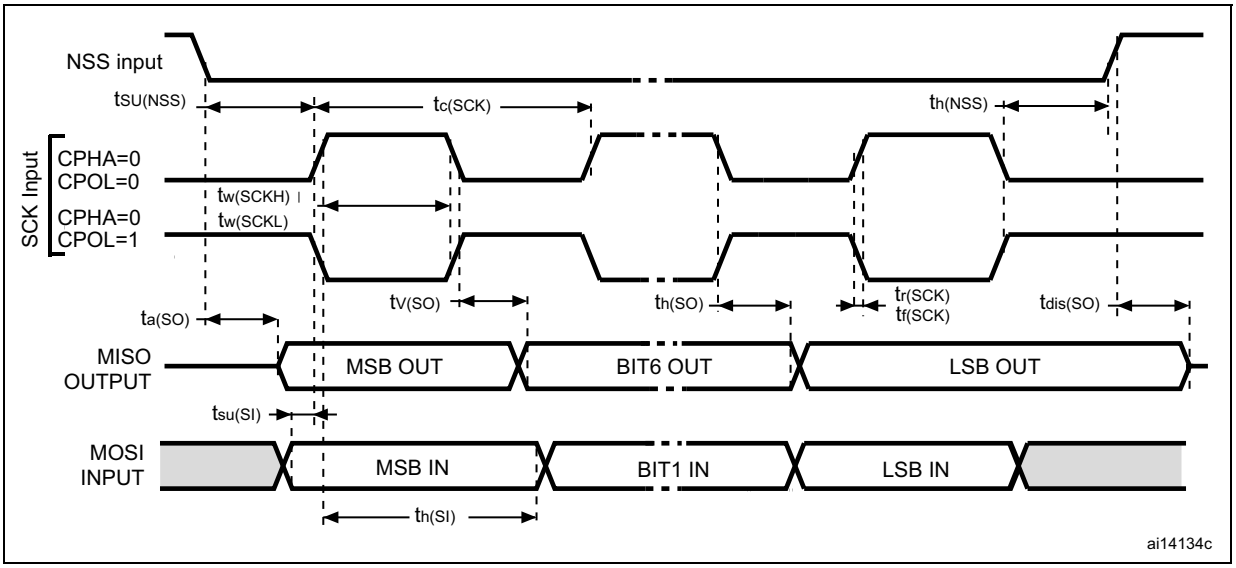
Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 42. SPI characteristics**

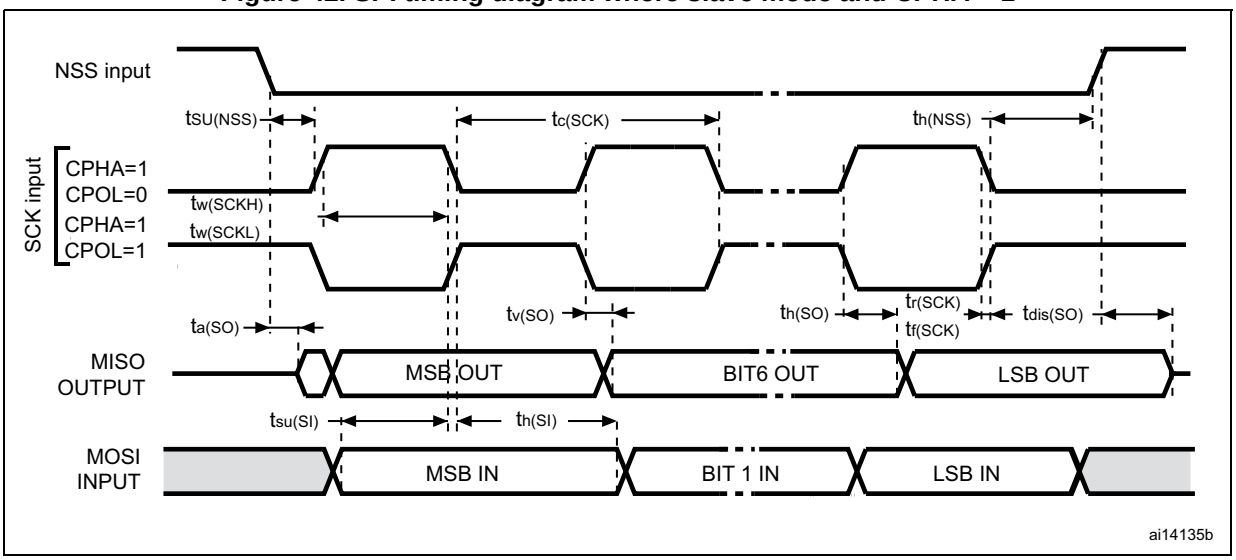
| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 6 | |

**Figure 41. SPI timing diagram where slave mode and CPHA = 0**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 42. SPI timing diagram where slave mode and CPHA = 1**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

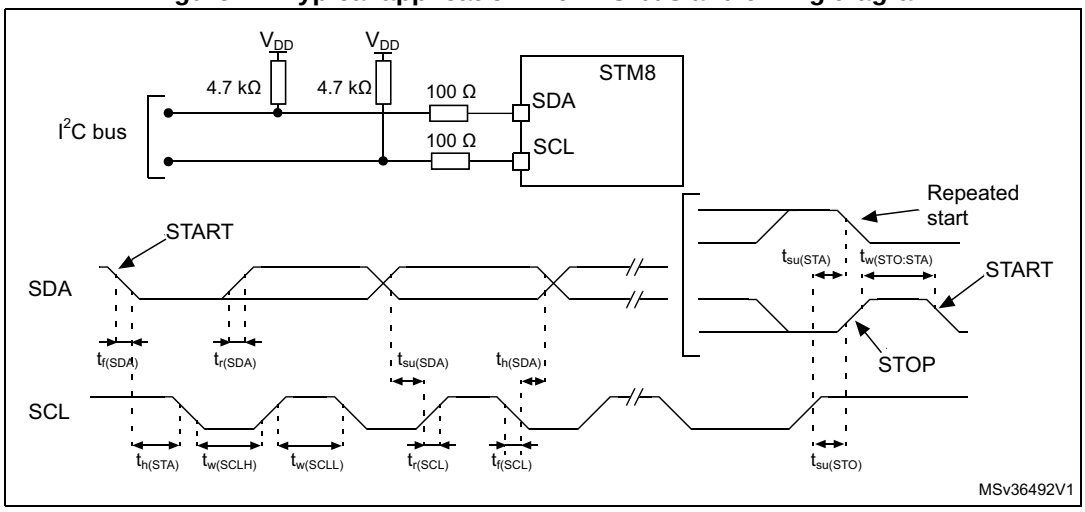
### 10.3.10 I²C interface characteristics

**Table 43. I²C characteristics**

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max(2) | Min(2) | Max(2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | - | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time ($V_{DD}$ = 3 to 5.5 V) | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time ($V_{DD}$ = 3 to 5.5 V) | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{MASTER}$, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

**Figure 44. Typical application with I²C bus and timing diagram**



### Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 50. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A = 25$ °C | A |
| | | $T_A = 85$ °C | |
| | | $T_A = 125$ °C | |

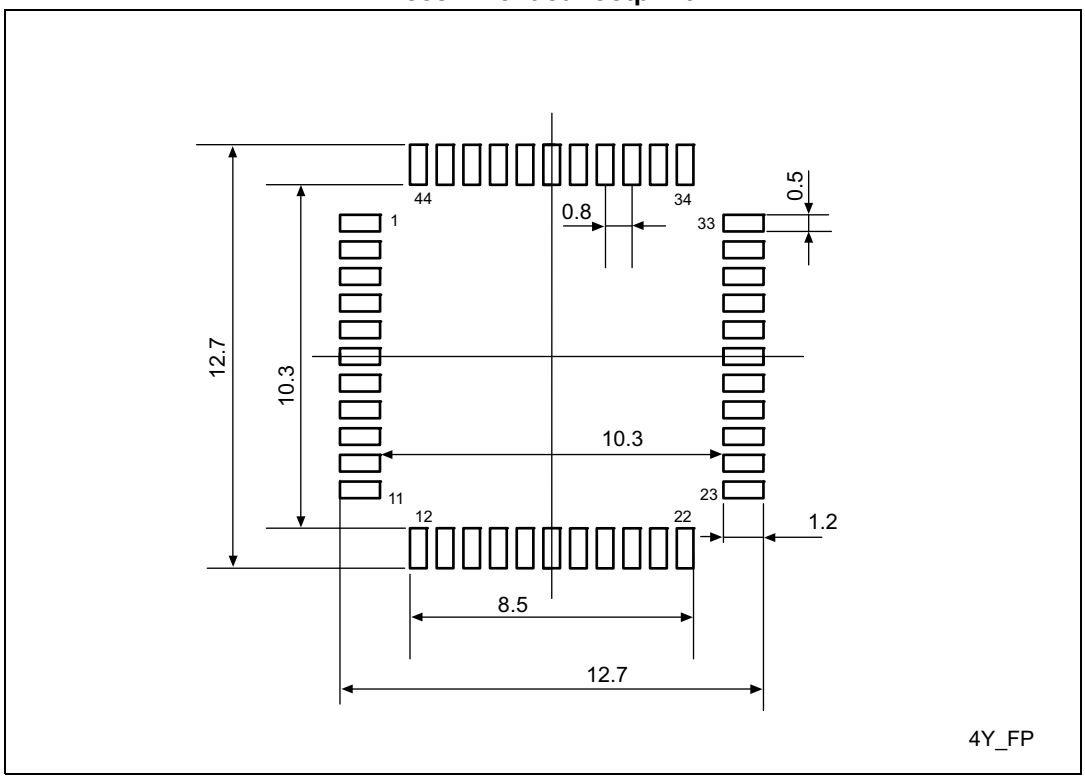
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

**Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 51. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

### Padding value for unused program memory (check only one option)

| | |
|---|---|
| [ ] 0xFF | Fixed value |
| [ ] 0x83 | TRAP instruction code |
| [ ] 0x75 | Illegal opcode (causes a reset when executed) |

### OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

### OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

| | |
|---|---|
| UBC, bit0 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit1 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit2 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit3 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit4 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit5 | [ ] 0: Reset<br>[ ] 1: Set |

### OTP2 alternate function remapping

| | |
|---|---|
| AFR0<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description<br>[ ] 1: Port D3 alternate function = ADC_ETR |
| AFR1<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description<br>[ ] 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3 |
| AFR2<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description<br>[ ] 1: Port D0 alternate function = CLK_CCO<br>*Note: if both AFR2 and AFR3 are activated, AFR2 option has priority over AFR3.* |
| AFR3<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description<br>[ ] 1: Port D0 alternate function = TIM1_BKIN |

## 14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

### 14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

#### ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

#### ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

### 14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

#### C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

#### STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

# 15 Revision history

**Table 57. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jun-2018 | 1 | Initial release. |
| 23-Jun-2018 | 2 | Corrected the number of high sink outputs to 9 in I/Os in *Features*.<br>Updated part numbers in *STM8S105xx access line features*. |
| 12-Aug-2008 | 3 | Updated the part numbers in *STM8S105xx access line features*.<br>USART renamed UART1, LINUART renamed UART2.<br>Added *Table: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices.* |
| 17-Sep-2008 | 4 | Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM.<br>Updated STM8S103 pinout section<br>Added low and medium density Flash memory categories.<br>Added Note 1 in *Section: Current characteristics.*<br>Updated *Section: Option bytes.* |
| 05-Feb-2009 | 5 | Updated STM8S103 pinout.<br>Updated number of High Sink I/Os in the pinout section.<br>TSSOP20 pinout modified (PD4 moved to pin 1 etc.)<br>Added WFQFN20 package<br>Updated *Section: Option bytes.*<br>Added *Section: Memory and register map.* |
| 27-Feb-2009 | 6 | Removed STM8S103x products (separate STM8S103 datasheet created).<br>Updated *Section: Electrical characteristics.* |

**Table 57. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 07-Feb-2014 | 13 | UART2_CK mapped to correct pin (pin 24) in *Figure: LQFP 44-pin pinout.*<br>Reserved area updated in *Table: Option bytes.*<br>Package Information updated in *Table: 32-lead ultra thin fine pitch quad flat no-lead package mechanical data.* |
| 01-Jul-2015 | 14 | Added:<br>– *Figure 49: LQFP48 marking example (package top view)*,<br>– *Figure 52: LQFP44 marking example (package top view)*,<br>– *Figure 55: LQFP32 marking example (package top view)*,<br>– *Figure 58: UFQFPN32 marking example (package top view)*,<br>– *Figure 60: SDIP32 marking example (package top view)*.<br>Updated:<br>– *Figure 41: SPI timing diagram where slave mode and CPHA = 0*,<br>– the standard for EMI data in *Table 48: EMI data*. |
| 23-Sep-2015 | 15 | Added the footnotes related to *Figure 56: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*. |