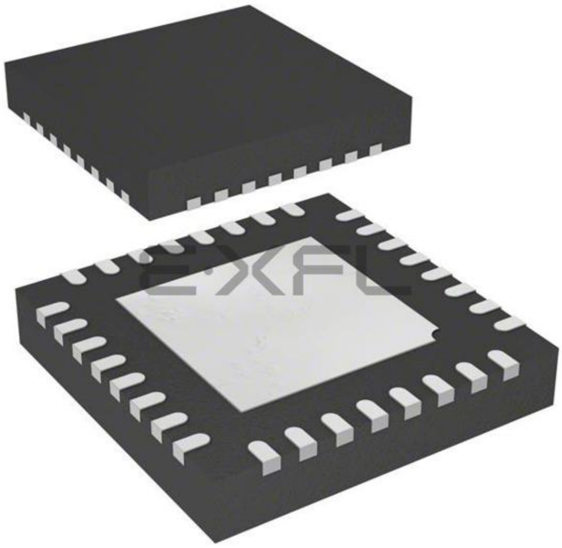


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k4u6a

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.1 master capability
- SPI: Full and half-duplex, 8 Mbit/s
- I^2C: Up to 400 kbit/s

4.14.1 UART2

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- LIN slave mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (fCPU/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

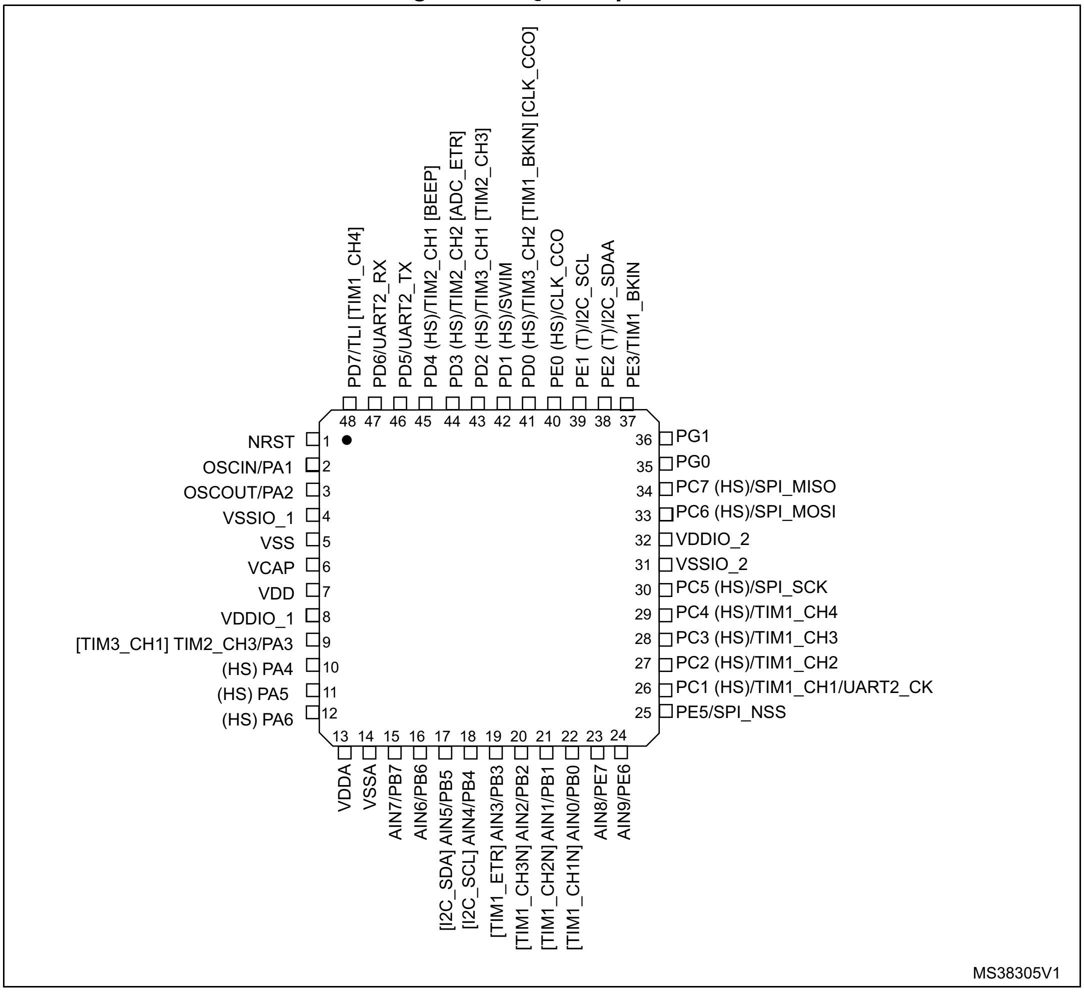
Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (fCPU/16)

LIN master mode

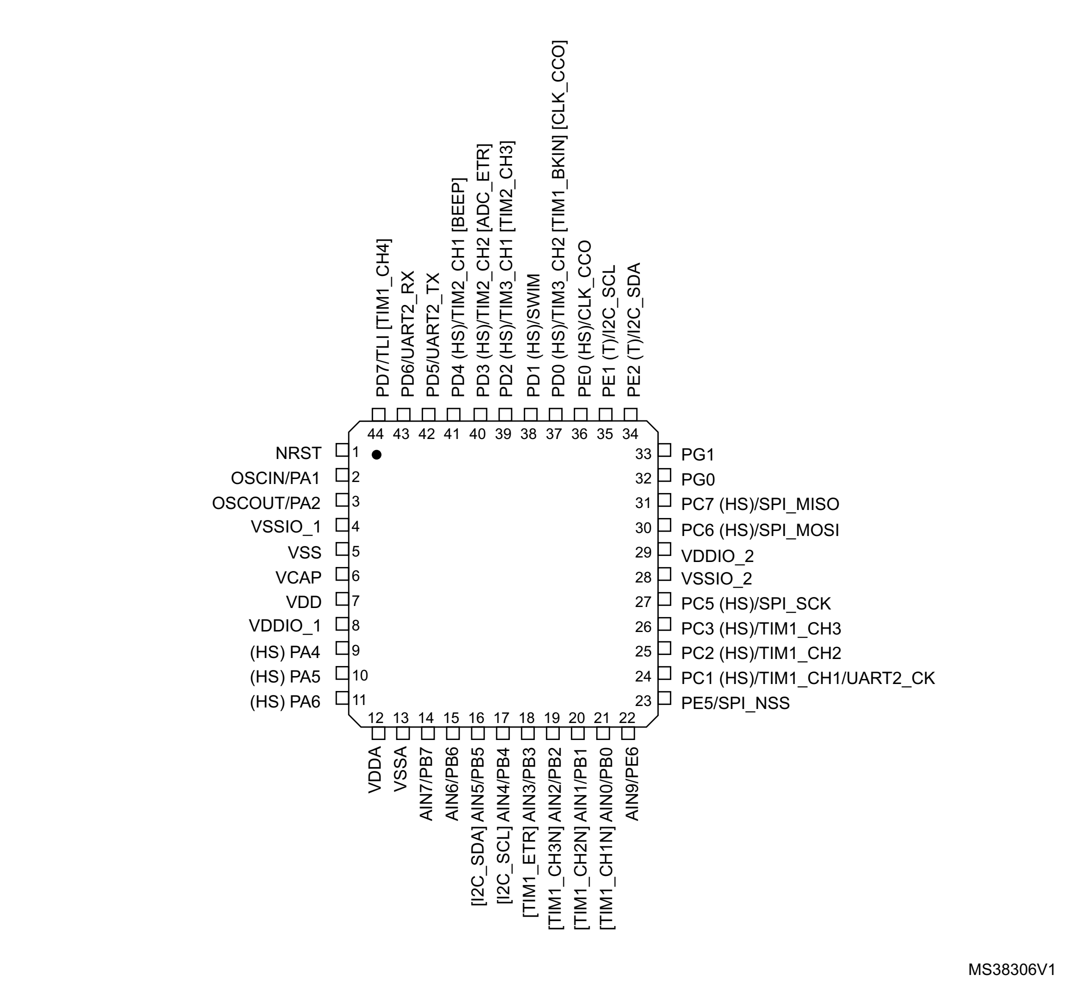
- Emission: Generates 13-bit synch. break frame
- Reception: Detects 11-bit break frame

Figure 3. LQFP48 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4. LQFP44 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

6.2.2 General hardware register map

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX[(1)]
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX[(2)]
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF

9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x48CD	X co-ordinate on the wafer	U_ID[7:0]							
0x48CE		U_ID[15:8]							
0x48CF	Y co-ordinate on the wafer	U_ID[23:16]							
0x48D0		U_ID[31:24]							
0x48D1	Wafer number	U_ID[39:32]							
0x48D2	Lot number	U_ID[47:40]							
0x48D3		U_ID[55:48]							
0x48D4		U_ID[63:56]							
0x48D5		U_ID[71:64]							
0x48D6		U_ID[79:72]							
0x48D7		U_ID[87:80]							
0x48D8		U_ID[95:88]							

3. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the VDDIO/VSSIO pins.
4. $I_{INJ(PIN)}$ must never be exceeded. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.
5. Negative injection disturbs the analog performance of the device. See note in *Section: TIM2, TIM3 - 16-bit general purpose timers.*
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	150	

10.3 Operating conditions

The device must be used in operating conditions that respect the parameters described in the table below. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}/V_{DDIO}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85 °C for suffix 6 or T_A= 125° C for suffix 3	44- and 48-pin devices, with output on eight standard ports, two high sink ports and two open drain ports simultaneously(4)	-	443	mW
		32-pin package, with output on eight standard ports and two high sink ports simultaneously(4)	-	360	

Table 19. Operating conditions at power-up/power-down (continued)

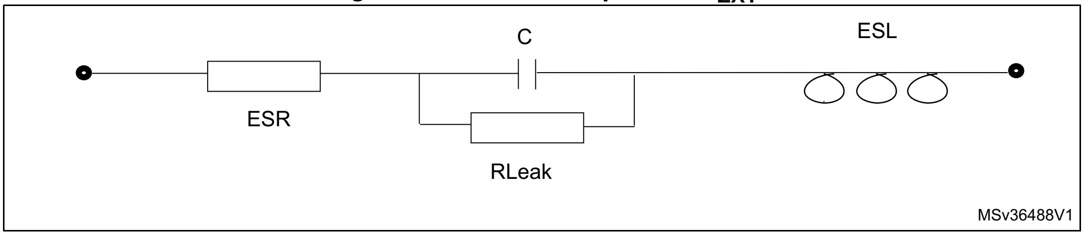
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.65	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 18*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 10: Pin input voltage*.

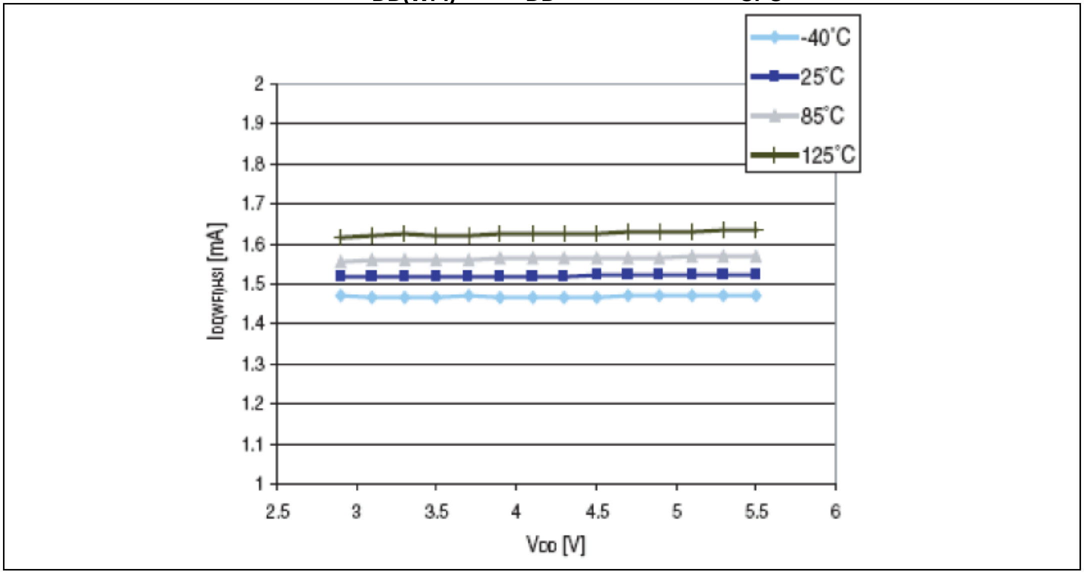
Total current consumption in run mode

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.2	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	7.7	-	mA
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc. (16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Figure 18. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



10.3.11 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 44. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD}= 2.95 to 5.5 V	1	-	4	MHz
		V_{DD}= 4.5 to 5.5 V	1	-	6	
V_{DDA}	Analog supply	-	3.0	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5(1)	
V_{AIN}	Conversion voltage range(2)	-	V_{SSA}	-	V_{DDA}	V
		Devices with external V_{REF+}/V_{REF-}	V_{REF-}	-	V_{REF+}	
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(2)	Minimum sampling time	f_{ADC} = 4 MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz		3.5		µs
		f_{ADC} = 6 MHz		2.33		µs
		-		14		$1/f_{ADC}$

1. Data guaranteed by design, not tested in production.
2. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 45. ADC accuracy with R_{AIN}< 10 kΩ, V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max[(1)]	Unit
$\lvert E_T \rvert$	Total unadjusted error[(2)]	f_{ADC} = 2 MHz	1.0	2.5	LSB
		f_{ADC} = 4 MHz	1.4	3.0	
		f_{ADC} = 6 MHz	1.6	3.5	
$\lvert E_O \rvert$	Offset error[(2)]	f_{ADC} = 2 MHz	0.6	2.0	
		f_{ADC} = 4 MHz	1.1	2.5	
		f_{ADC} = 6 MHz	1.2	2.5	
$\lvert E_G \rvert$	Gain error[(2)]	f_{ADC} = 2 MHz	0.2	2.0	
		f_{ADC} = 4 MHz	0.6	2.5	
		f_{ADC} = 6 MHz	0.8	2.5	
$\lvert E_D \rvert$	Differential linearity error[(2)]	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.8	1.5	
$\lvert E_L \rvert$	Integral linearity error[(2)]	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	
		f_{ADC} = 6 MHz	0.6	1.5	

1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max[(1)]	Unit
$\lvert E_T \rvert$	Total unadjusted error[(2)]	f_{ADC} = 2 MHz	1.1	2.0	LSB
		f_{ADC} = 4 MHz	1.6	2.5	
$\lvert E_O \rvert$	Offset error[(2)]	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	1.3	2.0	
$\lvert E_G \rvert$	Gain error[(2)]	f_{ADC} = 2 MHz	0.2	1.5	
		f_{ADC} = 4 MHz	0.5	2.0	
$\lvert E_D \rvert$	Differential linearity error[(2)]	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.0	
$\lvert E_L \rvert$	Integral linearity error[(2)]	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	

1. Data based on characterization results, not tested in production.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

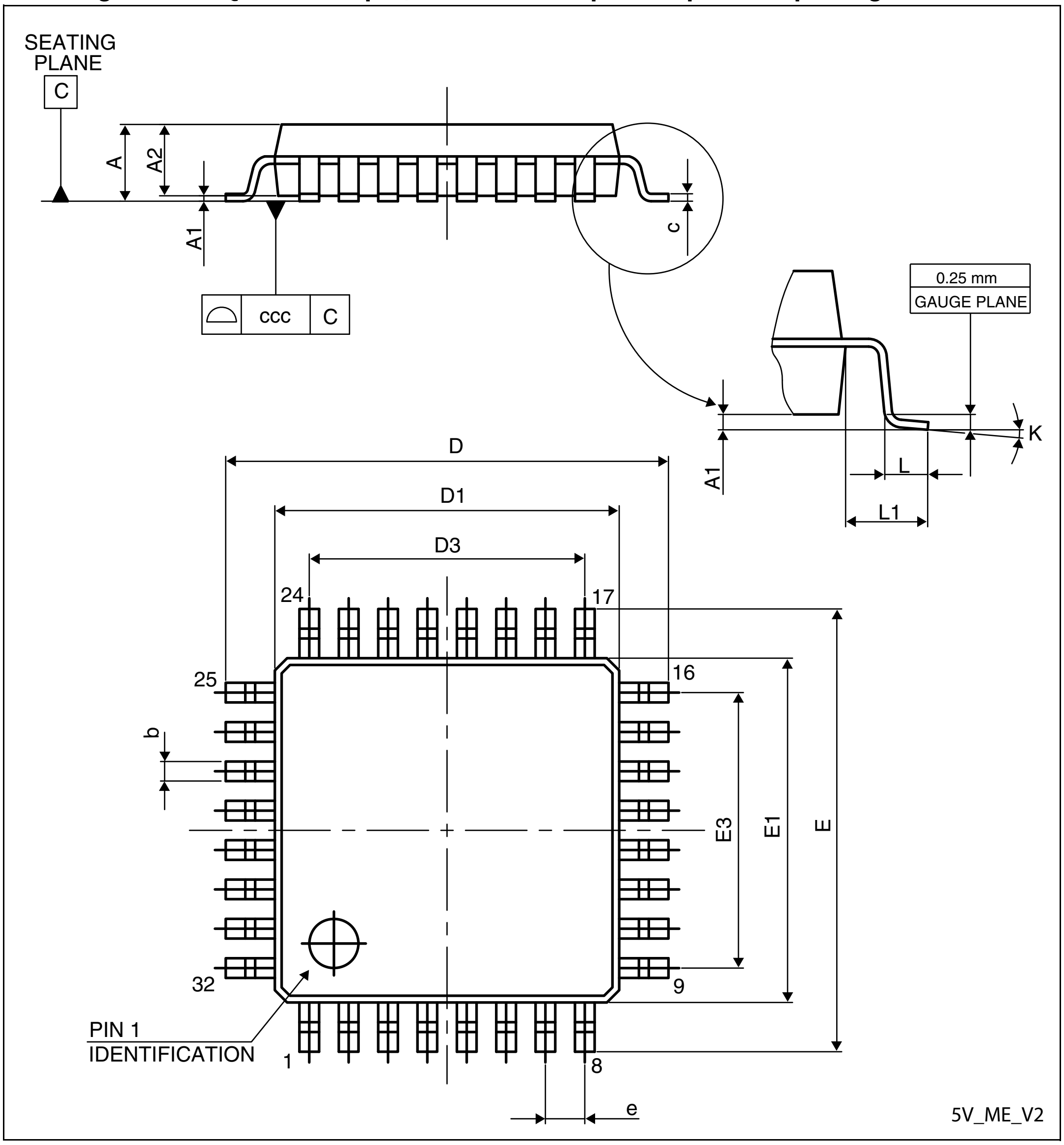
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A(1)

11.3 LQFP32 package information

Figure 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 18: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 56. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7x7 mm		°C/W
	Thermal resistance junction-ambient LQFP44 - 10x10 mm		
	Thermal resistance junction-ambient LQFP32 - 7x7 mm		
	Thermal resistance junction-ambient UFQFPN32 - 5x5 mm		
	Thermal resistance junction-ambient SDIP32 - 400 ml		

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

13.1 STM8S105 FASTROM microcontroller option list

(last update: September 2010)

Customer	....
Address	....
Contact	....
Phone number	....
FASTROM code reference(1)	....

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .Hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation.

Device type/memory size/package (check only one option)

FASTROM device	16 Kbyte	32 Kbyte
LQFP32	[ ] STM8S105K4	[ ] STM8S105K6
LQFP44	[ ] STM8S105S4	[ ] STM8S105S6
LQFP48	[ ] STM8S105C4	[ ] STM8S105C6

Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

LQFP32: 2 lines of 7 characters max: "_ _ _ _ _ _ _" and "_ _ _ _ _ _ _"
LQFP44: 2 lines of 7 characters max: "_ _ _ _ _ _ _" and "_ _ _ _ _ _ _"
LQFP48: 2 lines of 8 characters max: "_ _ _ _ _ _ _ _" and "_ _ _ _ _ _ _ _"

Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

15 Revision history

Table 57. Document revision history

Date	Revision	Changes
05-Jun-2018	1	Initial release.
23-Jun-2018	2	Corrected the number of high sink outputs to 9 in I/Os in *Features*. Updated part numbers in *STM8S105xx access line features*.
12-Aug-2008	3	Updated the part numbers in *STM8S105xx access line features*. USART renamed UART1, LINUART renamed UART2. Added *Table: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices.*
17-Sep-2008	4	Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM. Updated STM8S103 pinout section Added low and medium density Flash memory categories. Added Note 1 in *Section: Current characteristics.* Updated *Section: Option bytes.*
05-Feb-2009	5	Updated STM8S103 pinout. Updated number of High Sink I/Os in the pinout section. TSSOP20 pinout modified (PD4 moved to pin 1 etc.) Added WFQFN20 package Updated *Section: Option bytes.* Added *Section: Memory and register map.*
27-Feb-2009	6	Removed STM8S103x products (separate STM8S103 datasheet created). Updated *Section: Electrical characteristics.*