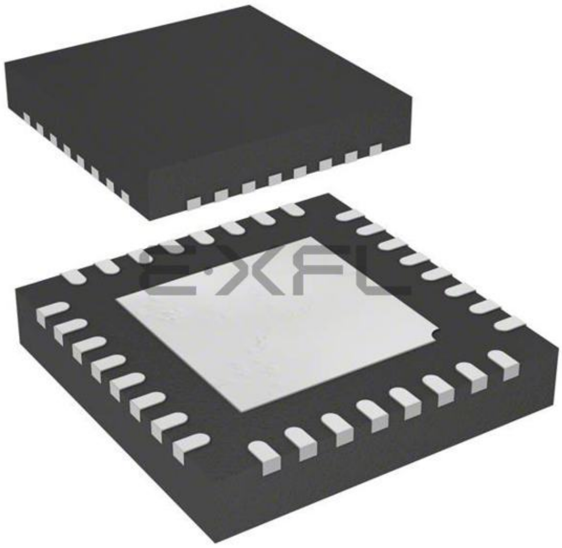

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k4u6atr

Table 1. STM8S105x4/6 access line features

Device	STM8S105C6	STM8S105C4	STM8S105S6	STM8S105S4	STM8S105K6	STM8S105K4
Pin count	48	48	44	44	32	32
Maximum number of GPIOs	38	38	34	34	25	25
Ext. Interrupt pins	35	35	31	31	23	23
Timer CAPCOM channels	9	9	8	8	8	8
Timer complementary outputs	3	3	3	3	3	3
A/D Converter channels	10	10	9	9	7	7
High sink I/Os	16	16	15	15	12	12
Medium density Flash Program memory (byte)	32K	16K	32K	16K	32K	16K
Data EEPROM (bytes)	1024	1024	1024	1024	1024	1024
RAM (bytes)	2K	2K	2K	2K	2K	2K
Peripheral set	Advanced control timer (TIM1), General-purpose timers (TIM2 and TIM3), Basic timer (TIM4) SPI, I2C, UART, Window WDG, Independent WDG, ADC					

4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

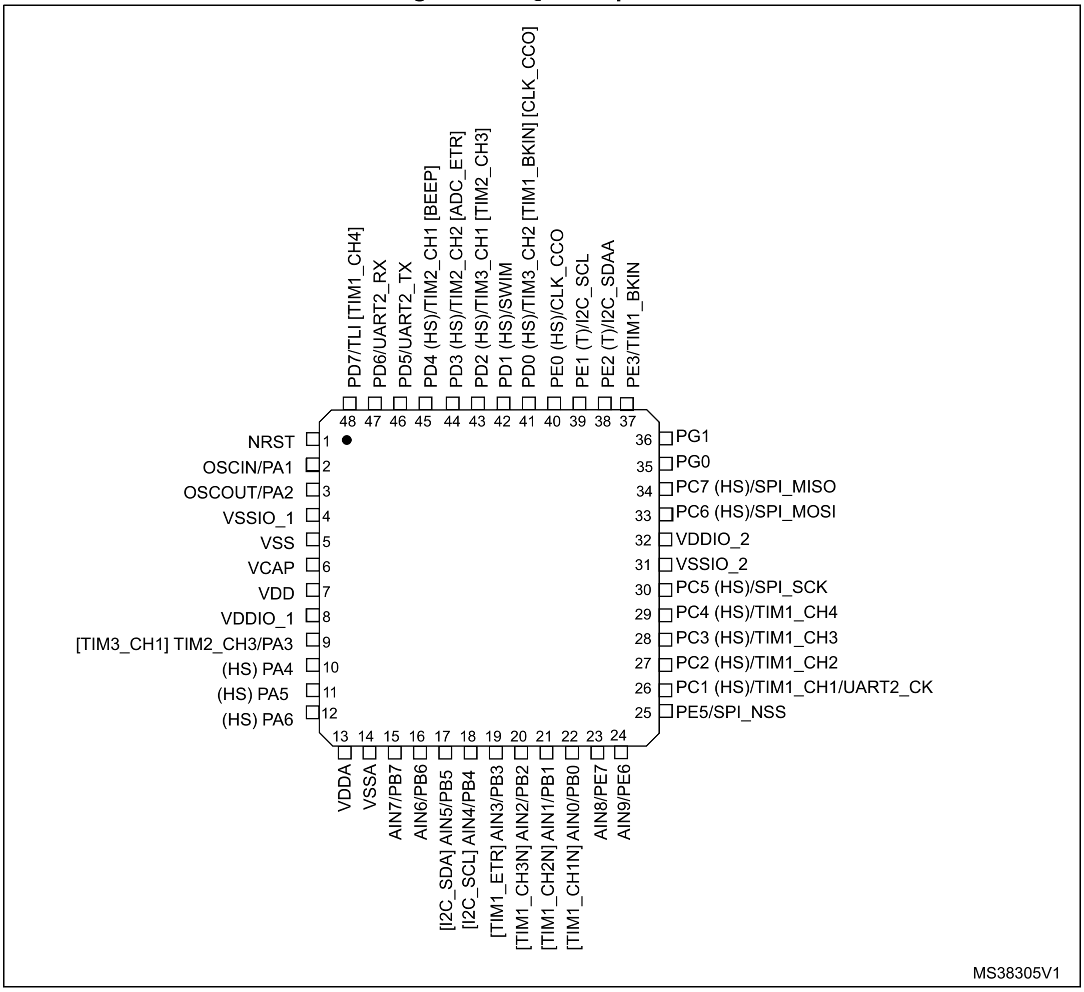
Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  – 1-16 MHz high-speed external crystal (HSE)
  – Up to 16 MHz high-speed user-external clock (HSE user-ext)
  – 16 MHz high-speed internal RC oscillator (HSI)
  – 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

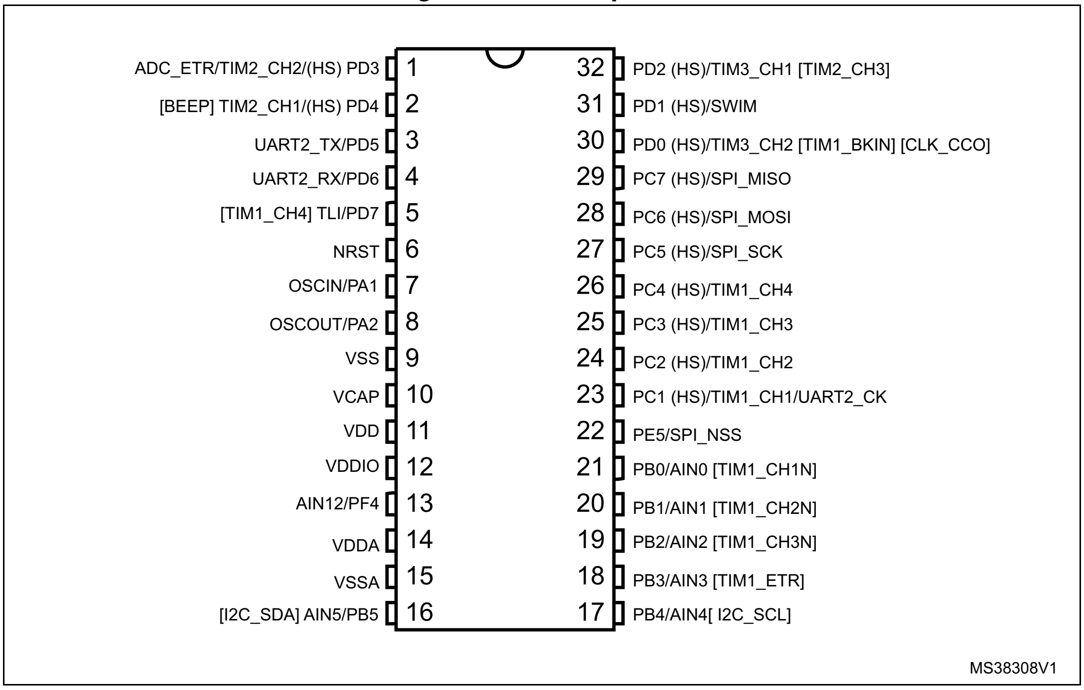
Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART2	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

Figure 3. LQFP48 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 6. SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	6	NRST	I/O	-	X	-	-		-	-	Reset		-
2	2	2	7	PA1/ OSC IN	I/O	X	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
3	3	3	8	PA2/ OSC OUT	I/O	X	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
4	4	-	-	VSSIO_1	S	-	-	-	-	-	-	-	I/O ground		-
5	5	4	9	VSS	S	-	-	-	-	-	-	-	Digital ground		-
6	6	5	10	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-

Table 7. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX(1)
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX(1)
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX(1)
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

1. Depends on the external circuitry.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 Interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare reg. 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 byte)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC_DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			

Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
20	UART2	Tx complete	-	-	0x00 8058
21	UART2	Receive register DATA FULL	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

Table 11. Option byte (continued)

Addr.	Option name	Option byte no.	Option bits 7	6	5	4	3	2	1	0	Factory default setting
0x487E	Bootloader	OPTBL	BL[7:0]								0x00
0x487F		NOPTBL	NBL[7:0]								0xFF

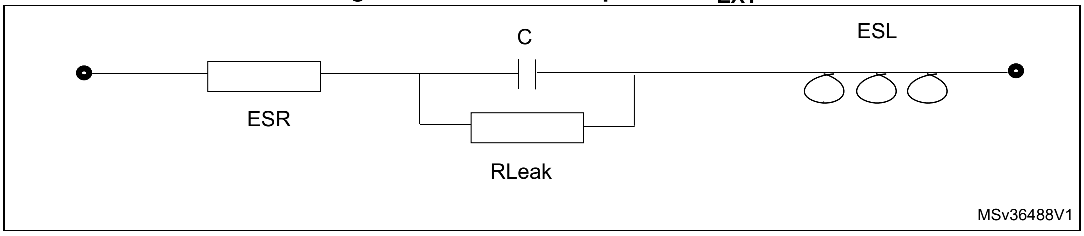
Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03: Page 0 to 4 defined as UBC, memory write-protected ... 0x3E: Pages 0 to 63 defined as UBC, memory write-protected Other values: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following table for the description of the alternate function remapping description of bits [7:2].
OPT3	**HSITRIM:** High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 18*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 10: Pin input voltage*.

Total current consumption in run mode

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.2	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	7.7	-	mA
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc. (16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Low power mode wakeup times

Table 28. Wakeup times

Symbol	Parameter	Conditions			Typ	Max[(1)]	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode[(2)]	0 to 16 MHz			-	See note[(3)]	μs
$t_{WU(WFI)}$	Wakeup time from run mode[(2)]	$f_{CPU}= f_{MASTER}=$ 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode[(2)]	MVR voltage regulator on[(4)]	Flash in operating mode[(5)]	HSI (after wakeup)	1[(6)]	2[(6)]	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode[(2)]	MVR voltage regulator off[(4)]	Flash in operating mode[(5)]	HSI (after wakeup)	3[(6)]	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode[(2)]	MVR voltage regulator off[(4)]	Flash in operating mode[(5)]	HSI (after wakeup)	48[(6)]	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode[(2)]	MVR voltage regulator off[(4)]	Flash in power-down mode[(5)]	HSI (after wakeup)	50[(6)]	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode[(2)]	Flash in operating mode[(5)]			52	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode[(2)]	Flash in power-down mode[(5)]			54	-	

1. Data based on characterization results, not tested in production.
2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 29. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max[(1)]	Unit
$I_{DD(R)}$	Supply current in reset state[(2)]	V_{DD} = 5 V	500	-	μA
		V_{DD} = 3.3 V	400	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	μs

1. Data guaranteed by design, not tested in production.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

10.3.3 External clock sources and timing characteristics

HSE user external clock

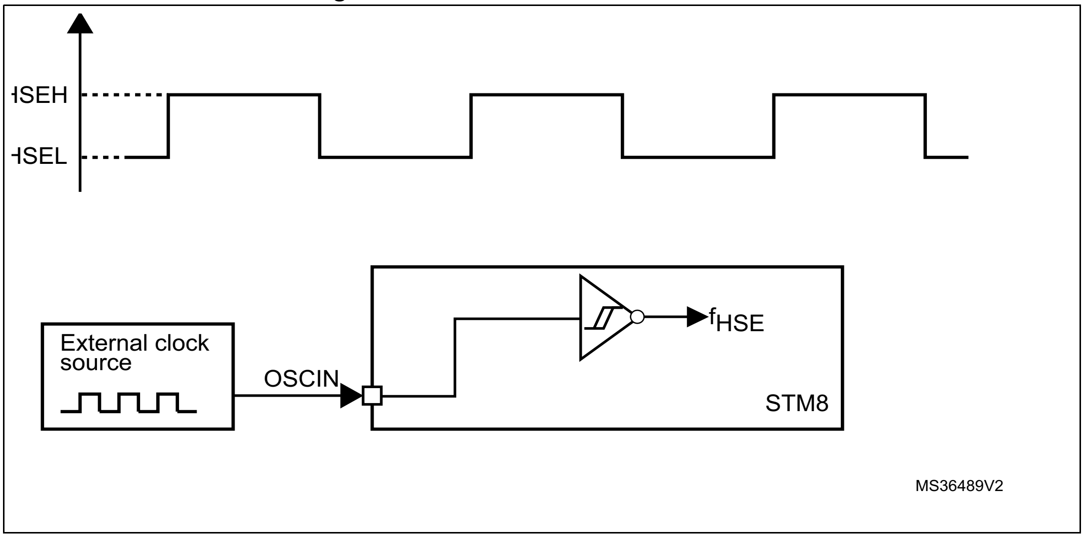
Subject to general operating conditions for V_{DD} and T_A.

Table 31. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Data based on characterization results, not tested in production.

Figure 19. HSE external clock source



10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 20 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250(3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Data based on characterization results, not tested in production

Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

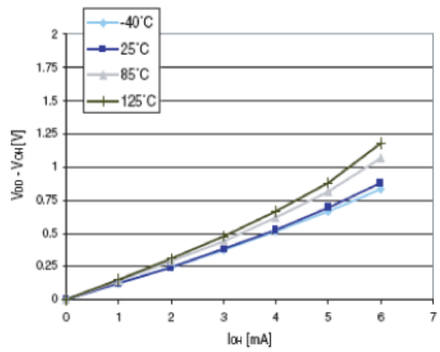


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

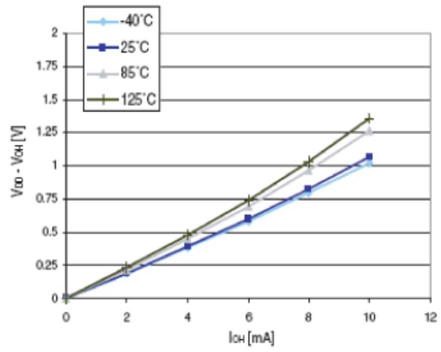


Figure 35. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

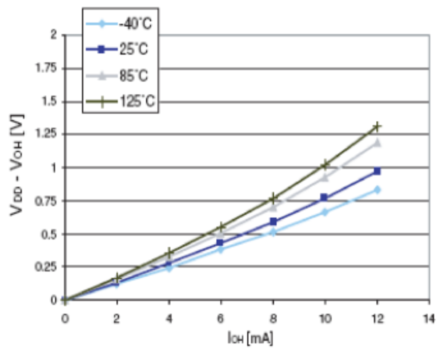
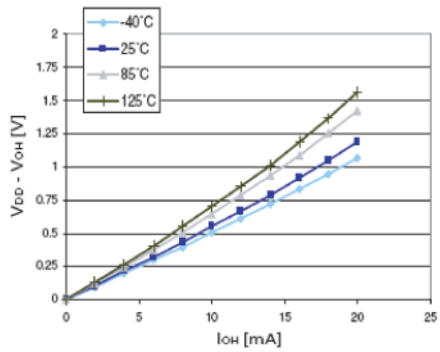


Figure 36. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



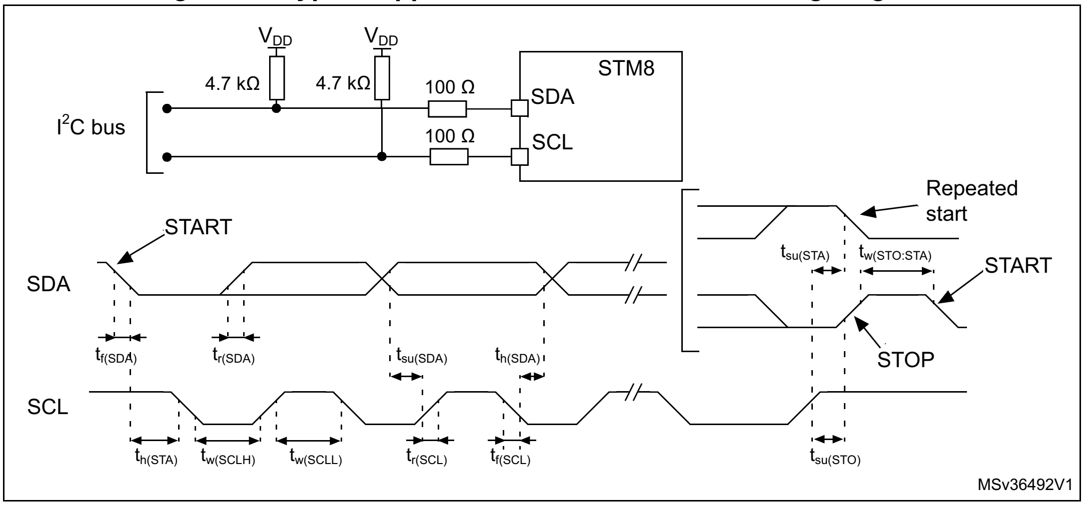
10.3.10 I²C interface characteristics

Table 43. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	μs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	ns
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 44. Typical application with I²C bus and timing diagram



10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A(1)

13 Ordering information

Figure 61. STM8S105x4/6 access line ordering information scheme(1)

Example: STM8 S 105 K 4 T 6 TR

Product class
STM8 microcontroller

Family type
S = Standard

Sub-family type
10x = Access line
105 sub-family

Pin count
K = 32 pins
S = 44 pins
C = 48 pins

Program memory size
4 = 16 Kbyte
6 = 32 Kbyte

Package type
B = SDIP
T = LQFP
U = UFQFPN

Temperature range
3 = -40 to 125 °C
6 = -40 to 85 °C

Package pitch/thickness
Blank = 0.5 mm
C = 0.8 mm
A = 0.55 mm thickness for UFQFPN32

Packing
No character = Tray or tube
TR = Tape and reel

1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

AFR4 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D7 alternate function = TIM1_CH4
AFR5 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N.
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port B5 alternate function = I2C_SDA, port B4 alternate function = I2C_SCL
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D4 alternate function = BEEP.

OPT3 watchdog

WWDG_HALT (check only one option)	[ ] 0: No reset generated on halt if WWDG active[[ ] 1: Reset generated on halt if WWDG active
WWDG_HW (check only one option)	[ ] 0: WWDG activated by software [ ] 1: WWDG activated by hardware
IWDG_HW (check only one option)	[ ] 0: IWDG activated by software [ ] 1: IWDG activated by hardware
LSI_EN (check only one option)	[ ] 0: LSI clock is not available as CPU clock source [ ] 1: LSI clock is available as CPU clock source
HSITRIM (check only one option)	[ ] 0: 3-bit trimming supported in CLK_HSITRIMR register [ ] 1: 4-bit trimming supported in CLK_HSITRIMR register

OPT4 watchdog

PRSC (check only one option)	[ ] for 16 MHz to 128 kHz prescaler [ ] for 8 MHz to 128 kHz prescaler [ ] for 4 MHz to 128 kHz prescaler
CKAWUSEL (check only one option)	[ ] LSI clock source selected for AWU [ ] HSE clock with prescaler selected as clock source for AWU
EXTCLK (check only one option)	[ ] External crystal connected to OSCIN/OSCOUT [ ] External signal on OSCIN

14 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

14.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

14.1.1 STice key features

- Occurrence and time profiling and code coverage (new features),
- Advanced breakpoints with up to 4 levels of conditions,
- Data breakpoints,
- Program and data trace recording up to 128 KB records,
- Read/write on the fly of memory during emulation,
- In-circuit debugging/programming via SWIM protocol,
- 8-bit probe analyzer,
- 1 input and 2 output triggers,
- Power supply follower managing application voltages between 1.62 to 5.5 V,
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

15 Revision history

Table 57. Document revision history

Date	Revision	Changes
05-Jun-2018	1	Initial release.
23-Jun-2018	2	Corrected the number of high sink outputs to 9 in I/Os in *Features*. Updated part numbers in *STM8S105xx access line features*.
12-Aug-2008	3	Updated the part numbers in *STM8S105xx access line features*. USART renamed UART1, LINUART renamed UART2. Added *Table: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices.*
17-Sep-2008	4	Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM. Updated STM8S103 pinout section Added low and medium density Flash memory categories. Added Note 1 in *Section: Current characteristics.* Updated *Section: Option bytes.*
05-Feb-2009	5	Updated STM8S103 pinout. Updated number of High Sink I/Os in the pinout section. TSSOP20 pinout modified (PD4 moved to pin 1 etc.) Added WFQFN20 package Updated *Section: Option bytes.* Added *Section: Memory and register map.*
27-Feb-2009	6	Removed STM8S103x products (separate STM8S103 datasheet created). Updated *Section: Electrical characteristics.*

Table 57. Document revision history (continued)

Date	Revision	Changes
12-May-2009	7	Added SDIP32 silhouette and package to *Features* and *Section: SDIP32 package mechanical data*; updated *Section: Pinout and pin description*. Updated VDD range (2.95 V to 5.5 V) on Features. Amended name of package VQFPN32. Added Table 5 on page 22. Updated *Section: Auto wakeup counter.* Updated pins 25, 30, and 31 in *Section: Pinout and pin description*. Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Added *Table: Description of alternate function remapping bits [7:0] of OPT2.* *Section: Electrical characteristics:* Updated VCAP specifications; updated Table 15, Table 18, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 29, Table 35, and Table 42; added current consumption curves; removed Figure 20: typical HSE frequency vs fcpu @ 4 temperatures; updated Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17; modified HSI accuracy in Table 33 ; added Figure 44; modified $f_{SCK,}$ $t_{V(SO)}$ and $t_{V(MO)}$ in Table 42; updated figures and tables of High speed internal RC oscillator (HSI); replaced Figure 23, Figure 24, Figure 26, and Figure 39. *Section Package information:* updated *Section: Thermal characteristics* and removed Table 57: Junction temperature range. Updated *Section: STM8S105xx access line ordering information scheme.*
10-Jun-2009	8	Document status changed from “preliminary data” to “datasheet”. Standardized the name of the VFQFPN package. Removed ‘wpu’ from I2C pins Section: Pinout and pin description