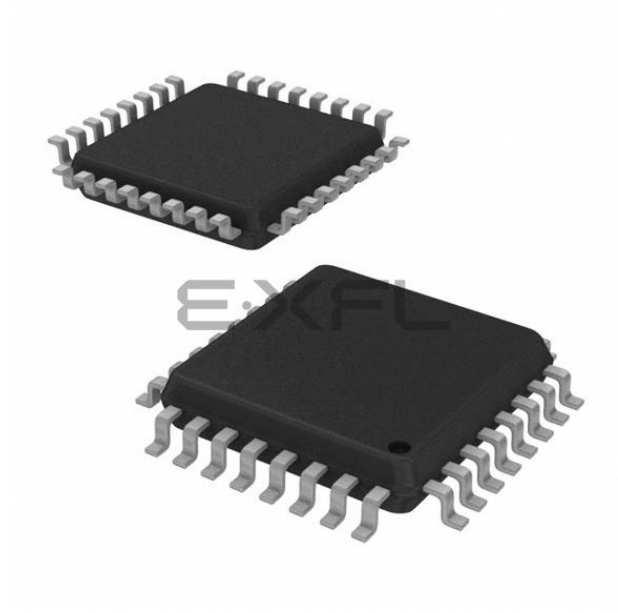

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k6t3ctr

Contents

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

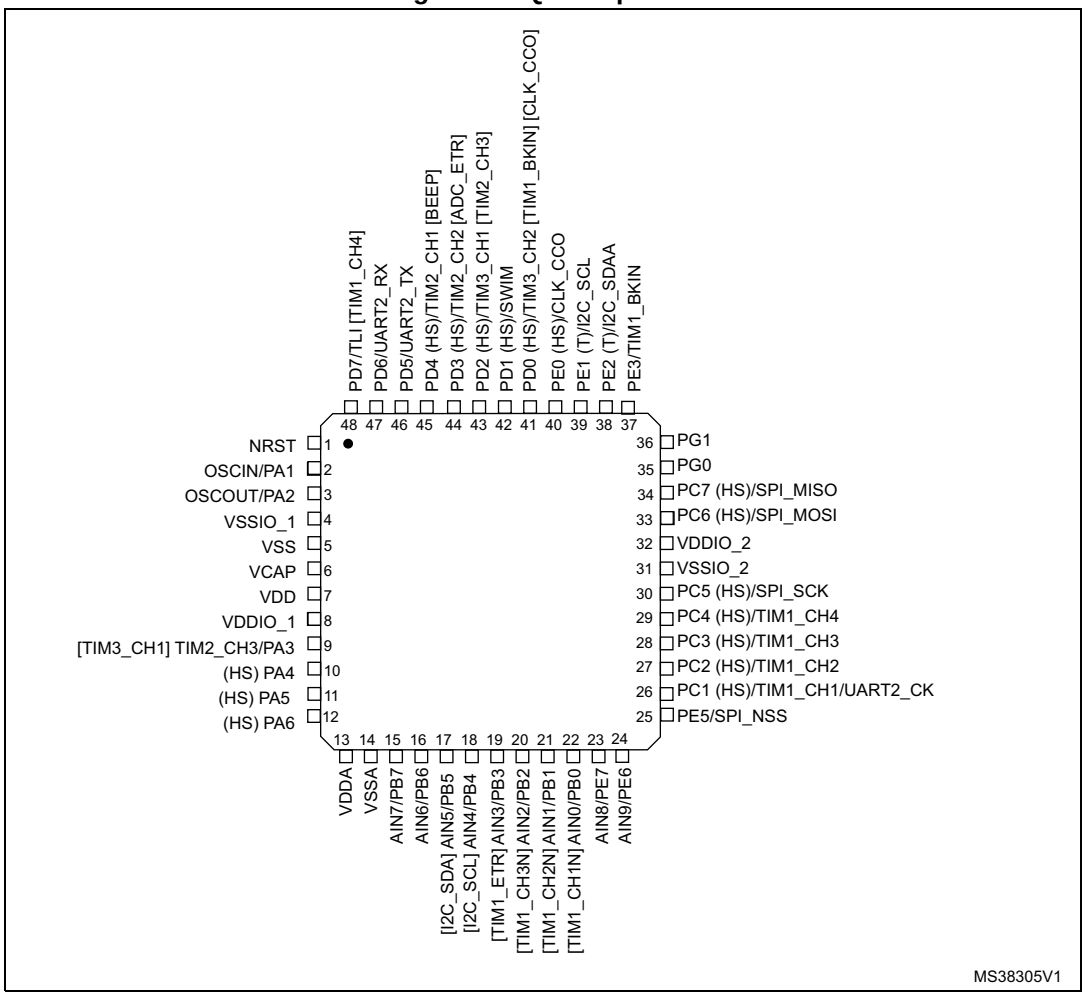
This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

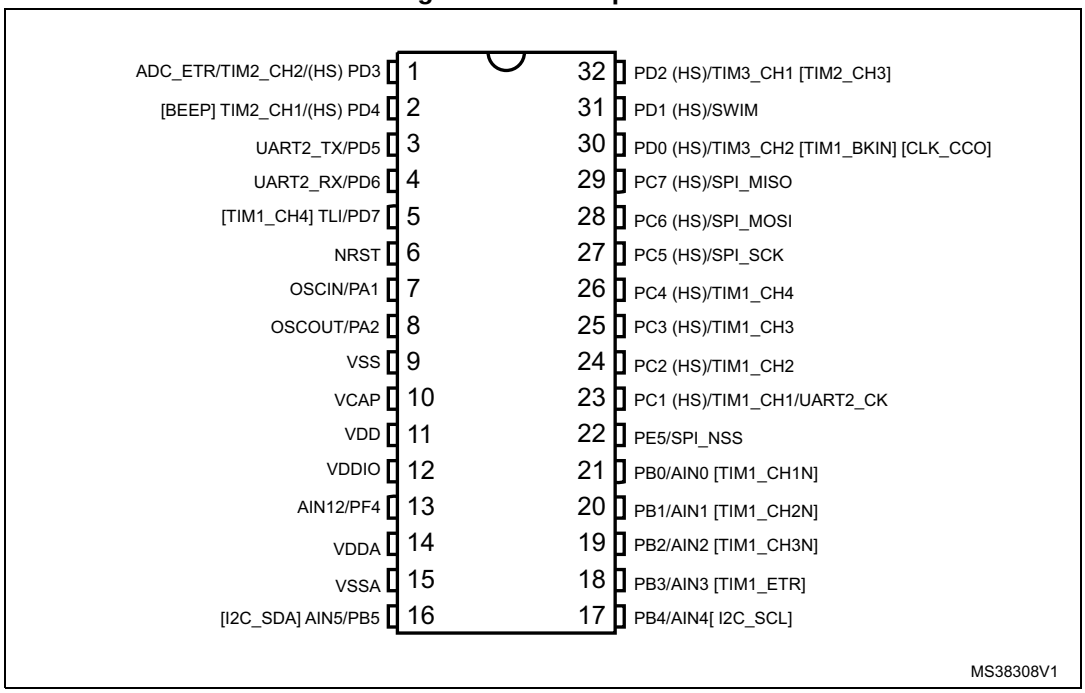
- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Figure 3. LQFP48 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 6. SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	6	NRST	I/O	-	**X**	-	-		-	-	Reset		-
2	2	2	7	PA1/ OSC IN	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
3	3	3	8	PA2/ OSC OUT	I/O	**X**	X	-	-	O1	X	X	Port A1	Resonator/ crystal in	
4	4	-	-	VSSIO_1	S	-	-	-	-	-	-	-	I/O ground		-
5	5	4	9	VSS	S	-	-	-	-	-	-	-	Digital ground		-
6	6	5	10	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

Table 6. Flash, data EEPROM and RAM boundary address

Memory area	Size (byte)	Start address	End address
Flash program memory	32 K	0x00 8000	0x00 FFFF
	16 K	0x00 8000	0x00 BFFF
RAM	2 K	0x00 0000	0x00 07FF
Data EEPROM	1024	0x00 4000	0x00 43FF

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only.

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved	-	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM2	TIM2 update/ overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/ compare	-	-	0x00 8040
15	TIM3	TIM3 update/ overflow	-	-	0x00 8044
16	TIM3	TIM3 capture/ compare	-	-	0x00 8048
17	Reserved	-	-	-	0x00 804C
18	Reserved	-	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054

8.1 Alternate function remapping bits

Table 13. Alternate function remapping bits [7:0] of OPT2

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate functions.(2) 1: Port D4 alternate function = BEEP. **AFR6** Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port B5 alternate function = I2C_SDA; port B4 alternate function = I2C_SCL. **AFR5** Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port B3 alternate function = TIM1_ETR; port B2 alternate function = TIM1_NCC3; port B1 alternate function = TIM1_CH2N; port B0 alternate function = TIM1_CH1N. **AFR4** Alternate function remapping option 4 0: AFR4 remapping option inactive: Default alternate functions.(2) 1: Port D7 alternate function = TIM1_CH4. **AFR3** Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = TIM1_BKIN. **AFR2** Alternate function remapping option 2 0: AFR2 remapping option inactive: Default alternate functions.(2) 1: Port D0 alternate function = CLK_CCO. Note: AFR2 option has priority over AFR3 if both are activated. **AFR1** Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions.(2) 1: Port A3 alternate function = TIM3_CH1; port D2 alternate function TIM2_CH3 **AFR0** Alternate function remapping option 0 0: AFR0 remapping option inactive: Default alternate functions.(2) 1: Port D3 alternate function = ADC_ETR.

1. Do not use more than one remapping option in the same port.
2. Refer to STM8S105x4/6 pin descriptions.

3. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the VDDIO/VSSIO pins.
4. $I_{INJ(PIN)}$ must never be exceeded. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.
5. Negative injection disturbs the analog performance of the device. See note in *Section: TIM2, TIM3 - 16-bit general purpose timers.*
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	150	

10.3 Operating conditions

The device must be used in operating conditions that respect the parameters described in the table below. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}/V_{DDIO}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85 °C for suffix 6 or T_A= 125° C for suffix 3	44- and 48-pin devices, with output on eight standard ports, two high sink ports and two open drain ports simultaneously(4)	-	443	mW
		32-pin package, with output on eight standard ports and two high sink ports simultaneously(4)	-	360	

Table 19. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.65	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.

Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	680	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	320	400	
			Power down mode	HSE crystal osc. (16 MHz)	630	-	-	
			Power down mode	LSI RC osc. (128 kHz)	140	270	350	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	120	220	
			Power down mode	LSI RC osc. (128 kHz)	10	60	150	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 26. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	62	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	6.5	25	80	

1. Data based on characterization results, not tested in production.

Table 27. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	90	150	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	20	80	

1. Data based on characterization results, not tested in production.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 30. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	230	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	115	
$I_{DD(TIM3)}$	TIM3 supply current(1)	90	
$I_{DD(TIM4)}$	TIM4 supply current(1)	30	
$I_{DD(UART2)}$	UART2 supply current (2)	110	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	955	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

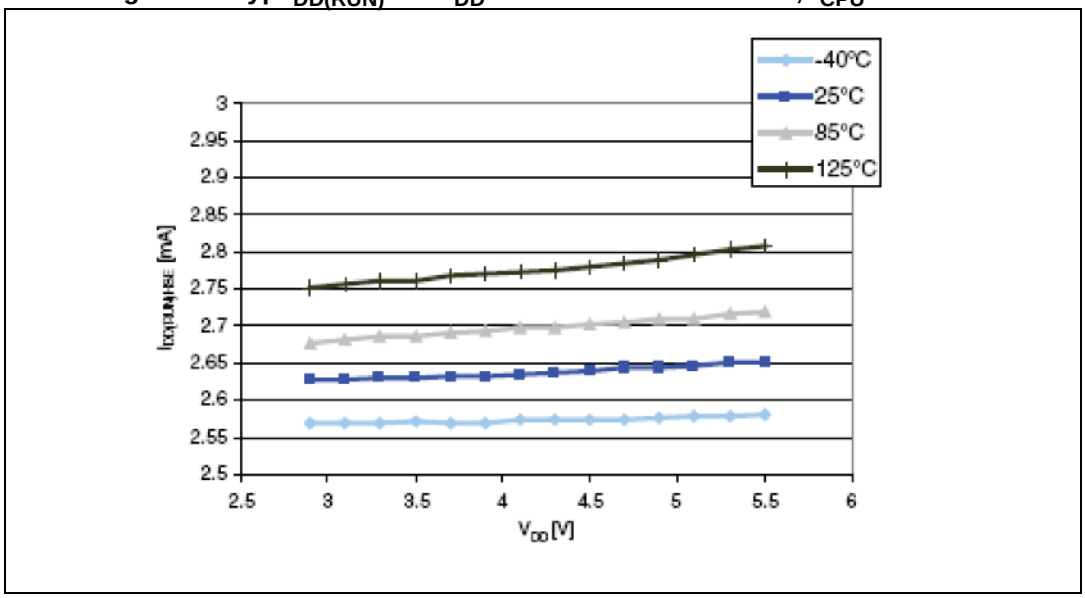
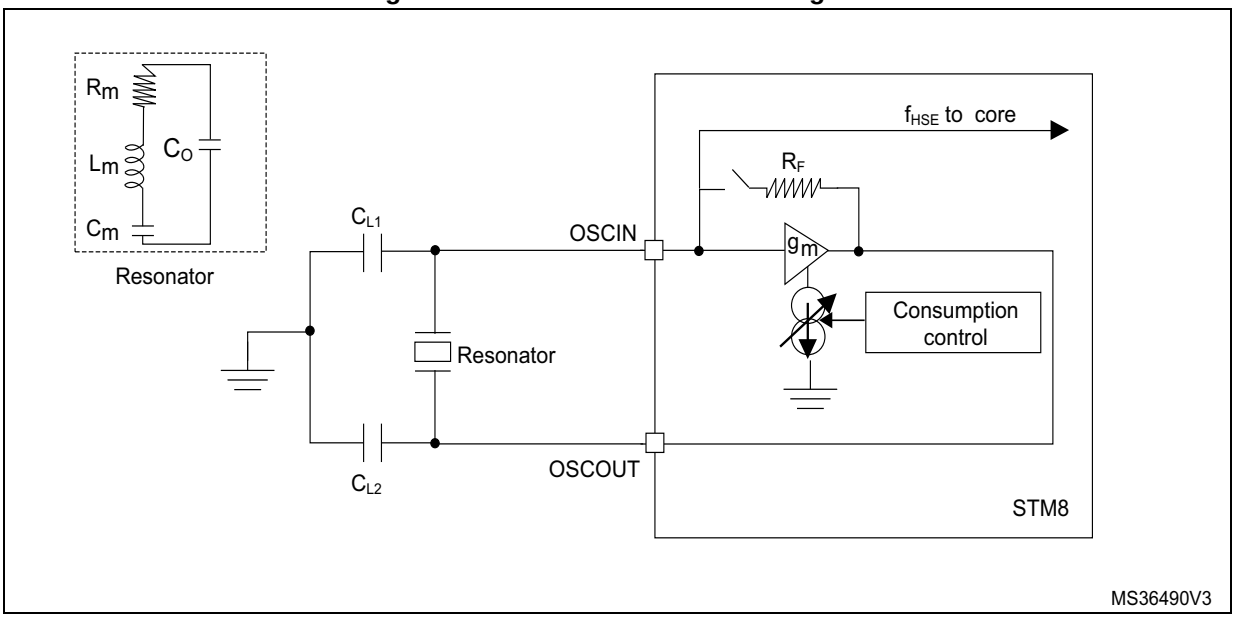


Figure 20. HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

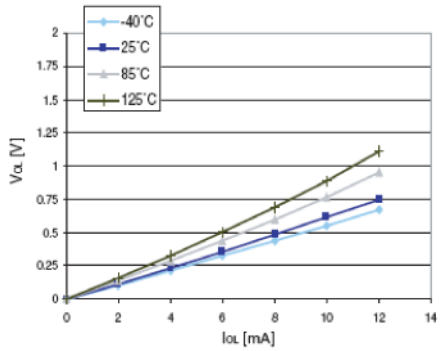


Figure 30. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

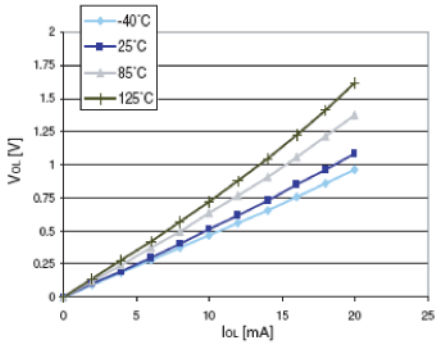


Figure 31. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

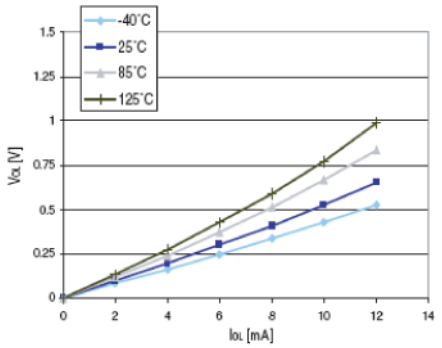


Figure 32. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

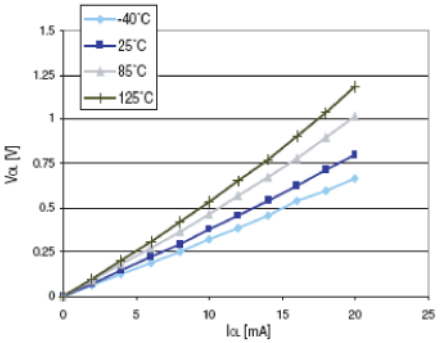


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

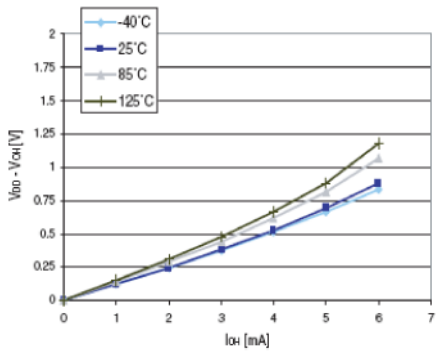


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

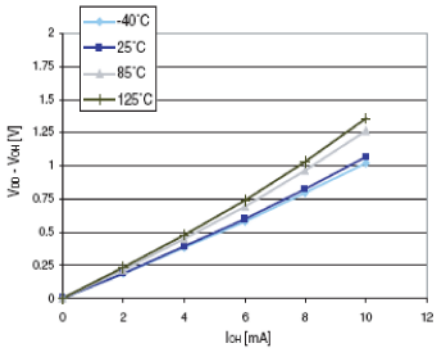


Figure 35. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

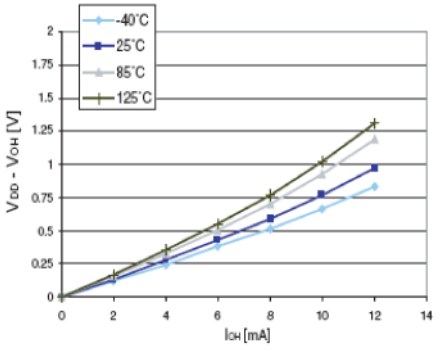
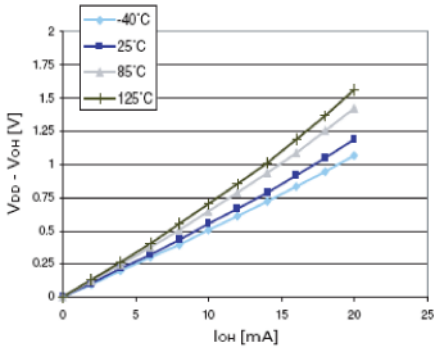


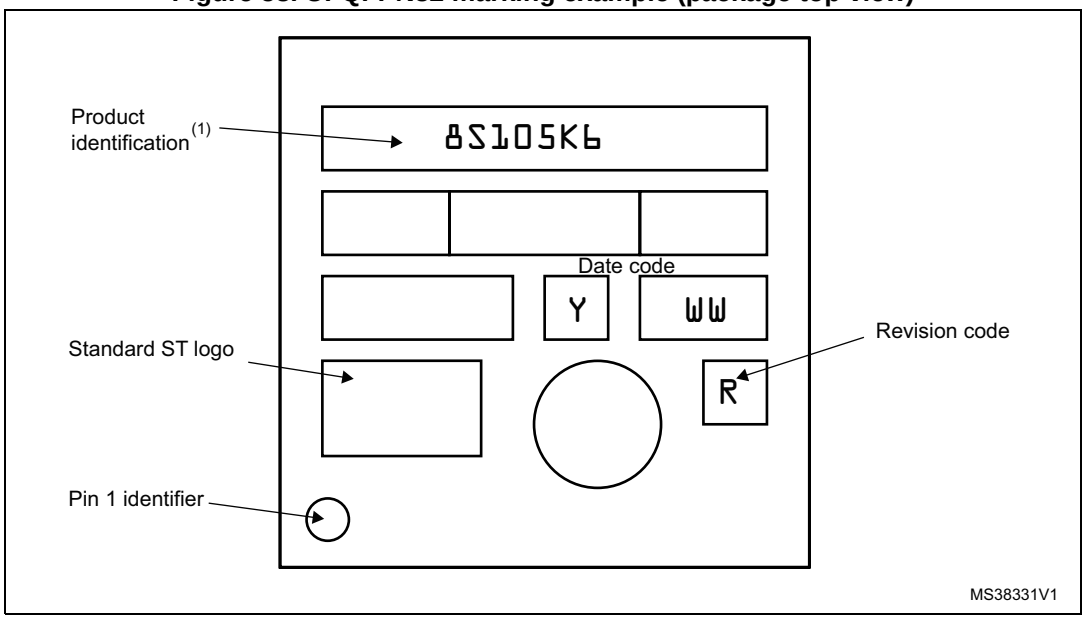
Figure 36. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 58. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.5 SDIP32 package information

Figure 59. SDIP32 package outline

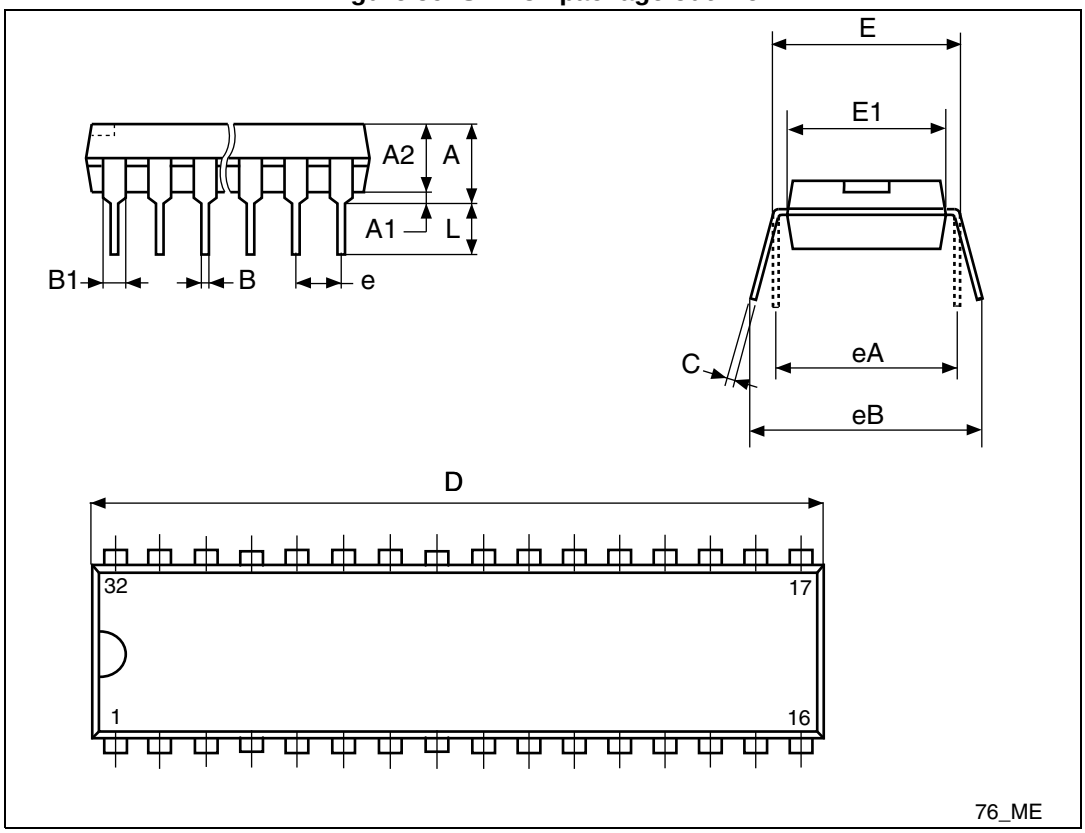


Table 55. SDIP32 package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

13.1 STM8S105 FASTROM microcontroller option list

(last update: September 2010)

Customer	.....
Address	.....
Contact	.....
Phone number	.....
FASTROM code reference(1)	.....

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .Hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation.

Device type/memory size/package (check only one option)

FASTROM device	16 Kbyte	32 Kbyte
LQFP32	[ ] STM8S105K4	[ ] STM8S105K6
LQFP44	[ ] STM8S105S4	[ ] STM8S105S6
LQFP48	[ ] STM8S105C4	[ ] STM8S105C6

Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

LQFP32: 2 lines of 7 characters max: “_ _ _ _ _ _ _” and “_ _ _ _ _ _ _”

LQFP44: 2 lines of 7 characters max: “_ _ _ _ _ _ _” and “_ _ _ _ _ _ _”

LQFP48: 2 lines of 8 characters max: “_ _ _ _ _ _ _ _” and “_ _ _ _ _ _ _ _”

Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C