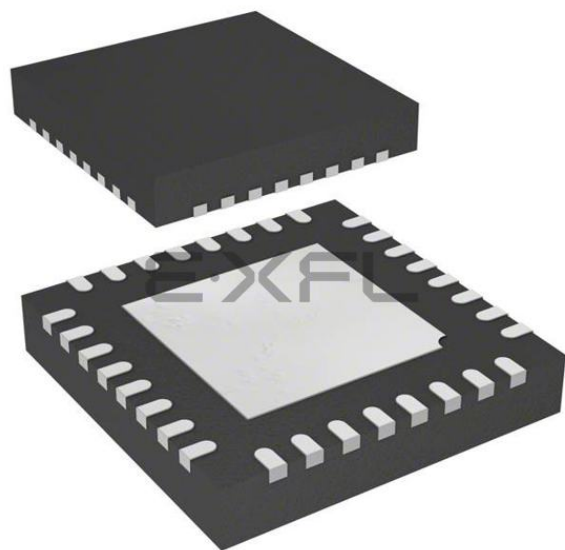




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Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105k6u6atr

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4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 μ s up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

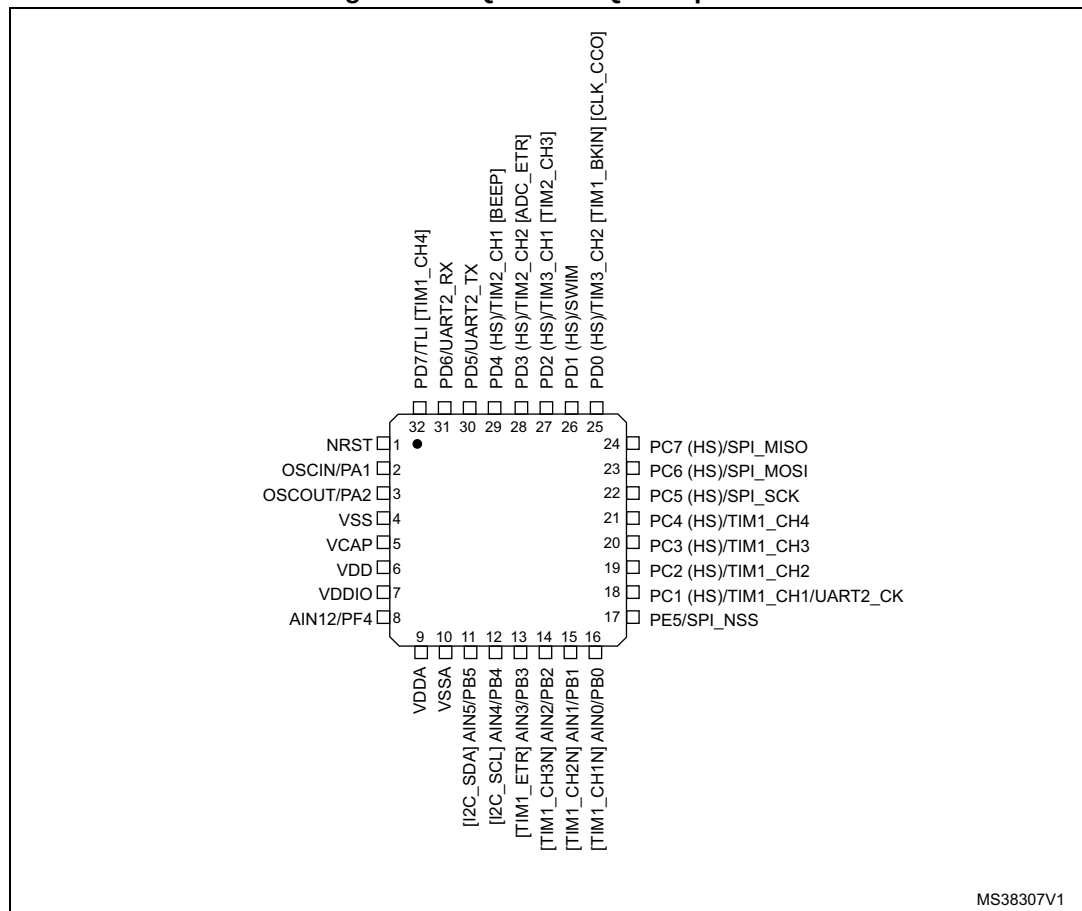
It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

5 Pinout and pin description

Table 4. Legend/abbreviations for pin description tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold X (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Figure 5. UFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	22	-	-	PE6/ AIN9	I/O	<u>X</u>	X	X	-	O1	X	X	Port E6	Analog input 9 ⁽³⁾	-
25	23	17	22	PE5/ SPI_NSS	I/O	<u>X</u>	X	X	-	O1	X	X	Port E5	SPI master/ slave select	-
26	24	18	23	PC1/ TIM1_CH1/ UART2_CK	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1/UART2 synchronous clock	-
27	25	19	24	PC2/ TIM1_CH2	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	-
28	26	20	25	PC3/ TIM1_CH3	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
29	-	21	26	PC4/ TIM1_CH4	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4	-
30	27	22	27	PC5/ SPI_SCK	I/O	<u>X</u>		X	HS	O3	X	X	Port C5	SPI clock	-
31	28	-	-	VSSIO_2	S	-	-	-	-	-	-	-	I/O ground		-
32	29	-	-	VDDIO_2	S	-	-	-	-	-	-	-	I/O power supply		-
33	30	23	28	PC6/ SPI_MOSI	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-
34	31	24	29	PC7/ SPI_MISO	I/O	<u>X</u>	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
35	32	-	-	PG0	I/O	<u>X</u>	X	-	-	O1	X	X	Port G0	-	-
36	33	-	-	PG1	I/O	<u>X</u>	X	-	-	O1	X	X	Port G1	-	-
37	-	-	-	PE3/ TIM1_BKIN	I/O	<u>X</u>	X	X	-	O1	X	X	Port E3	Timer 1 - break input	-
38	34	-	-	PE2/ I2C_SDA	I/O	<u>X</u>	-	X	-	O1	T ₍₄₎	-	Port E2	I2C data	-
39	35	-	-	PE1/ I2C_SCL	I/O	<u>X</u>	-	X	-	O1	T ₍₄₎	-	Port E1	I2C clock	-

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 Interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530C		TIM2_PSCR	IM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 byte)			

8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF
0x480B	Reserved	OPT6	Reserved								0x00
0x480C		NOPT6	Reserved								0xFF
0x480D	Reserved	OPT7	Reserved								0x00
0x480E		NOPT7	Reserved								0xFF
0x480F	Reserved	-	Reserved								-
0x48FD		-	Reserved								-

HSI internal RC/ $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$, $V_{DD} = 5 \text{ V}$

Table 30. Peripheral current consumption

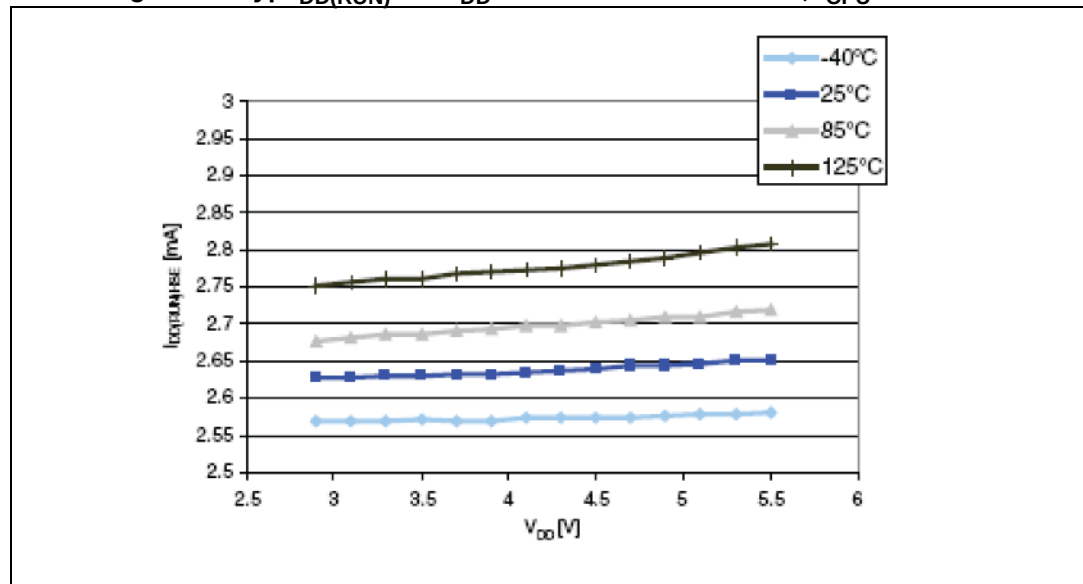
Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current ⁽¹⁾	230	μA
$I_{DD(TIM2)}$	TIM2 supply current ⁽¹⁾	115	
$I_{DD(TIM3)}$	TIM3 supply current ⁽¹⁾	90	
$I_{DD(TIM4)}$	TIM4 supply current ⁽¹⁾	30	
$I_{DD(UART2)}$	UART2 supply current ⁽²⁾	110	
$I_{DD(SPI)}$	SPI supply current ⁽²⁾	45	
$I_{DD(I2C)}$	I2C supply current ⁽²⁾	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting ⁽³⁾	955	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, $f_{CPU} = 16 \text{ MHz}$



10.3.3 External clock sources and timing characteristics

HSE user external clock

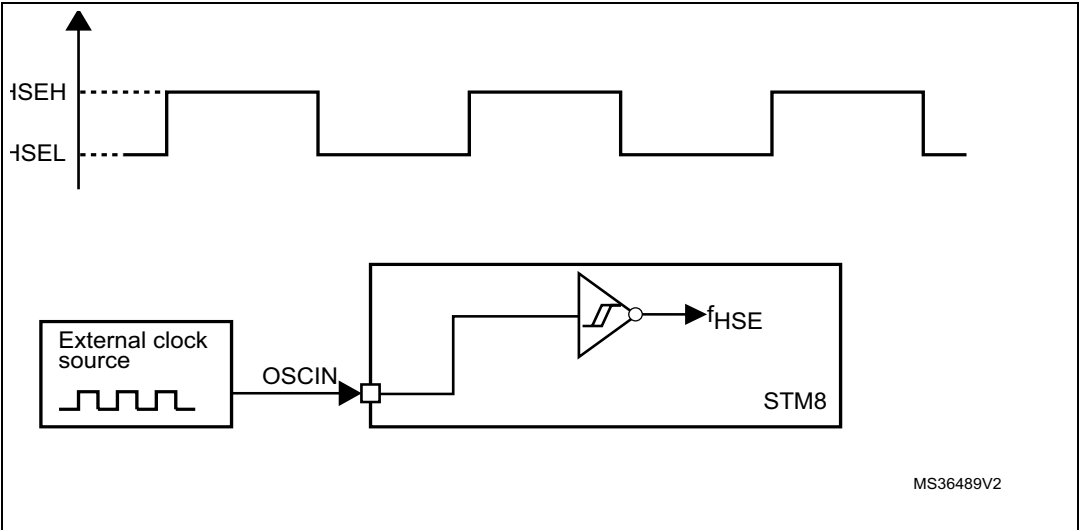
Subject to general operating conditions for V_{DD} and T_A .

Table 31. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
$V_{HSEH}^{(1)}$	OSCIN input pin high level voltage	-	$0.7 \times V_{DD}$	$V_{DD} + 0.3\text{ V}$	V
$V_{HSEL}^{(1)}$	OSCIN input pin low level voltage	-	V_{SS}	$0.3 \times V_{DD}$	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	μA

1. Data based on characterization results, not tested in production.

Figure 19. HSE external clock source



MS36489V2

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

High speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

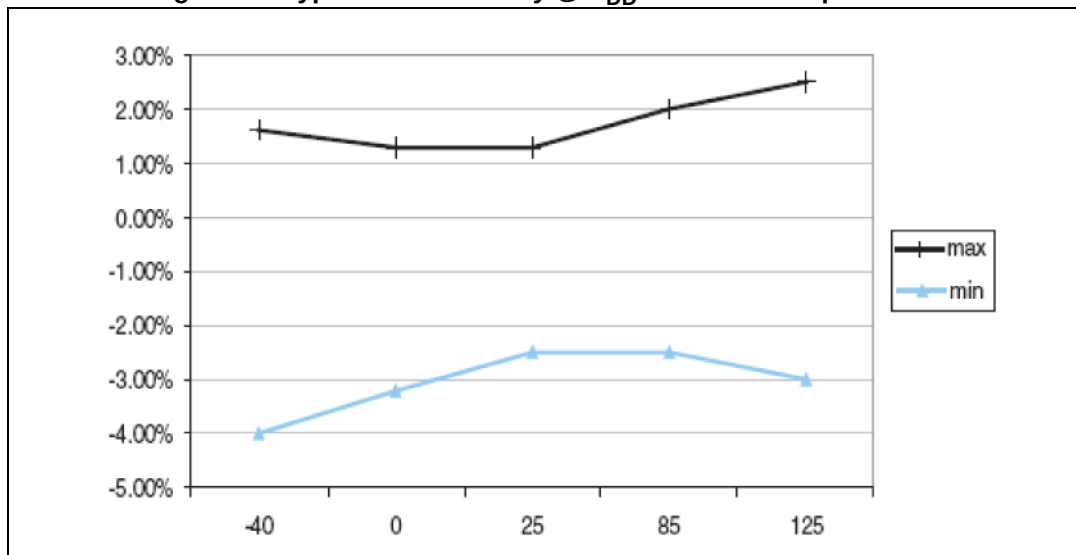
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	Accuracy of HSI oscillator	User-trimmed with CLK_HSITRIMR register for given V_{DD} and T_A conditions ⁽¹⁾	-	-	1 ⁽²⁾	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} = 5\text{ V}$, $T_A = 25\text{ °C}$ ⁽³⁾	-1.0	-	1.0	
		$V_{DD} = 5\text{ V}$, $-25\text{ °C} \leq T_A \leq 85\text{ °C}$	-2.0	-	2.0	
		$2.95\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40\text{ °C} \leq T_A \leq 125\text{ °C}$	-3.0 ⁽³⁾	-	3.0 ⁽³⁾	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration	-	-	-	1.0 ⁽²⁾	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250 ⁽³⁾	μA

1. Refer to application note.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

Figure 21. Typical HSI accuracy @ $V_{DD} = 5\text{ V}$ vs 5 temperatures



10.3.5 Memory characteristics

RAM and hardware registers

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode ⁽¹⁾	Halt mode (or reset)	V_{IT-max} ⁽²⁾	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.

2. Refer to [Section 10.3: Operating conditions](#) for the value of V_{IT-max} .

Flash program memory/data EEPROM memory

Table 36. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	$f_{CPU} \leq 16 \text{ MHz}$	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/128 byte)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 byte)	-	-	3	3.33	
t_{erase}	Erase time for 1 block (128 byte)	-	-	3	3.33	
N_{RW}	Erase/write cycles (program memory) ⁽²⁾	$T_A = +85^\circ\text{C}$	10k	-	-	cycle
	Erase/write cycles (data memory) ⁽²⁾	$T_A = +125^\circ\text{C}$	300k	1M	-	
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at $T_A = +55^\circ\text{C}$	$T_{RET} = 55^\circ\text{C}$	20	-	-	year
	Data retention (data memory) after 300k erase/write cycles at $T_A = +125^\circ\text{C}$	$T_{RET} = 85^\circ\text{C}$	1	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 byte)	-	-	2	-	mA

1. Data based on characterization results, not tested in production.

2. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Figure 33. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3\text{ V}$
(standard ports)

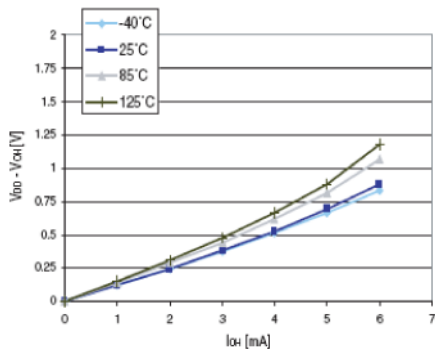


Figure 34. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0\text{ V}$
(standard ports)

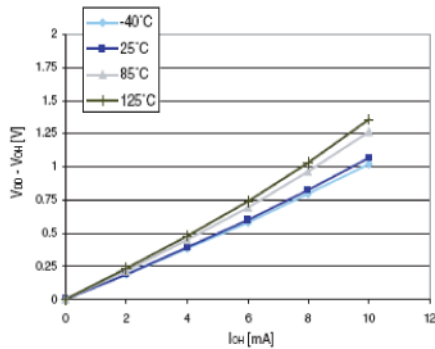


Figure 35. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3\text{ V}$ (high
sink ports)

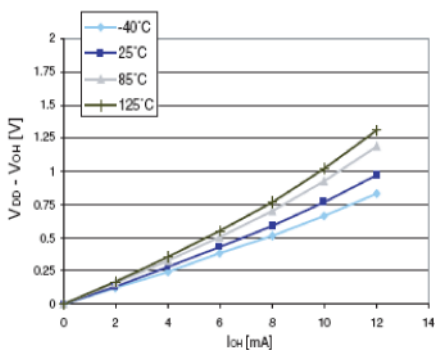
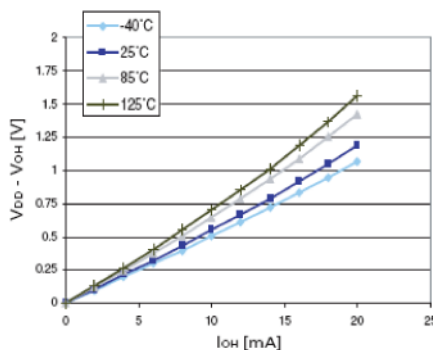


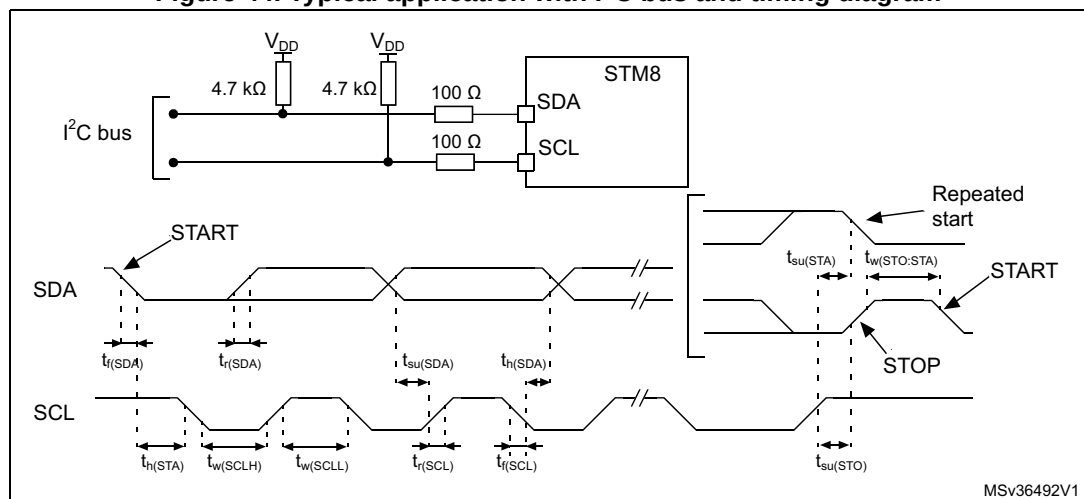
Figure 36. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0\text{ V}$ (high
sink ports)



10.3.10 I²C interface characteristicsTable 43. I²C characteristics

Symbol	Parameter	Standard mode I ² C		Fast mode I ² C ⁽¹⁾		Unit
		Min ⁽²⁾	Max ⁽²⁾	Min ⁽²⁾	Max ⁽²⁾	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_h(SDA)$	SDA data hold time	0 ⁽³⁾	-	0 ⁽⁴⁾	900 ⁽³⁾	
$t_r(SDA)$ $t_r(SCL)$	SDA and SCL rise time ($V_{DD} = 3$ to 5.5 V)	-	1000	-	300	
$t_f(SDA)$ $t_f(SCL)$	SDA and SCL fall time ($V_{DD} = 3$ to 5.5 V)	-	300	-	300	
$t_h(STA)$	START condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_w(STO:STA)$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER} must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

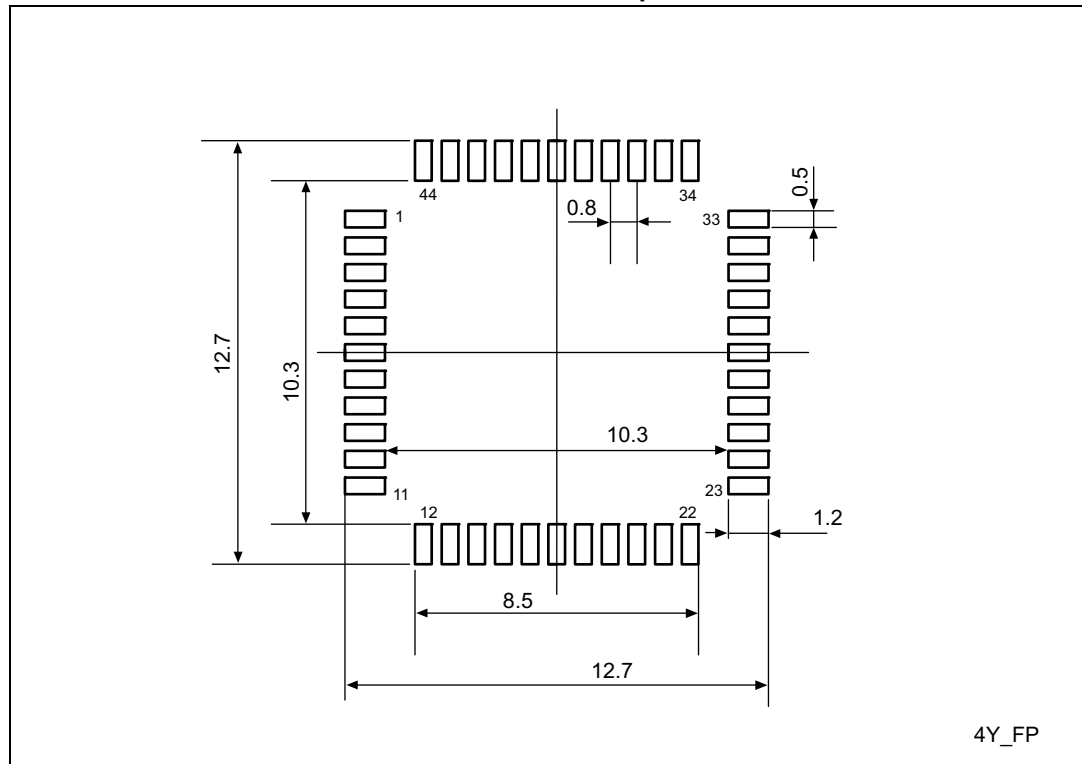
Figure 44. Typical application with I²C bus and timing diagram

**Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 51. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

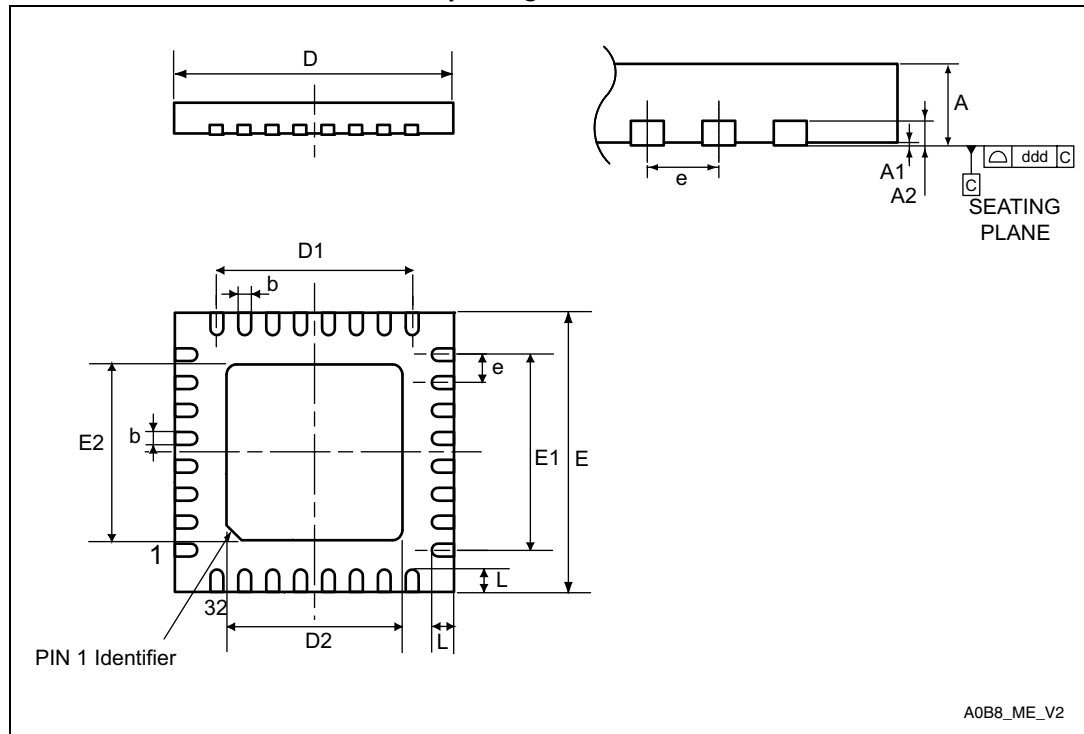
**Table 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.4 UFQFPN32 package information

Figure 56. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

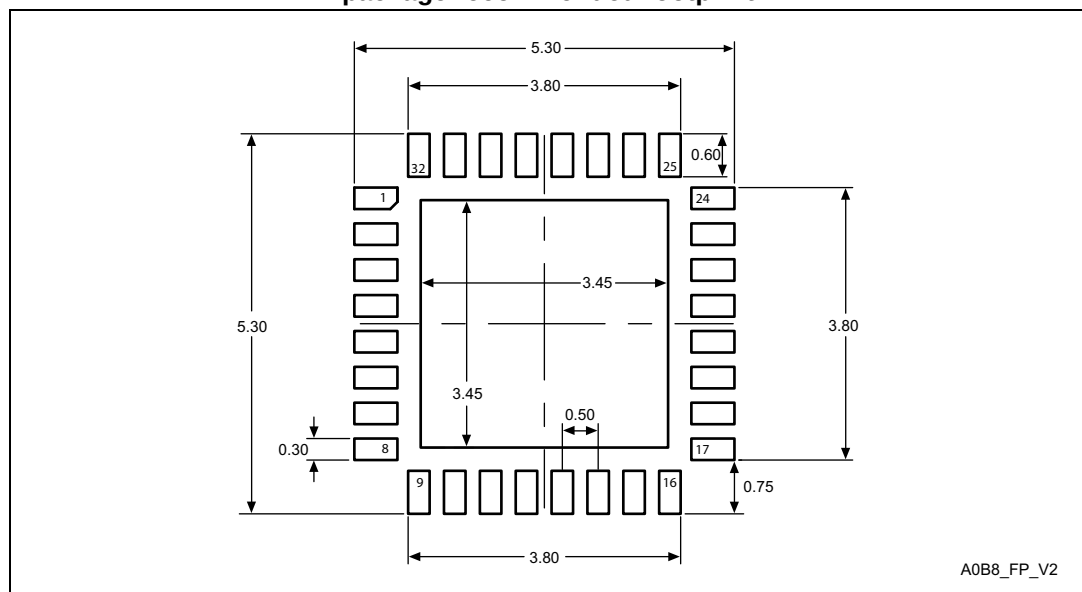


1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

Table 54. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. UFQFPN32 - 32-pin, 5 x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

Table 55. SDIP32 package mechanical data (continued)

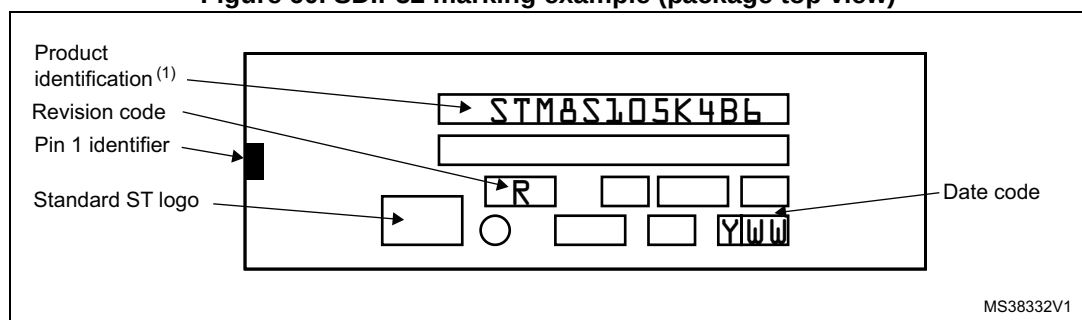
Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
eB	-	-	12.700	-	-	0.5000
L	2.540	3.048	3.810	0.1000	0.1200	0.1500

1. Values in inches are converted from mm and rounded to 4 decimal digits

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 60. SDIP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.