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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105s4t6ctr

Table 1. STM8S105x4/6 access line features

Device	STM8S105C6	STM8S105C4	STM8S105S6	STM8S105S4	STM8S105K6	STM8S105K4
Pin count	48	48	44	44	32	32
Maximum number of GPIOs	38	38	34	34	25	25
Ext. Interrupt pins	35	35	31	31	23	23
Timer CAPCOM channels	9	9	8	8	8	8
Timer complementary outputs	3	3	3	3	3	3
A/D Converter channels	10	10	9	9	7	7
High sink I/Os	16	16	15	15	12	12
Medium density Flash Program memory (byte)	32K	16K	32K	16K	32K	16K
Data EEPROM (bytes)	1024	1024	1024	1024	1024	1024
RAM (bytes)	2K	2K	2K	2K	2K	2K
Peripheral set	Advanced control timer (TIM1), General-purpose timers (TIM2 and TIM3), Basic timer (TIM4) SPI, I2C, UART, Window WDG, Independent WDG, ADC					

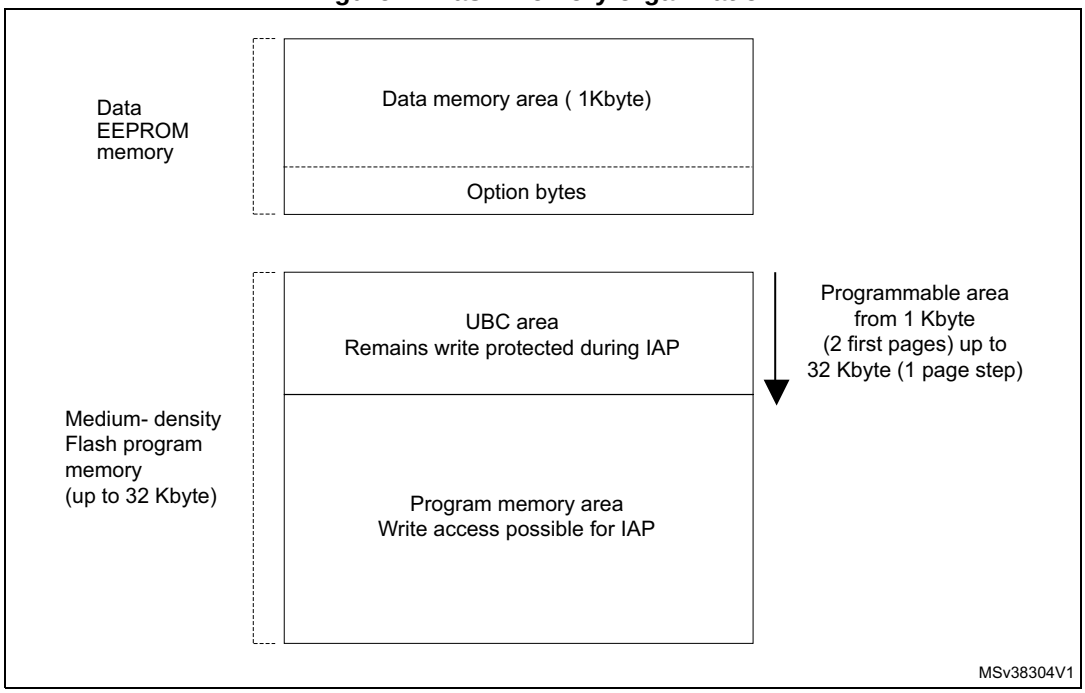
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (512 byte) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 32 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 32 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	22	-	-	PE6/ AIN9	I/O	X	X	X	-	O1	X	X	Port E6	Analog input 9(3)	-
25	23	17	22	PE5/ SPI_NSS	I/O	X	X	X	-	O1	X	X	Port E5	SPI master/ slave select	-
26	24	18	23	PC1/ TIM1_CH1/ UART2_CK	I/O	X	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1/ UART2 synchron ous clock	-
27	25	19	24	PC2/ TIM1_CH2	I/O	X	X	X	HS	O3	X	X	Port C2	Timer 1- channel 2	-
28	26	20	25	PC3/ TIM1_CH3	I/O	X	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
29	-	21	26	PC4/ TIM1_CH4	I/O	X	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4	-
30	27	22	27	PC5/ SPI_SCK	I/O	X		X	HS	O3	X	X	Port C5	SPI clock	-
31	28	-	-	VSSIO_2	S	-	-	-	-	-	-	-	I/O ground		-
32	29	-	-	VDDIO_2	S	-	-	-	-	-	-	-	I/O power supply		-
33	30	23	28	PC6/ SPI_MOSI	I/O	X	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-
34	31	24	29	PC7/ SPI_ MISO	I/O	X	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
35	32	-	-	PG0	I/O	X	X	-	-	O1	X	X	Port G0	-	-
36	33	-	-	PG1	I/O	X	X	-	-	O1	X	X	Port G1	-	-
37	-	-	-	PE3/ TIM1_BKIN	I/O	X	X	X	-	O1	X	X	Port E3	Timer 1 - break input	-
38	34	-	-	PE2/ I 2C_ SDA	I/O	X	-	X	-	O1	T (4)	-	Port E2	I 2C data	-
39	35	-	-	PE1/ I2C_ SCL	I/O	X	-	X	-	O1	T (4)	-	Port E1	I 2C clock	-

Table 5. STM8S105x4/6 pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/UFQFPN32	SDIP32			Floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
40	36	-	-	PE0/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	Port E0	Configurable clock output	-
41	37	25	30	PD0/ TIM3_CH2 [TIM1_BKIN] [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	Port D0	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	38	26	31	PD1/ SWIM(5)	I/O	**X**	X	X	X	HS	O4	X	Port D1	SWIM data interface	-
43	39	27	32	PD2/ TIM3_CH1 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	40	28	1	PD3/ TIM2_CH2 [ADC_ETR]	I/O	**X**	X	X	HS	O3	X	X	Port D3	Timer 2 - channel 2	ADC_ETR [AFR0]
45	41	29	2	PD4/ TIM2_CH1 [BEEP]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1	BEEP output [AFR7]
46	42	30	3	PD5/ UART2_TX	I/O	**X**	X	X	-	O1	X	X	Port D5	UART2 data transmit	-
47	43	31	4	PD6/ UART2_RX	I/O	**X**	X	X	-	O1	X	X	Port D6	UART2 data receive	-
48	44	32	5	PD7/ TLI [TIM1_CH4	I/O	**X**	X	X	-	O1	X	X	Port D7	Top level interrupt	TIM1_CH4 [AFR4]

1. A pull-up is applied to PF4 during the reset phase. This pin is input floating after reset release.
2. AIN12 is not selectable in ADC scan mode or with analog watchdog.
3. In 44-pin package, AIN9 cannot be used by ADC scan mode.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
20	UART2	Tx complete	-	-	0x00 8058
21	UART2	Receive register DATA FULL	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified ‘on the fly’ by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF
0x480B	Reserved	OPT6	Reserved								0x00
0x480C		NOPT6	Reserved								0xFF
0x480D	Reserved	OPT7	Reserved								0x00
0x480E		NOPT7	Reserved								0xFF
0x480F	Reserved	-	Reserved								-
0x48FD		-	Reserved								-

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Typical current consumption

For typical current consumption measurements, VDD, VDDIO and VDDA are connected together in the configuration shown in the following figure.

Figure 8. Supply current measurement conditions

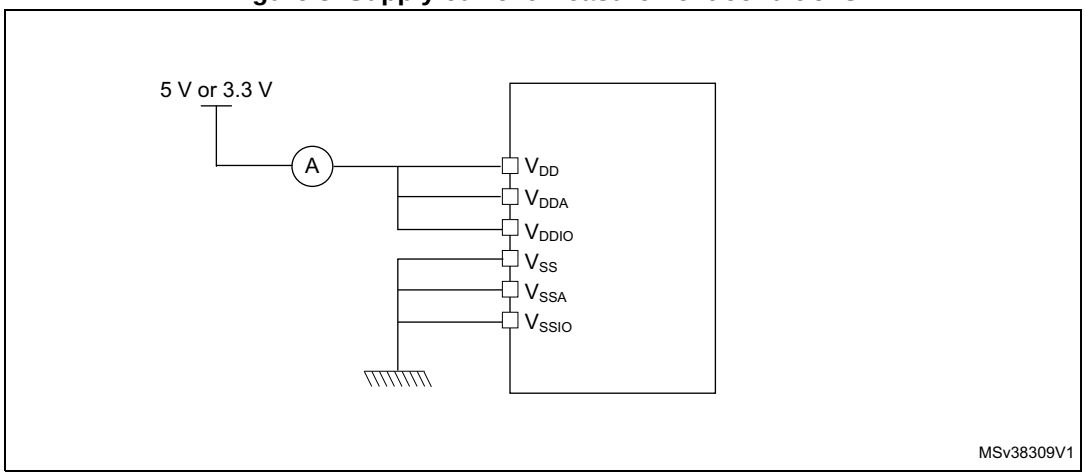


Table 18. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	-40	85	°C
T_A	Ambient temperature for suffix 3 version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax}- T_A)/\Theta_{JA}$ (see *Section 12: Thermal characteristics*) with the value for T_{Jmax} given in the previous table and the value for Θ_{JA} given in *Section 12: Thermal characteristics*.
4. See *Section 12: Thermal characteristics*.

Figure 11. f_{CPUmax} versus V_{DD}

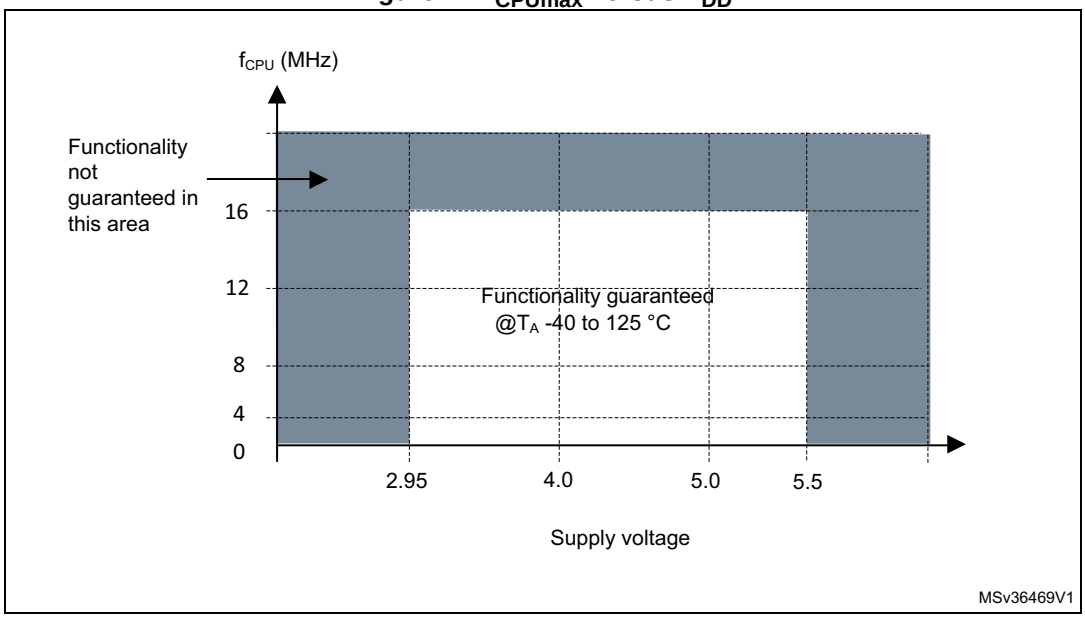


Table 19. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7(1)	ms

Table 19. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.65	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 30. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	230	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	115	
$I_{DD(TIM3)}$	TIM3 supply current(1)	90	
$I_{DD(TIM4)}$	TIM4 supply current(1)	30	
$I_{DD(UART2)}$	UART2 supply current (2)	110	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	955	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

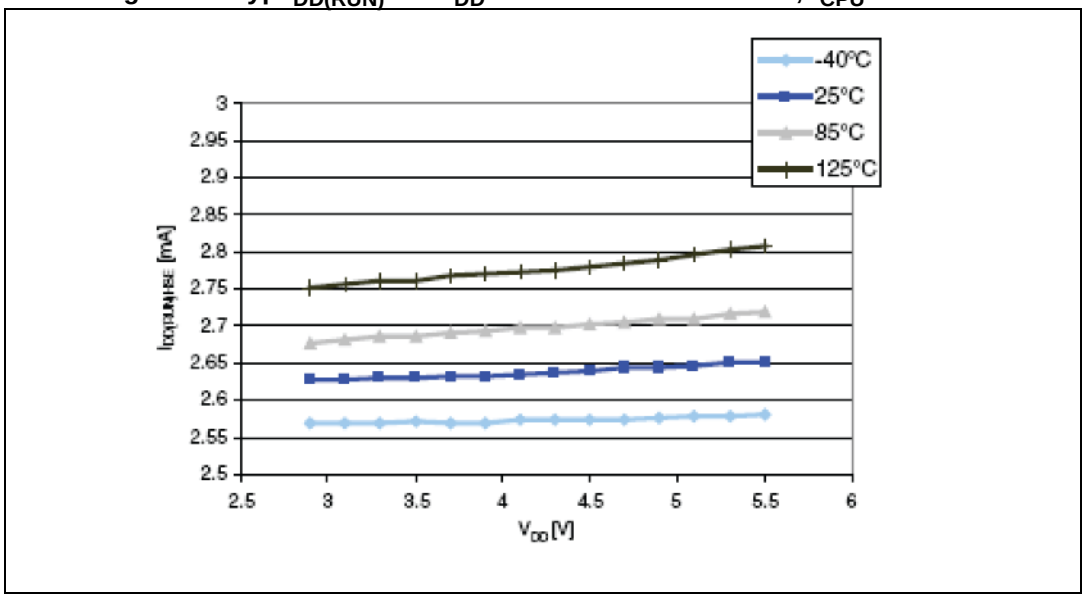


Table 42. SPI characteristics (continued)

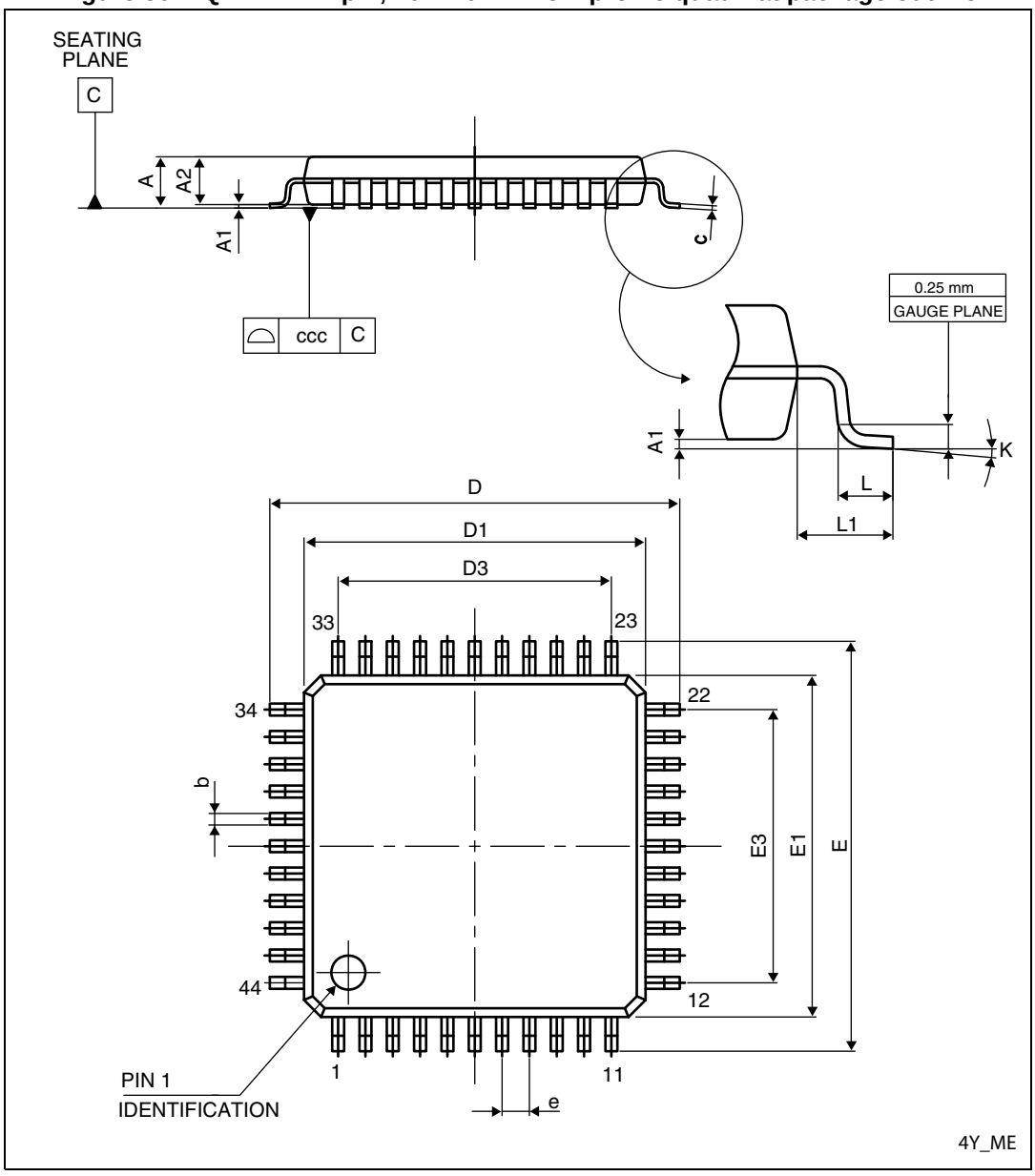
Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$[2]	NSS setup time	Slave mode	4 * t_{MASTER}	-	
$t_{h(NSS)}$[2]	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$[2] $t_{su(SI)}$[2]	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$[2] $t_{h(SI)}$[2]	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$[2][3]	Data output access time	Slave mode	-	3* t_{MASTER}	
$t_{dis(SO)}$[2][4]	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$[2]	Data output valid time	Slave mode (after enable edge)	-	73	
$t_{v(MO)}$[2]	Data output valid time	Master mode (after enable edge)	-	36	
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	28	-	
$t_{h(MO)}$[2]		Master mode (after enable edge)	12	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11.2 LQFP44 package information

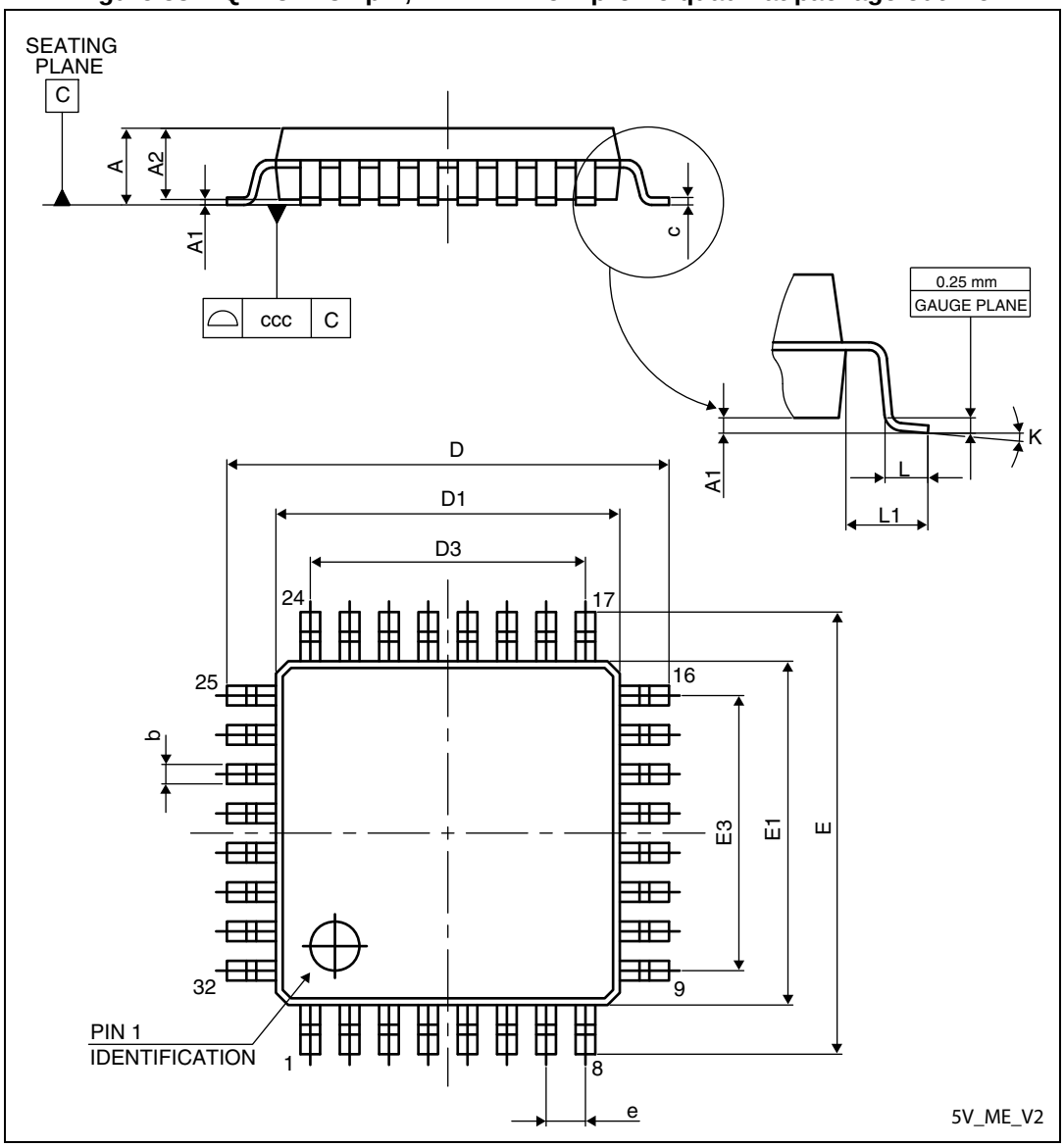
Figure 50. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

11.3 LQFP32 package information

Figure 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 18: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 56. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7x7 mm		°C/W
	Thermal resistance junction-ambient LQFP44 - 10x10 mm		
	Thermal resistance junction-ambient LQFP32 - 7x7 mm		
	Thermal resistance junction-ambient UFQFPN32 - 5x5 mm		
	Thermal resistance junction-ambient SDIP32 - 400 ml		

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for the STM8 programming.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.