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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s105s6t6ctr

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Table 1. STM8S105x4/6 access line features

Device	STM8S105C6	STM8S105C4	STM8S105S6	STM8S105S4	STM8S105K6	STM8S105K4
Pin count	48	48	44	44	32	32
Maximum number of GPIOs	38	38	34	34	25	25
Ext. Interrupt pins	35	35	31	31	23	23
Timer CAPCOM channels	9	9	8	8	8	8
Timer complementary outputs	3	3	3	3	3	3
A/D Converter channels	10	10	9	9	7	7
High sink I/Os	16	16	15	15	12	12
Medium density Flash Program memory (byte)	32K	16K	32K	16K	32K	16K
Data EEPROM (bytes)	1024	1024	1024	1024	1024	1024
RAM (bytes)	2K	2K	2K	2K	2K	2K
Peripheral set	Advanced control timer (TIM1), General-purpose timers (TIM2 and TIM3), Basic timer (TIM4) SPI, I2C, UART, Window WDG, Independent WDG, ADC					

The IWDG time base spans from 60 μ s to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

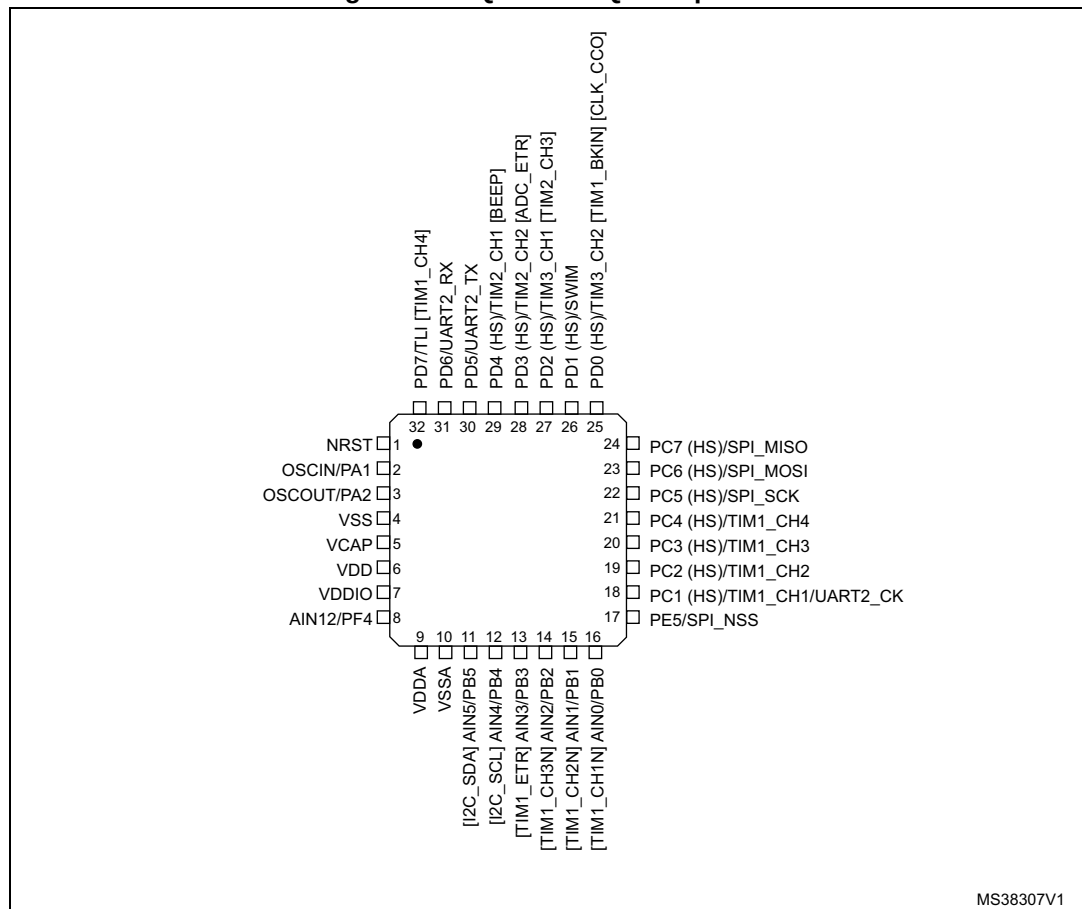
This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1...32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Figure 5. UFQFPN32/LQFP32 pinout



MS38307V1

1. (HS) high sink capability.
2. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 Interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530C		TIM2_PSCR	IM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC_AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

Table 11. Option byte (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x487E	Bootloader	OPTBL	BL[7:0]								0x00
0x487F		NOPTBL	NBL[7:0]								0xFF

Table 12. Option byte description

Option byte no.	Description
OPT0	ROP[7:0] Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) <i>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</i>
OPT1	UBC[7:0] User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03: Page 0 to 4 defined as UBC, memory write-protected ... 0x3E: Pages 0 to 63 defined as UBC, memory write-protected Other values: Reserved <i>Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.</i>
OPT2	AFR[7:0] Refer to the following table for the description of the alternate function remapping description of bits [7:2].
OPT3	HSITRIM: High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

Table 21. Total current consumption with code execution in run mode at $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER} = 16\text{ MHz}$	HSE crystal osc. (16 MHz)	2.8	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER} / 128 = 125\text{ kHz}$	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER} / 128 = 15.625\text{ kHz}$	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER} = 128\text{ kHz}$	LSI RC osc. (128 kHz)	0.55	-	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER} = 16\text{ MHz}$	HSE crystal osc. (16 MHz)	7.3	-	mA
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc. (16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER} = 2\text{ MHz}$	HSI RC osc. (16 MHz/8) ⁽²⁾	1.5	-	
		$f_{CPU} = f_{MASTER} / 128 = 125\text{ kHz}$	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER} / 128 = 15.625\text{ kHz}$	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER} = 128\text{ kHz}$	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.

2. Default clock configuration measured with all peripherals off.

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at $V_{DD} = 5\text{ V}$

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER} = 16\text{ MHz}$	HSE crystal osc. (16 MHz)	2.15	-	mA
			HSE user ext. clock (16 MHz)	1.55	2.0	
			HSI RC osc. (16 MHz)	1.5	1.9	
		$f_{CPU} = f_{MASTER} / 128 = 125\text{ kHz}$	HSI RC osc. (16 MHz)	1.3	-	
		$f_{CPU} = f_{MASTER} / 128 = 15.625\text{ kHz}$	HSI RC osc. (16 MHz/8) ⁽²⁾	0.7	-	
		$f_{CPU} = f_{MASTER} = 128\text{ kHz}$	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.

2. Default clock configuration measured with all peripherals off.

Low power mode wakeup times

Table 28. Wakeup times

Symbol	Parameter	Conditions			Typ	Max ⁽¹⁾	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode ⁽²⁾	0 to 16 MHz			-	See note ⁽³⁾	μs
$t_{WU(WFI)}$	Wakeup time from run mode ⁽²⁾	$f_{CPU} = f_{MASTER} = 16 \text{ MHz}$			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode ⁽²⁾	MVR voltage regulator on ⁽⁴⁾	Flash in operating mode ⁽⁵⁾	HSI (after wakeup)	1 ⁽⁶⁾	2 ⁽⁶⁾	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode ⁽²⁾	MVR voltage regulator off ⁽⁴⁾	Flash in operating mode ⁽⁵⁾	HSI (after wakeup)	3 ⁽⁶⁾	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode ⁽²⁾	MVR voltage regulator off ⁽⁴⁾	Flash in operating mode ⁽⁵⁾	HSI (after wakeup)	48 ⁽⁶⁾	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode ⁽²⁾	MVR voltage regulator off ⁽⁴⁾	Flash in power-down mode ⁽⁵⁾	HSI (after wakeup)	50 ⁽⁶⁾	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode ⁽²⁾	Flash in operating mode ⁽⁵⁾			52	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode ⁽²⁾	Flash in power-down mode ⁽⁵⁾			54	-	

1. Data based on characterization results, not tested in production.

2. Measured from interrupt event to interrupt vector fetch

3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$

4. Configured by the REGAH bit in the CLK_ICR register.

5. Configured by the AHALT bit in the FLASH_CR1 register.

6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 29. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$I_{DD(R)}$	Supply current in reset state ⁽²⁾	$V_{DD} = 5 \text{ V}$	500	-	μA
		$V_{DD} = 3.3 \text{ V}$	400	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	μs

1. Data guaranteed by design, not tested in production.

2. Characterized with all I/Os tied to V_{SS} .

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A .

Figure 16. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE external clock, $f_{CPU} = 16\text{ MHz}$

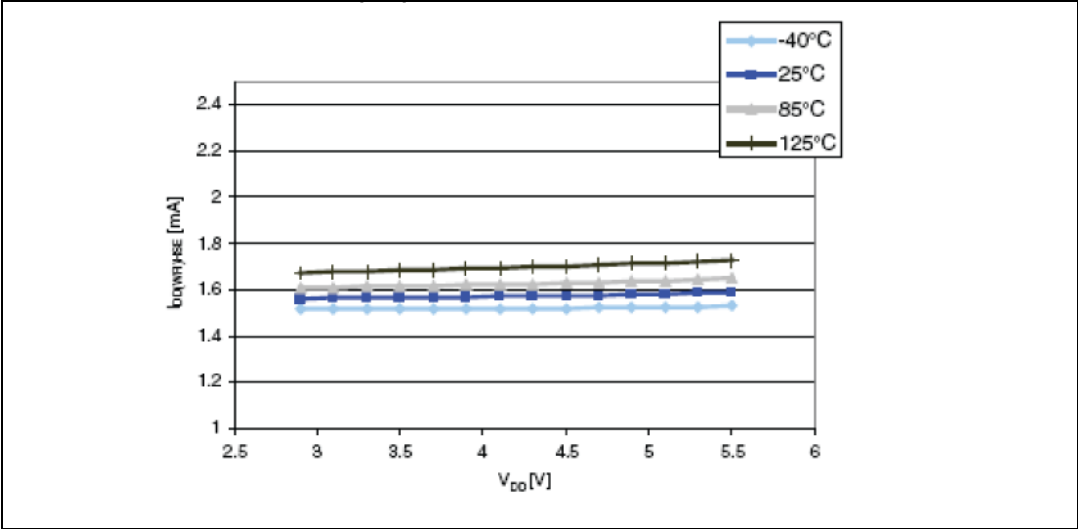
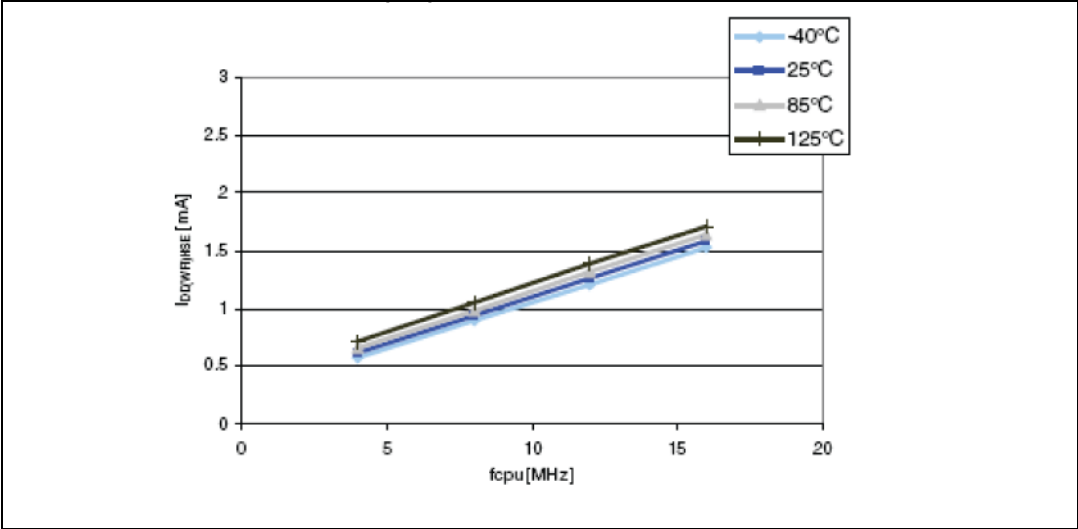


Figure 17. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, $V_{DD} = 5\text{ V}$



10.3.3 External clock sources and timing characteristics

HSE user external clock

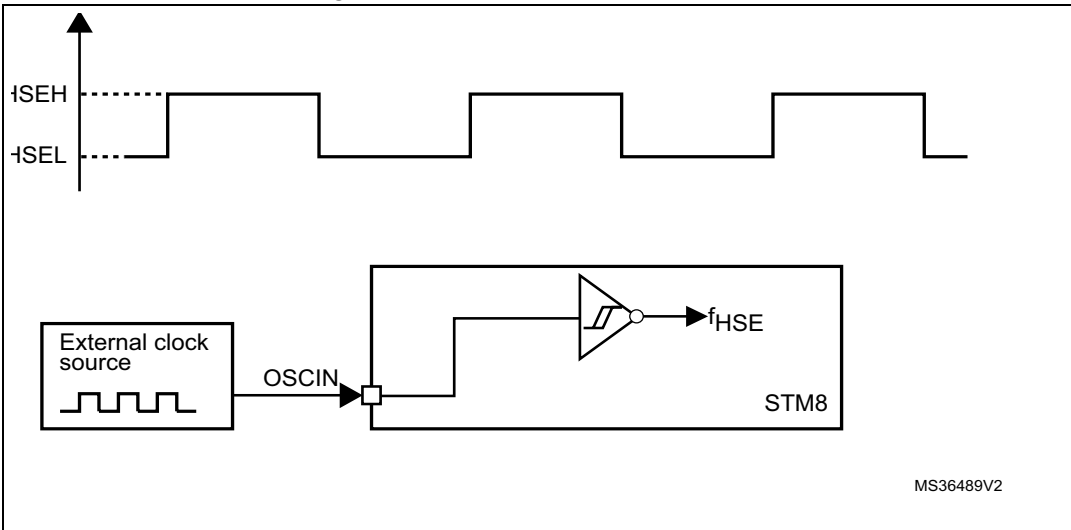
Subject to general operating conditions for V_{DD} and T_A .

Table 31. HSE user external clock characteristics

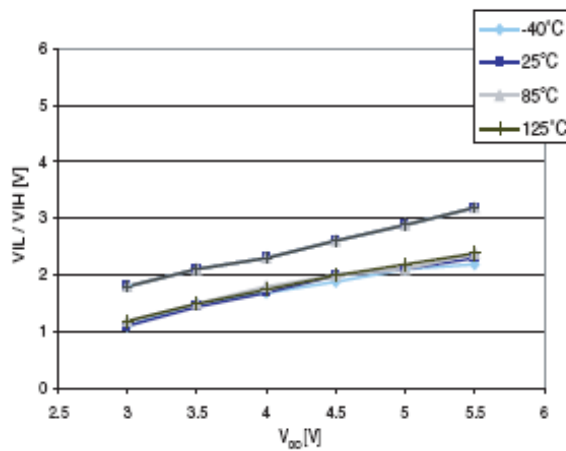
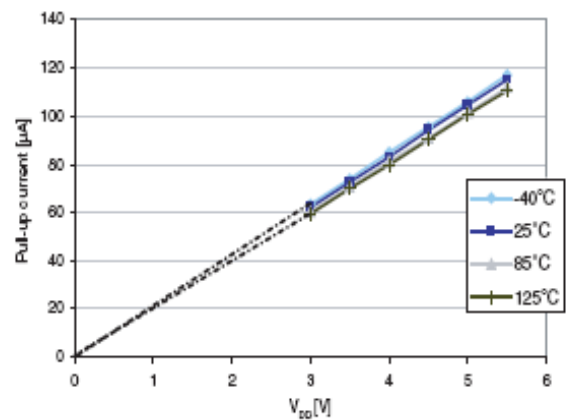
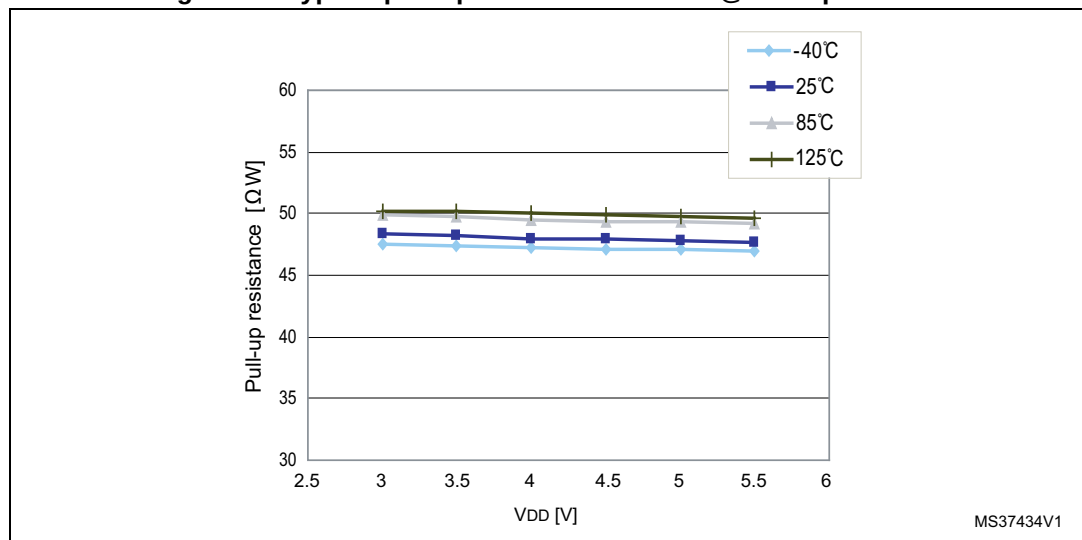
Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
$V_{HSEH}^{(1)}$	OSCIN input pin high level voltage	-	$0.7 \times V_{DD}$	$V_{DD} + 0.3 \text{ V}$	V
$V_{HSEL}^{(1)}$	OSCIN input pin low level voltage	-	V_{SS}	$0.3 \times V_{DD}$	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	μA

1. Data based on characterization results, not tested in production.

Figure 19. HSE external clock source



MS36489V2

Figure 24. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperaturesFigure 25. Typical pull-up current vs V_{DD} @ 4 temperaturesFigure 26. Typical pull-up resistance vs V_{DD} @ 4 temperatures

MS37434V1

Table 38. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$	-	2.0	V
	Output low level with 4 pins sunk	$I_{IO} = 4 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$	-	1.0 ⁽¹⁾	
V_{OH}	Output high level with 8 pins sourced	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$	2.4	-	
	Output high level with 4 pins sourced	$I_{IO} = 4 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$	2.0 ⁽¹⁾	-	

1. Data based on characterization results, not tested in production

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 48. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f _{HSE} /f _{CPU} ⁽¹⁾		
				8 MHz/ 8 MHz	8 MHz/ 16 MHz	
S _{EMI}	Peak level	V _{DD} = 5 V, T _A = 25 °C, LQFP48 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	13	14	dBμV
			30 MHz to 130 MHz	23	19	
			130 MHz to 1 GHz	-4.0	-4.0	
	EMI level		EMI level	2.0	1.5	-

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

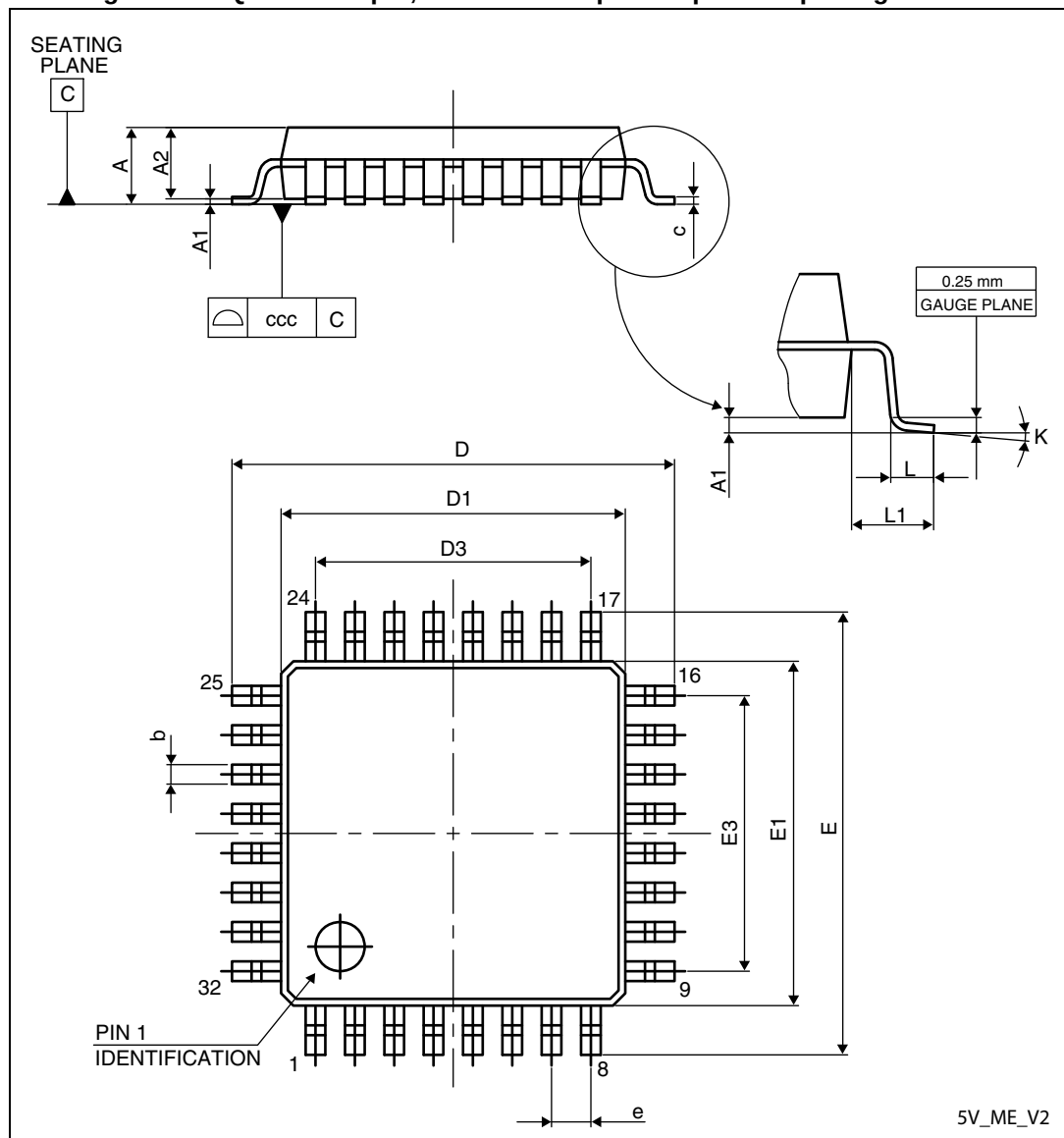
Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	$T_A = 25\text{ }^{\circ}\text{C}$, conforming to JESD22-A114	A	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	$T_A = 25\text{ }^{\circ}\text{C}$, conforming to SD22-C101	IV	1000	

1. Data based on characterization results, not tested in production

11.3 LQFP32 package information

Figure 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline

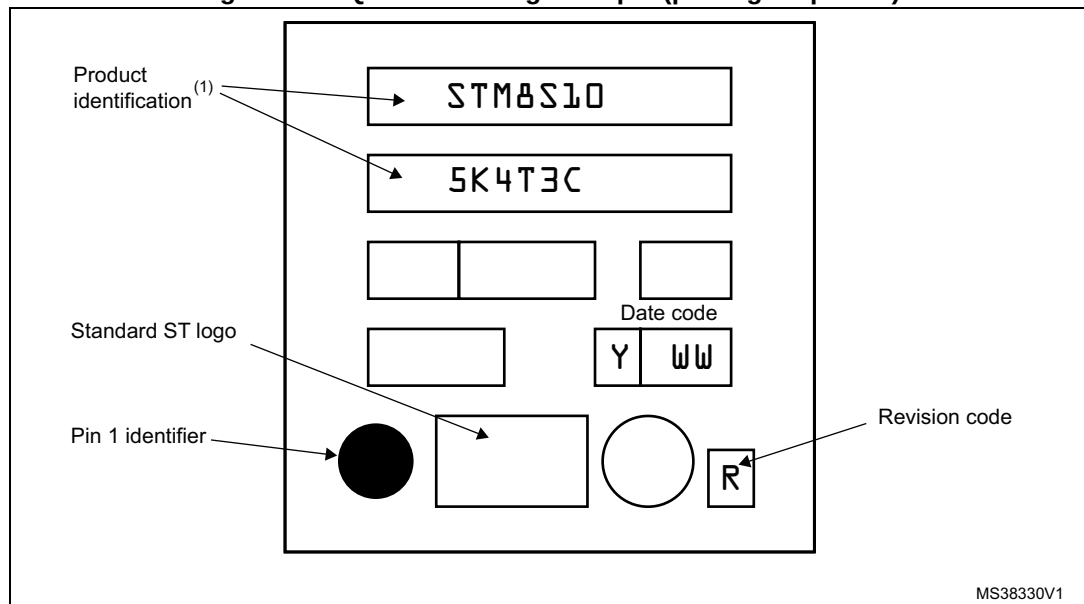


1. Drawing is not to scale.

5V_FP_V2

Device marking

Figure 55. LQFP32 marking example (package top view)

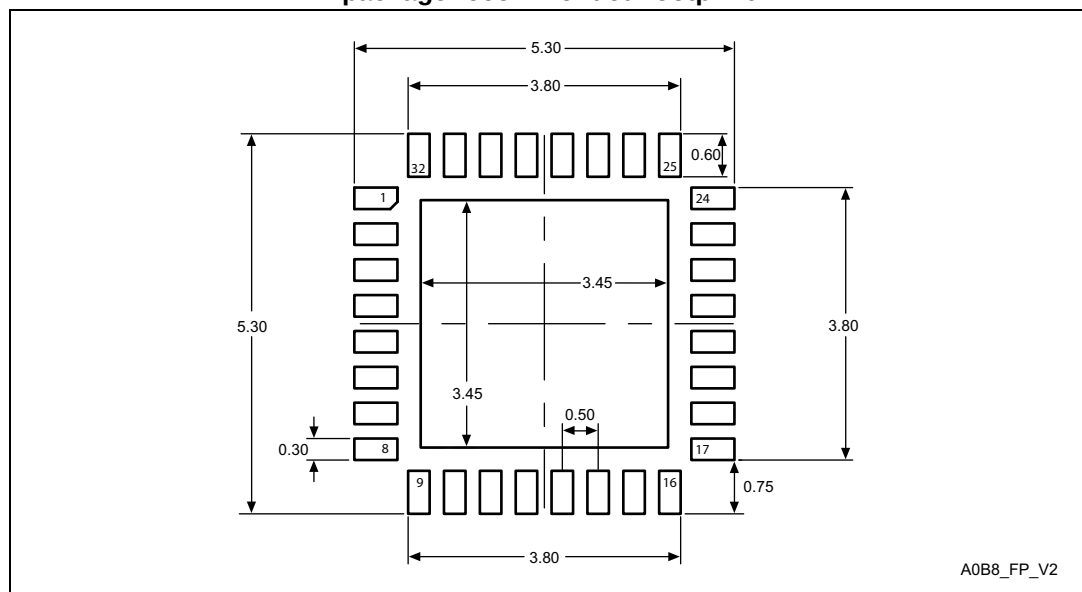


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 54. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. UFQFPN32 - 32-pin, 5 x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.