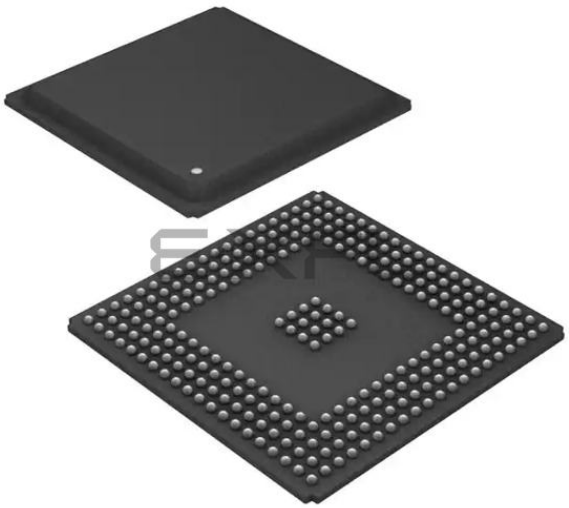

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5200cvr400b

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1.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or V_{CC}). Table 7 gives package thermal characteristics for this device.

Table 5. ESD and Latch-Up Protection Characteristics

Sym	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM)—JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM)—JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM)—JEDEC JESD22-C101	500	—	V	D4.3
I_{LAT}	Latch-up Current at T_A=85 °C positive negative	 +100 –100	—	mA	D4.4
I_{LAT}	Latch-up Current at T_A=27 °C positive negative	 +200 –200	—	mA	D4.5

1.1.5 Power Dissipation

Power dissipation of the MPC5200B is caused by 3 different components: the dissipation of the internal or core digital logic (supplied by VDD_CORE), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD) and the dissipation of the IO logic (supplied by VDD_IO_MEM and VDD_IO). Table 6 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated by the user for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f \qquad \textbf{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200B processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} \qquad \textbf{Eqn. 2}$$

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

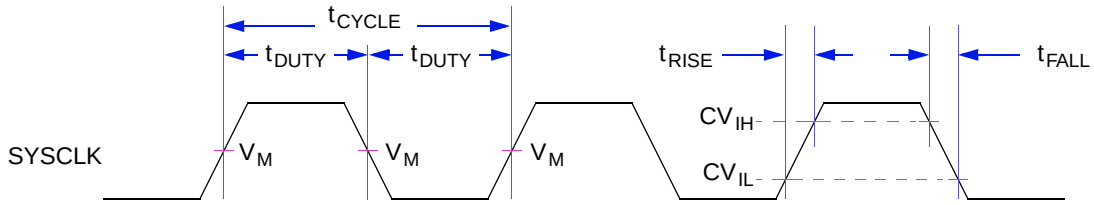

Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.(1)	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).(2)	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.

2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification.
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification.

For Measurement and Test Conditions, see the PCI Local Bus Specification.

1.3.8 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200B. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:

- WS = Wait State
- DC = Dead Cycle
- LB = Long Burst
- DS = Data Size in Bytes
- t_{PCIck} = PCI clock period
- t_{IPBIck} = IPBI clock period

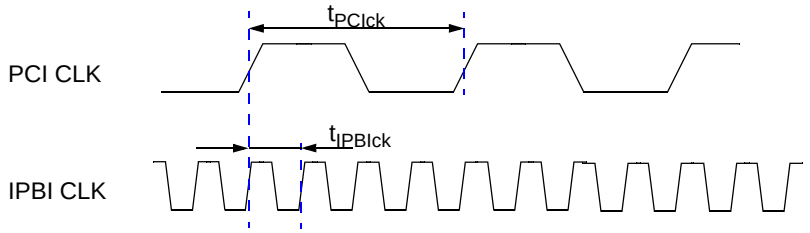

Figure 10. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

1.3.8.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.1
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.2
t_1	CS pulse width	(2 + WS) × t_{PCIck}	(2 + WS) × t_{PCIck}	ns	(1)	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	—	ns	(2)	A7.5
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.6
t_5	OE negation before CS negation	—	2.7	ns	—	A7.7
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.8
t_7	RW hold after CS negation	t_{IPBIck}	—	ns	—	A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	—	ns	—	A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	—	ns	—	A7.11

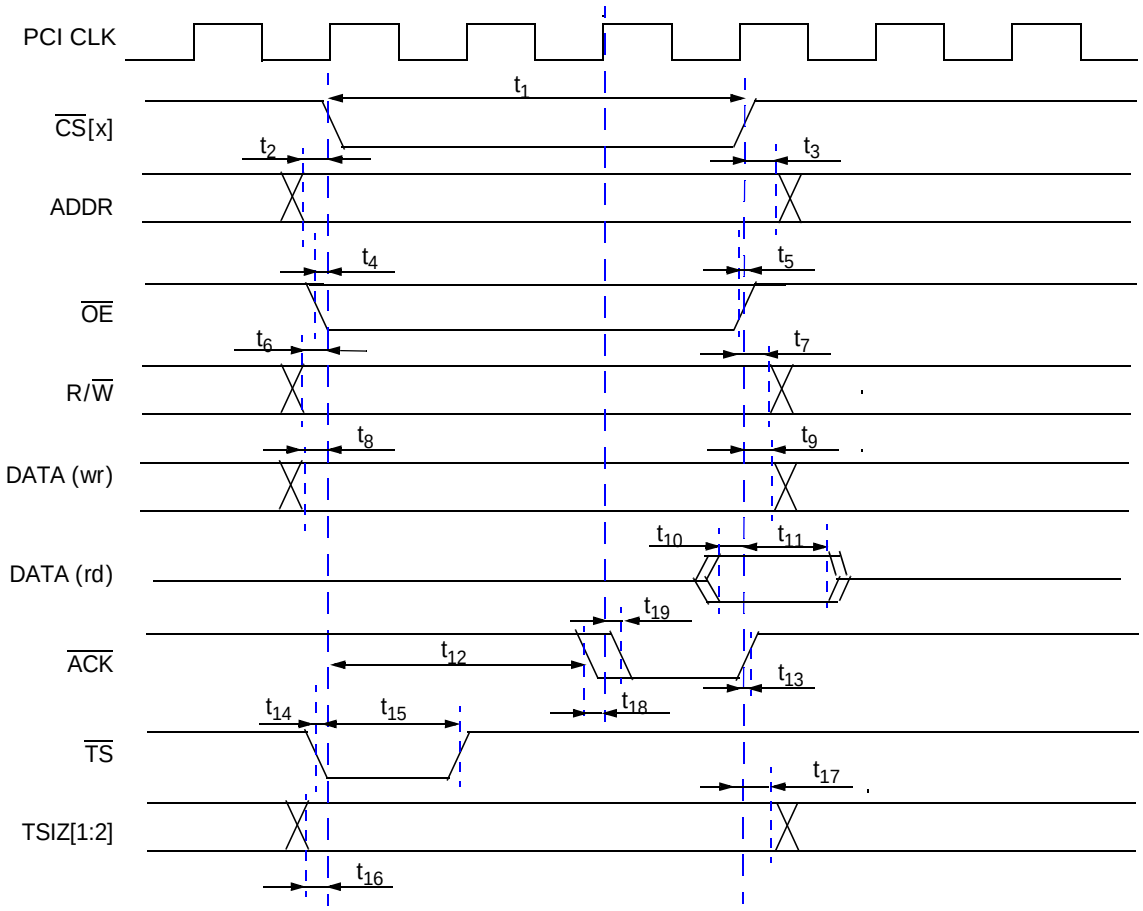

Figure 11. Timing Diagram—Non-MUXed Mode

1.3.8.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.22
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.23
t_1	CS pulse width	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	ns	(1),(2)	A7.24
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.25
t_3	ADDR hold after CS negation	–0.7	—	ns	—	A7.26
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.27
t_5	OE negation before CS negation	—	2.7	ns	—	A7.28
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.29
t_7	RW hold after CS negation	t_{PCIck}	—	ns	—	A7.30
t_8	DATA setup before rising edge of PCI clock	3.6	—	ns	—	A7.31

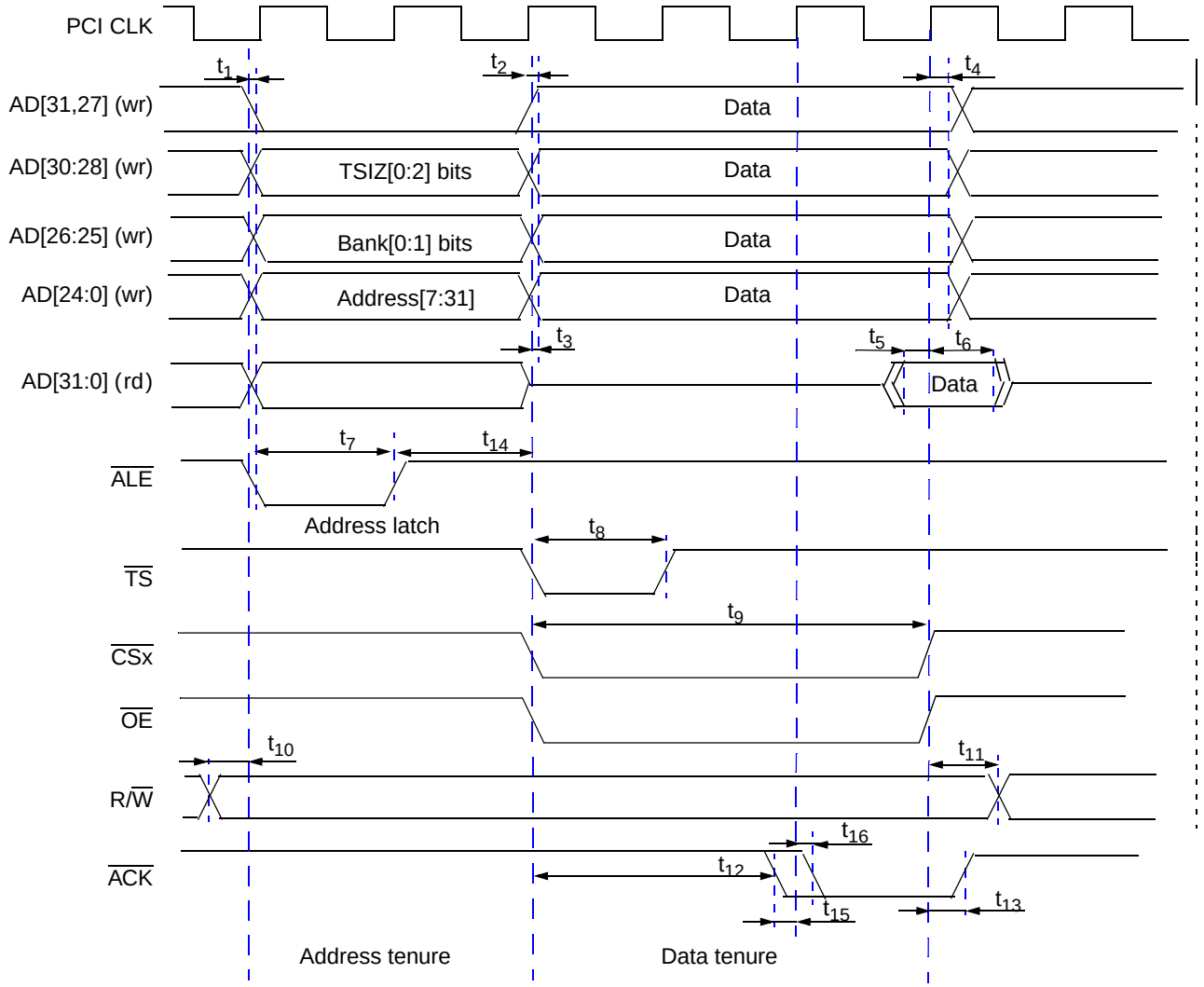

Figure 13. Timing Diagram—MUXed Mode

1.3.9 ATA

The MPC5200B ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5200B User's Manual (MPC5200BUM)*.

The MPC5200B ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold time beyond that required by the ATA-4 specification.

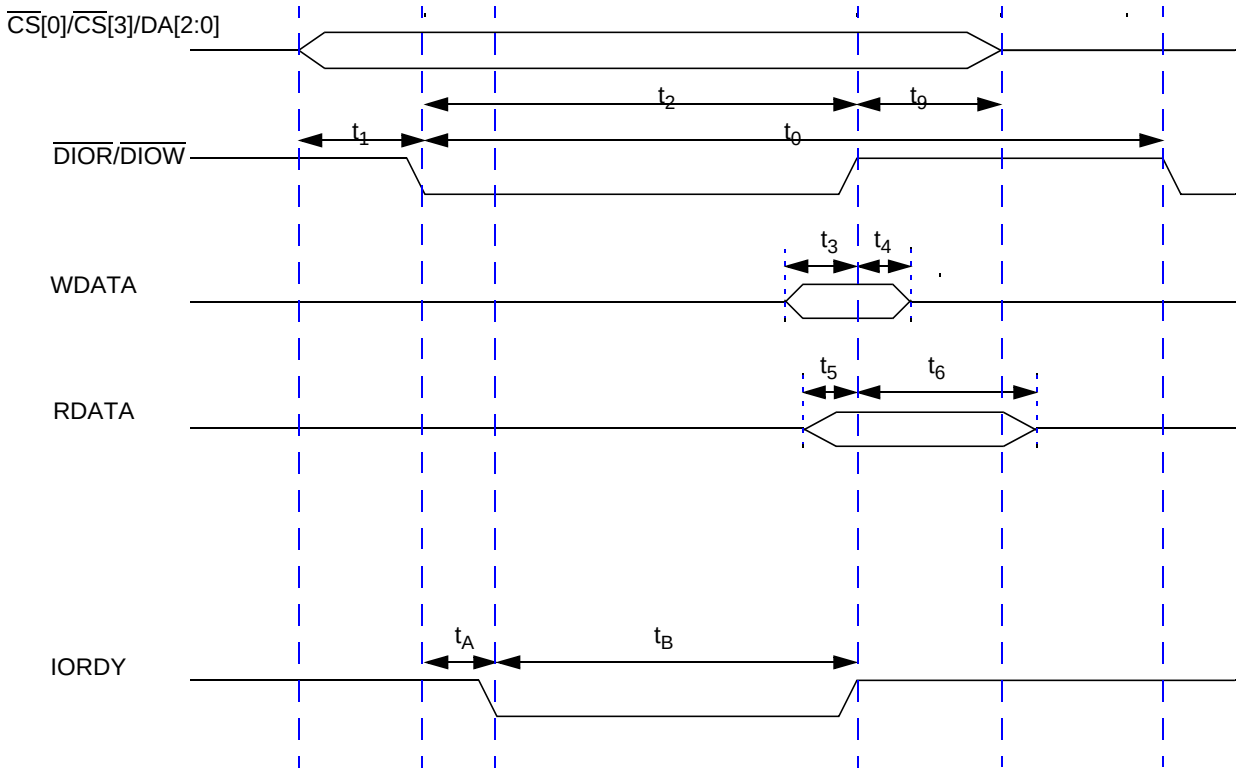

Figure 14. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

Sym	Multiword DMA Timing Parameters	Min/Max	Mode 0(ns)	Mode 1(ns)	Mode 2(ns)	SpecID
t_0	Cycle Time	min	480	150	120	A8.12
t_C	$\overline{\text{DMACK}}$ to DMARQ delay	max	—	—	—	A8.13
t_D	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width (16-bit)	min	215	80	70	A8.14
t_E	$\overline{\text{DIOR}}$ data access	max	150	60	50	A8.15
t_G	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ data setup	min	100	30	20	A8.16
t_F	$\overline{\text{DIOR}}$ data hold	min	5	5	5	A8.17
t_H	$\overline{\text{DIOW}}$ data hold	min	20	15	10	A8.18
t_I	DMACK to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	0	0	0	A8.19
t_J	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to $\overline{\text{DMACK}}$ hold	min	20	5	5	A8.20
t_{Kr}	$\overline{\text{DIOR}}$ negated pulse width	min	50	50	25	A8.21
t_{Kw}	$\overline{\text{DIOW}}$ negated pulse width	min	215	50	25	A8.22
t_{Lr}	$\overline{\text{DIOR}}$ to DMARQ delay	max	120	40	35	A8.23
t_{Lw}	$\overline{\text{DIOW}}$ to DMARQ delay	max	40	40	35	A8.24

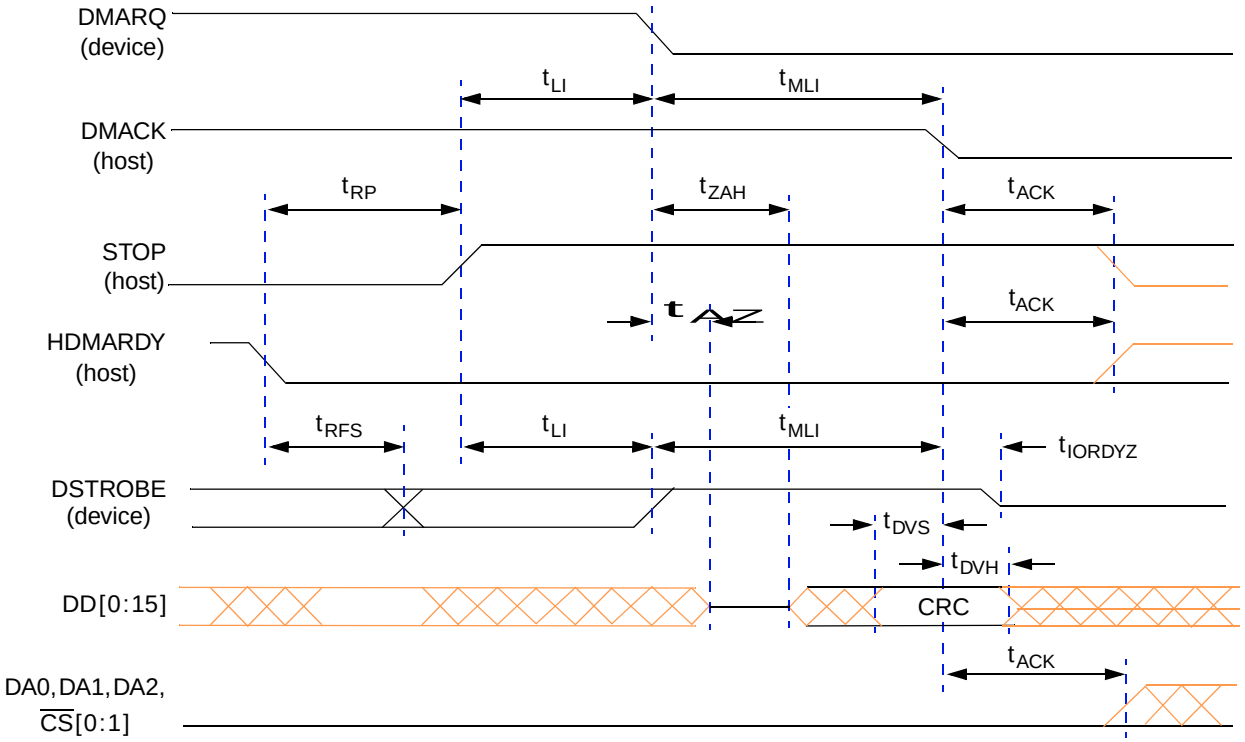

Figure 20. Timing Diagram—Host Terminating Ultra DMA Data In Burst

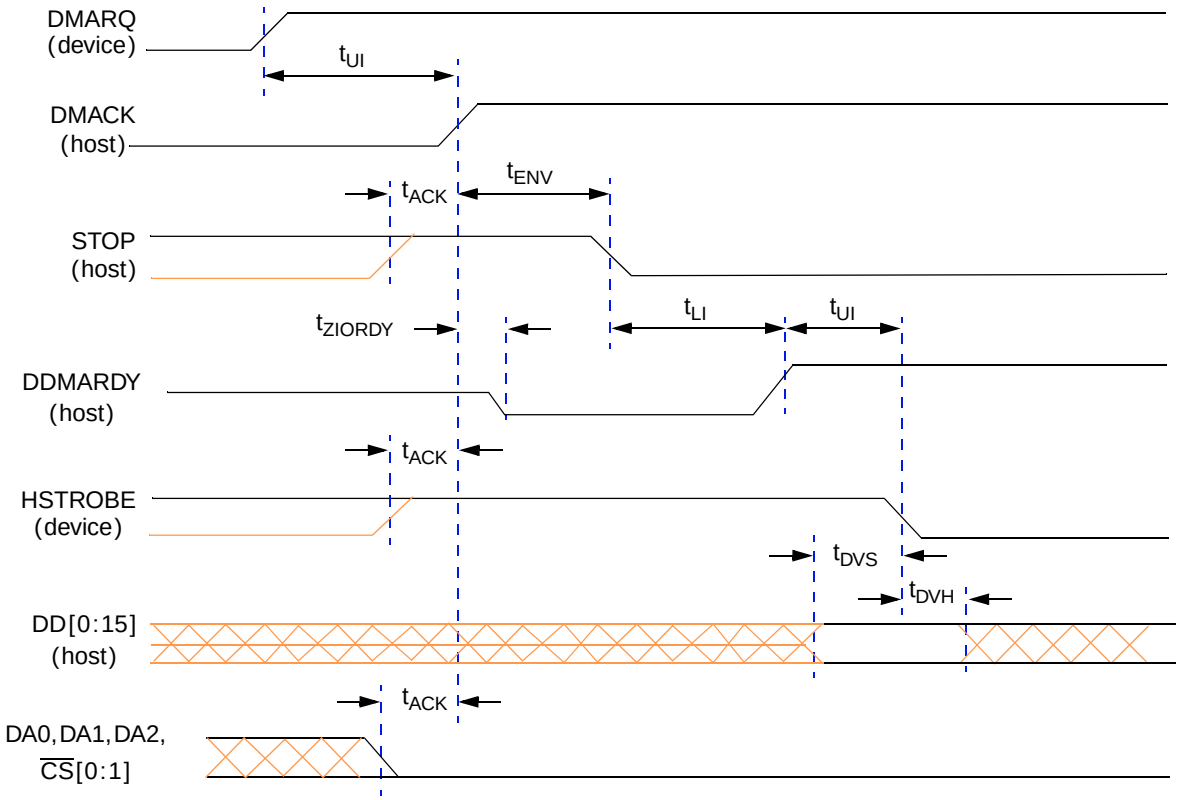

Figure 21. Timing Diagram—Initiating an Ultra DMA Data Out Burst

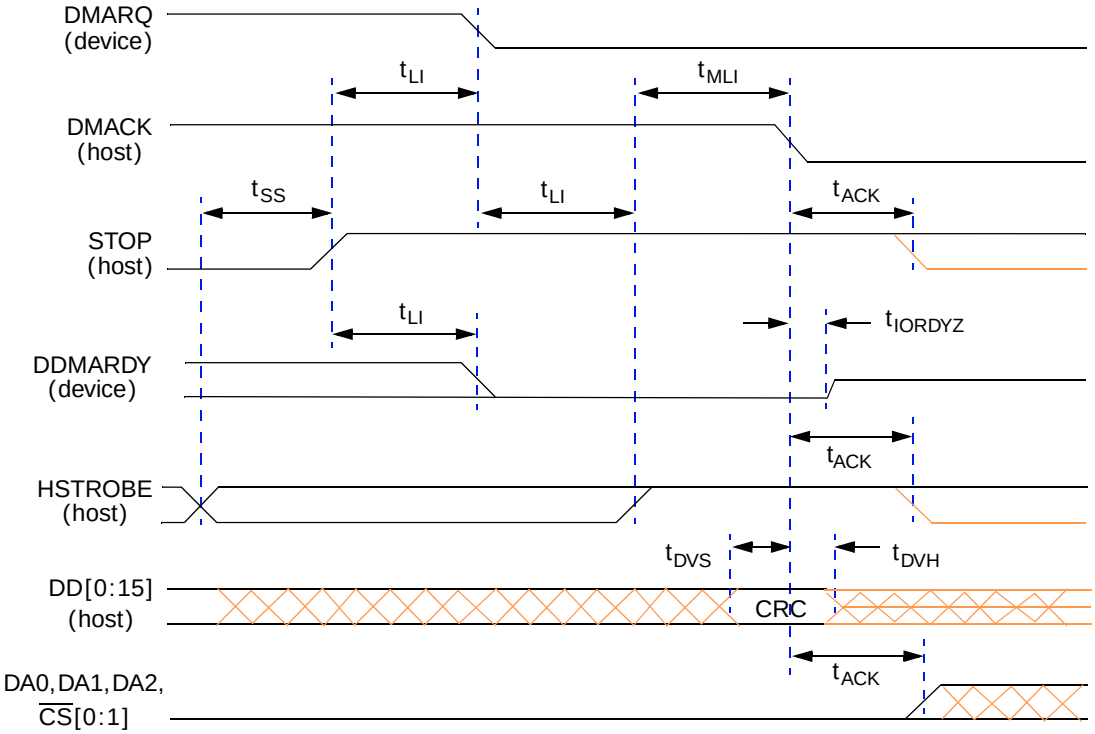

Figure 24. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

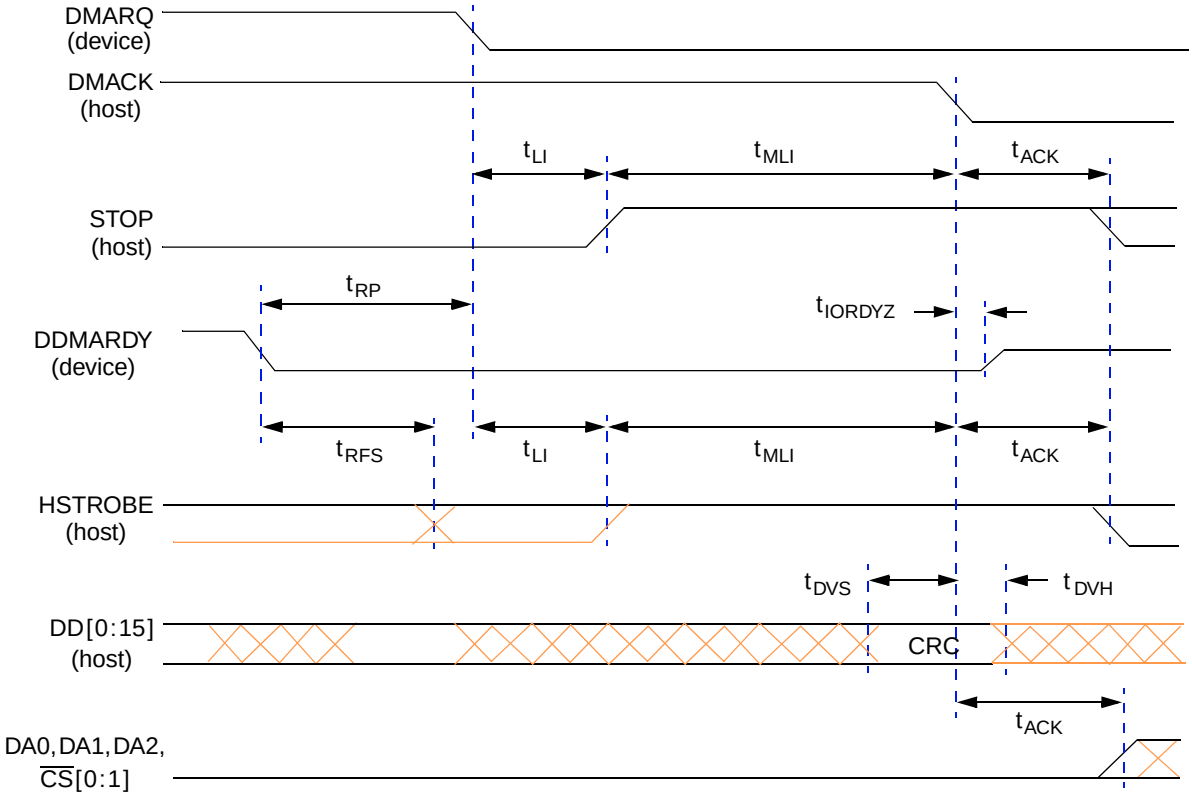

Figure 25. Timing Diagram—Drive Terminating Ultra DMA Data Out Burst

Table 32. MII Tx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns	A9.5
t_6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A9.6
t_7	TX_CLK pulse width high	35%	65%	TX_CLK Period(1)	A9.7
t_8	TX_CLK pulse width low	35%	65%	TX_CLK Period(1)	A9.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

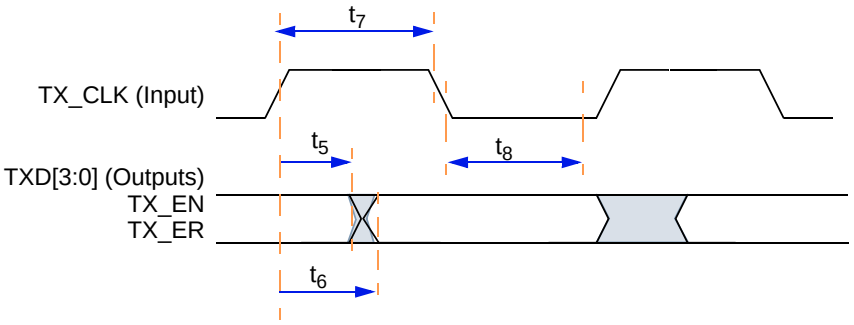

Figure 28. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A9.9

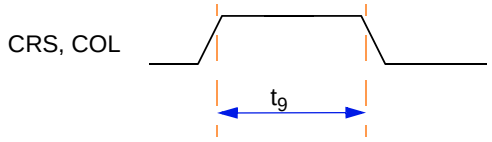

Figure 29. Ethernet Timing Diagram—MII Async

Table 34. MII Serial Management Channel Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_{10}	MDC falling edge to MDIO output delay	0	25	ns	A9.10
t_{11}	MDIO (input) to MDC rising edge setup	10	—	ns	A9.11
t_{12}	MDIO (input) to MDC rising edge hold	10	—	ns	A9.12
t_{13}	MDC pulse width high(1)	160	—	ns	A9.13
t_{14}	MDC pulse width low(1)	160	—	ns	A9.14
t_{15}	MDC period(2)	400	—	ns	A9.15

1 MDC is generated by MPC5200B with a duty cycle of 50% except when MII_SPEED in the FEC MII_SPEED control register is changed during operation. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 The MDC period must be set to a value of less than or equal to 2.5 MHz (to be compliant with the IEEE MII characteristic) by programming the FEC MII_SPEED control register. See the *MPC5200B User's Manual (MPC5200BUM)*.

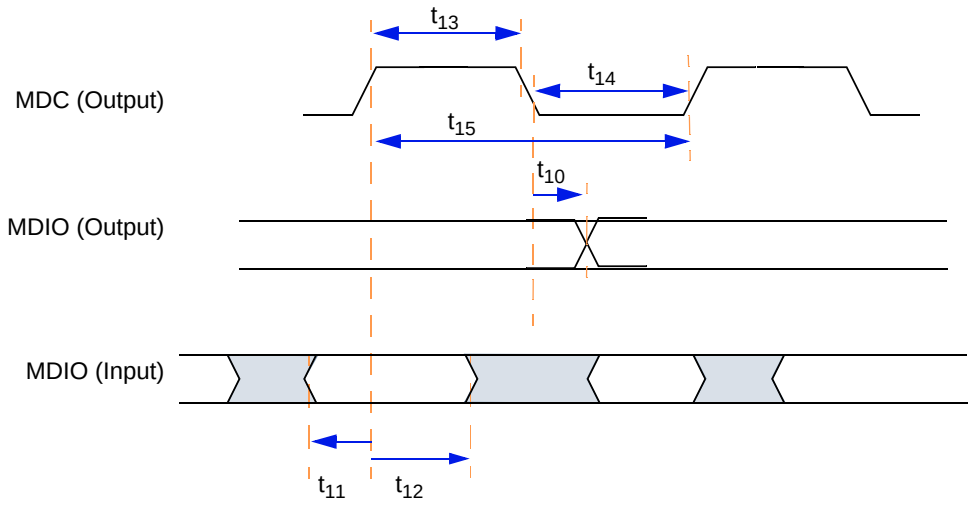

Figure 30. Ethernet Timing Diagram—MII Serial Management

1.3.11 USB

Table 35. Timing Specifications—USB Output Line

Sym	Description	Min	Max	Units	SpecID
1	USB Bit width(1)	83.3	667	ns	A10.1
2	Transceiver enable time	83.3	667	ns	A10.2
3	Signal falling time	—	7.9	ns	A10.3
4	Signal rising time	—	7.9	ns	A10.4

1 Defined in the USB config register, (12 Mbit/s or 1.5 Mbit/s mode).

NOTE

Output timing is specified at a nominal 50 pF load.

1.3.16 PSC

1.3.16.1 Codec Mode (8-,16-, 24-, and 32-bit)/I²S Mode

Table 42. Timing Specifications—8-, 16-, 24-, and 32-bit CODEC / I²S Master Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A15.1
2	Clock duty cycle	—	50	—	%(1)	A15.2
3	Bit Clock fall time	—	—	7.9	ns	A15.3
4	Bit Clock rise time	—	—	7.9	ns	A15.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A15.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A15.6
7	Output Data valid after clock edge	—	—	9.3	ns	A15.7
8	Input Data setup time	6.0	—	—	ns	A15.8

1 Bit Clock cycle time.

NOTE

Output timing is specified at a nominal 50 pF load.

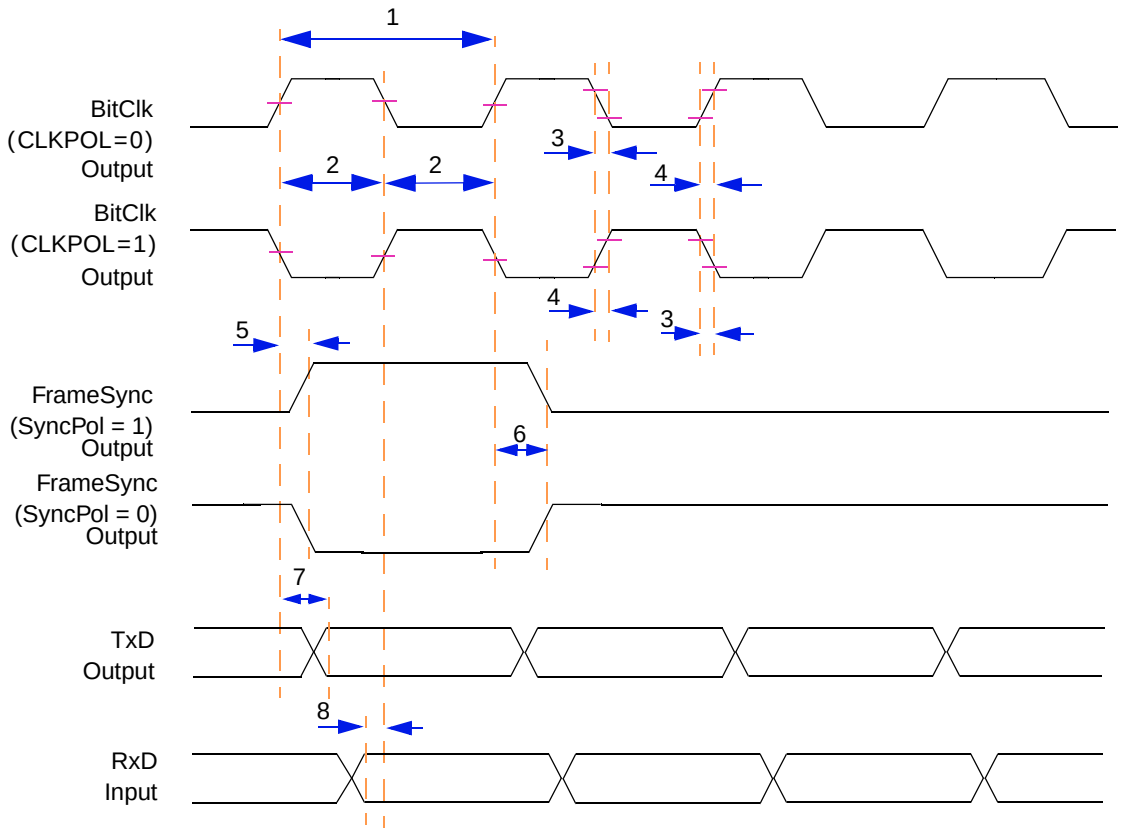

Figure 37. Timing Diagram — 8-, 16-, 24-, and 32-bit CODEC / I²S Master Mode

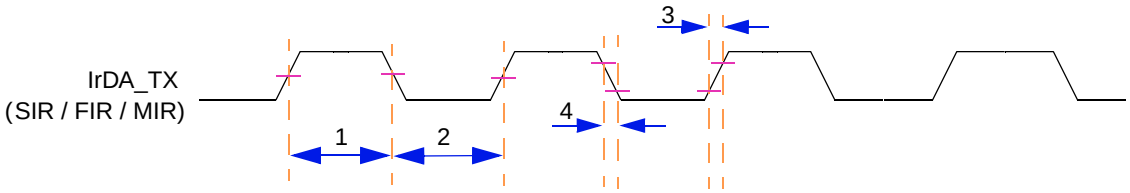

Figure 40. Timing Diagram — IrDA Transmit Line

1.3.16.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing is specified at a nominal 50 pF load.

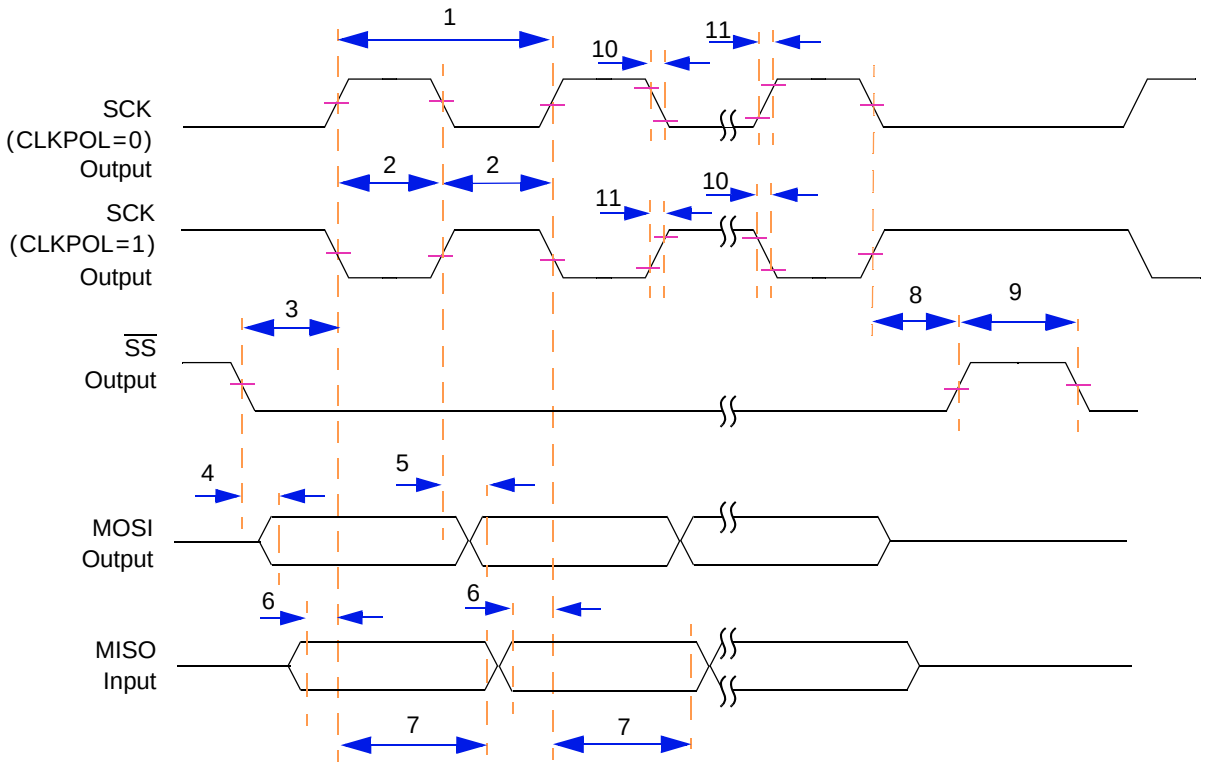

Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.38
3	Slave select clock delay	1.0	—	ns	A15.39
4	Input Data setup time	1.0	—	ns	A15.40
5	Input Data hold time	1.0	—	ns	A15.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A15.42
7	Output data valid after SCK	—	14.0	ns	A15.43
8	Slave disable lag time	0.0	—	ns	A15.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A15.45

NOTE

Output timing is specified at a nominal 50 pF load.

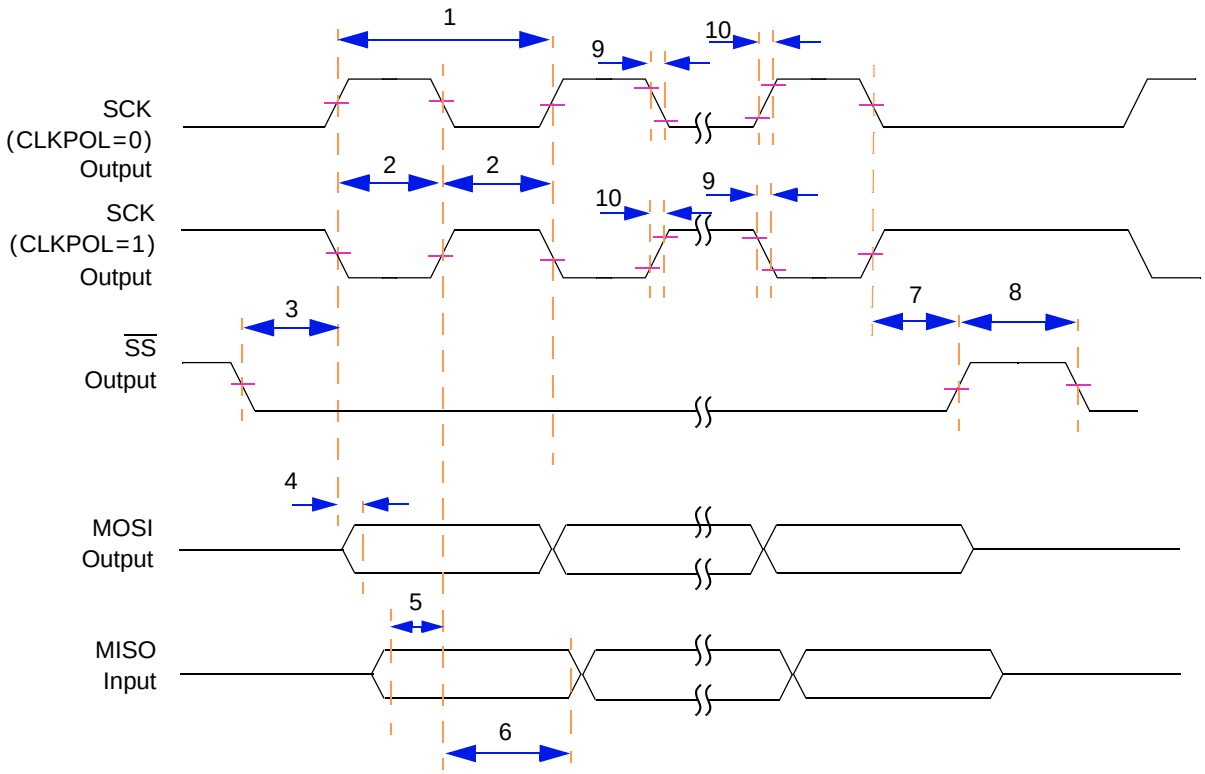

Figure 43. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.56
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.57
3	Slave select clock delay	0.0	—	ns	A15.58
4	Output data valid	—	14.0	ns	A15.59
5	Input Data setup time	2.0	—	ns	A15.60
6	Input Data hold time	1.0	—	ns	A15.61
7	Slave disable lag time	0.0	—	ns	A15.62
8	Minimum Sequential Transfer delay = 2 × IP-Bus clock cycle time	30.0	—	ns	A15.63

NOTE

Output timing is specified at a nominal 50 pF load.

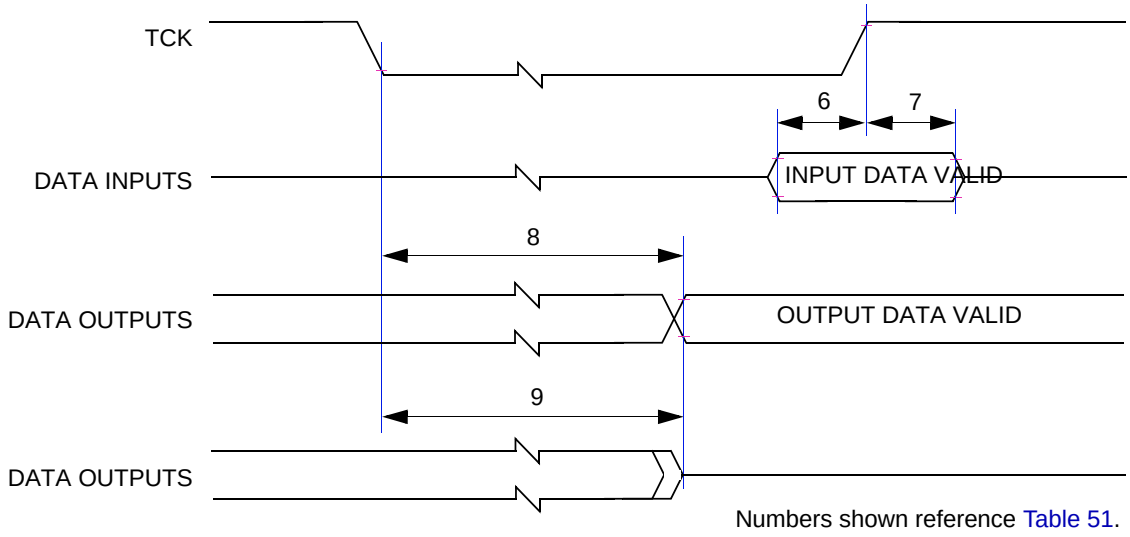

Figure 48. Timing Diagram—JTAG Boundary Scan

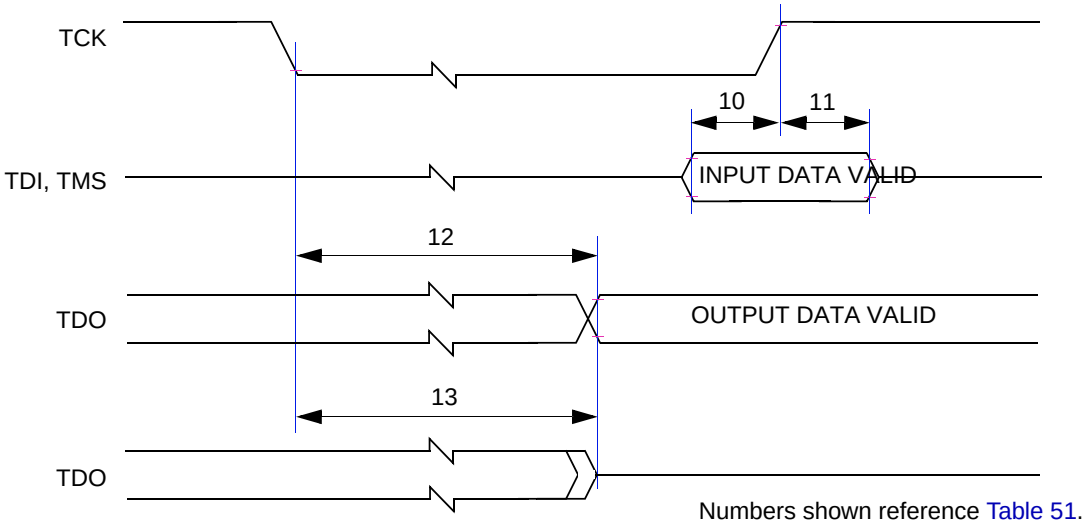

Figure 49. Timing Diagram—Test Access Port

2 Package Description

2.1 Package Parameters

The MPC5200B uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline: 27 mm x 27 mm
- Interconnects: 2
- Pitch: 1.27 mm

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
I2C_3	SDA	I/O	VDD_IO	DRV4	Schmitt	
PSC						
PSC1_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC1_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC1_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	Schmitt	
PSC1_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC2_0	TxD, Sdata_out, MOSI, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_1	RxD, Sdata_in, MISO, TX	I/O	VDD_IO	DRV4	TTL	
PSC2_2	Mclk, Sync, RTS	I/O	VDD_IO	DRV4	TTL	
PSC2_3	BitClk, SCK, CTS	I/O	VDD_IO	DRV4	Schmitt	
PSC2_4	Frame, $\overline{SS}$, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_0	USB_OE, TxDS, TX	I/O	VDD_IO	DRV4	TTL	
PSC3_1	USB_TXN, RxD, RX	I/O	VDD_IO	DRV4	TTL	
PSC3_2	USB_TXP, BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
PSC3_3	USB_RXD, Frame, $\overline{SS}$, CTS	I/O	VDD_IO	DRV4	TTL	
PSC3_4	USB_RXP, CD	I/O	VDD_IO	DRV4	TTL	
PSC3_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
PSC3_6	USB_PRTPWR, Mclk, MOSI	I/O	VDD_IO	DRV4	TTL	
PSC3_7	USB_SPEED. MISO	I/O	VDD_IO	DRV4	TTL	
PSC3_8	USB_SUPEND, $\overline{SS}$	I/O	VDD_IO	DRV4	TTL	
PSC3_9	USB_OVRCNT, SCK	I/O	VDD_IO	DRV4	TTL	
GPIO/TIMER						
GPIO_WKUP_6	MEM_CS1	I/O	VDD_MEM_IO	DRV16_MEM	TTL	PULLUP_MEM
GPIO_WKUP_7		I/O	VDD_IO	DRV8	TTL	
TIMER_0		I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
TIMER_1		I/O	VDD_IO	DRV4	TTL	
TIMER_2	MOSI	I/O	VDD_IO	DRV4	TTL	
TIMER_3	MISO	I/O	VDD_IO	DRV4	TTL	
TIMER_4	SS	I/O	VDD_IO	DRV4	TTL	
TIMER_5	SCK	I/O	VDD_IO	DRV4	TTL	
TIMER_6		I/O	VDD_IO	DRV4	TTL	
TIMER_7		I/O	VDD_IO	DRV4	TTL	
Clock						
SYS_XTAL_IN		Input	VDD_IO			
SYS_XTAL_OUT		Output	VDD_IO			
RTC_XTAL_IN		Input	VDD_IO			
RTC_XTAL_OUT		Output	VDD_IO			
Misc						
PORRESET		Input	VDD_IO	DRV4	Schmitt	
HRESET		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
SRESET		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
IRQ0		I/O	VDD_IO	DRV4	TTL	
IRQ1		I/O	VDD_IO	DRV4	TTL	
IRQ2		I/O	VDD_IO	DRV4	TTL	
IRQ3		I/O	VDD_IO	DRV4	TTL	
Test/Configuration						
SYS_PLL_TPA		I/O	VDD_IO	DRV4	TTL	
TEST_MODE_0		Input	VDD_IO	DRV4	TTL	
TEST_MODE_1		Input	VDD_IO	DRV4	TTL	
TEST_SEL_0		I/O	VDD_IO	DRV4	TTL	PULLUP
TEST_SEL_1		I/O	VDD_IO	DRV8	TTL	
JTAG_TCK	TCK	Input	VDD_IO	DRV4	Schmitt	PULLUP
JTAG_TDI	TDI	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDO	TDO	I/O	VDD_IO	DRV8	TTL	
JTAG_TMS	TMS	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TRST	TRST	Input	VDD_IO	DRV4	TTL	PULLUP
Power and Ground						
VDD_IO		—				