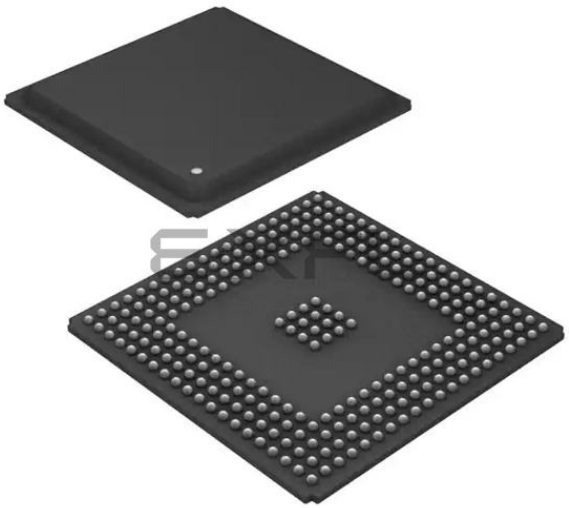

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5200vr400b

1.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	10	ms	O1.2

1.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

1.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	(1)	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	t_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	(2)	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	(3)	—	—	100	µs	O3.5

1 The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLKare reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

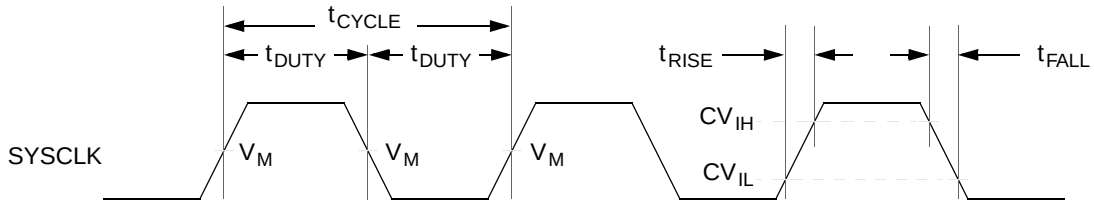

Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.(1)	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).(2)	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 —The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.

1.3.4 Resets

The MPC5200B has three reset pins:

- $\overline{\text{PORRESET}}$—Power on Reset
- $\overline{\text{HRESET}}$—Hard Reset
- $\overline{\text{SRESET}}$—Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200B inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

Table 14. Reset Pulse Width

Name	Description	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
$\overline{\text{PORRESET}}$	Power On Reset	$t_{VDD\_stable} + t_{up\_osc} + t_{lock}$	—	SYS_XTAL_IN	A3.1
$\overline{\text{HRESET}}$	Hardware Reset	4 clock cycles	—	SYS_XTAL_IN	A3.2
$\overline{\text{SRESET}}$	Software Reset	4 clock cycles	—	SYS_XTAL_IN	A3.3

For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.

The t_{VDD_stable} describes the time which is needed to get all power supplies stable.

For t_{lock}, refer to the Oscillator/PLL section of this specification for further details.

For t_{up_osc}, refer to the Oscillator/PLL section of this specification for further details.

Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.

The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 15. Reset Rise/Fall Timing

Description	Min	Max	Unit	SpecID
$\overline{\text{PORRESET}}$ fall time	—	1	ms	A3.4
$\overline{\text{PORRESET}}$ rise time	—	1	ms	A3.5
$\overline{\text{HRESET}}$ fall time	—	1	ms	A3.6
$\overline{\text{HRESET}}$ rise time	—	1	ms	A3.7
$\overline{\text{SRESET}}$ fall time	—	1	ms	A3.8
$\overline{\text{SRESET}}$ rise time	—	1	ms	A3.9

NOTE

Make sure that the $\overline{\text{PORRESET}}$ does not carry any glitches. The MPC5200B has no filter to prevent them from getting into the chip. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time. The assertion of $\overline{\text{HRESET}}$ becomes active at Power on Reset without any SYS_XTAL clock.

2) The interrupt latency descriptions in the table above are related to non competitive, non masked but enabled external interrupt sources. Take care of interrupt prioritization which may increase the latencies.

Because all external interrupt signals are synchronized into the internal processor bus clock domain, each of these signals has to exceed a minimum pulse width of more than one IP_CLK cycle.

Table 17. Minimum Pulse Width for External Interrupts to be Recognized

Name	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
All external interrupts (IRQs, GPIOs)	> 1 clock cycle	—	IP_CLK	A4.22

NOTES:

1) The frequency of the IP_CLK depends on the register settings in Clock Distribution Module. See the *MPC5200B User's Manual (MPC5200BUM)* for further information.

2) If the same interrupt occurs a second time while its interrupt service routine has not cleared the former one, the second interrupt is not recognized at all.

Besides synchronization, prioritization, and mapping the latency of an external interrupt to the start of its associated interrupt service routine also depends on the following conditions: To get a minimum interrupt service response time, it is recommended to enable the instruction cache and set up the maximum core clock, XL bus, and IP bus frequencies (depending on board design and programming). In addition, it is advisable to execute an interrupt handler, which has been implemented in assembly code.

1.3.6 SDRAM

1.3.6.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.25 + 0.4$	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.25 – 0.7$	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7

Table 24. Non-MUXed Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_{10}	DATA input setup before CS negation	8.5	—	ns	—	A7.12
t_{11}	DATA input hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(6)	A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	—	ns	(3)	A7.14
t_{13}	ACK negation after CS negation	—	t_{PCIck}	ns	(3)	A7.15
t_{14}	TS assertion before CS assertion	—	6.9	ns	(4)	A7.16
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	(4)	A7.17
t_{16}	TSIZ valid before CS assertion	t_{IPBIck}	—	ns	(5)	A7.18
t_{17}	TSIZ hold after CS negation	t_{IPBIck}	—	ns	(5)	A7.19
t_{18}	ACK change before PCI clock	—	2.0	ns	(1)	A7.20
t_{19}	ACK change after PCI clock	—	4.4	ns	(1)	A7.21

NOTES:

1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause the address to change before CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.
6. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

Table 25. Burst Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_9	DATA hold after rising edge of PCI clock	0	—	ns	—	A7.32
t_{10}	DATA hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(4)	A7.33
t_{11}	ACK assertion after CS assertion	—	(WS + 1) × t_{PCIck}	ns	—	A7.34
t_{12}	ACK negation before CS negation	—	7.0	ns	(3)	A7.35
t_{13}	ACK pulse width	4^{LB} × 2 × (32/DS) × t_{PCIck}	4^{LB} × 2 × (32/DS) × t_{PCIck}	ns	(2),(3)	A7.36
t_{14}	CS assertion after TS assertion	—	2.5	ns	—	A7.37
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	—	A7.38

NOTES:

1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => 4^1 × 2 × (32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1 + 10 + 32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.
4. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

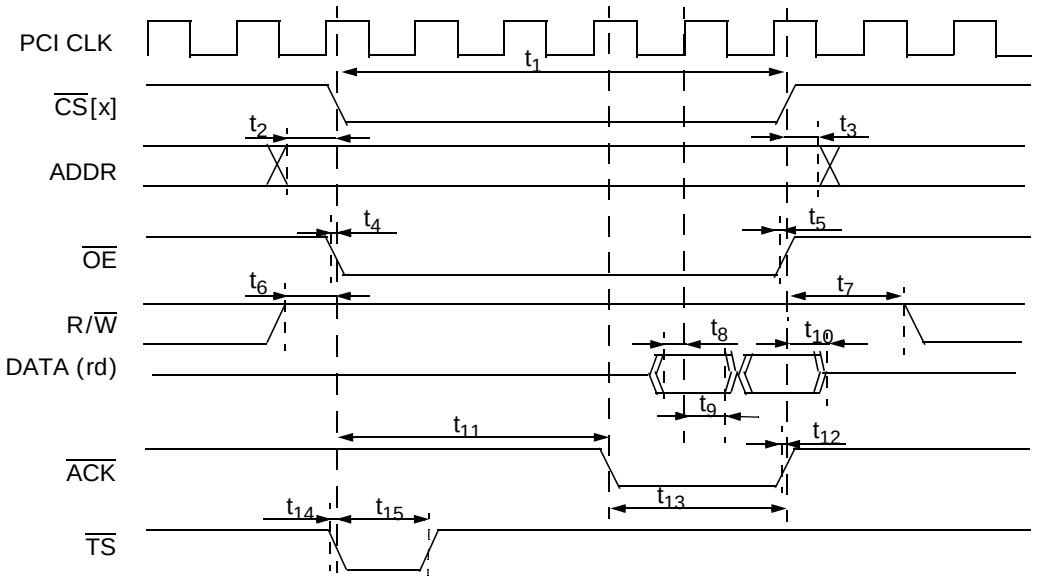

Figure 12. Timing Diagram—Burst Mode

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5200B operating frequency (IP bus clock frequency)
- Internal MPC5200B bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5200B. See the *MPC5200B User's Manual (MPC5200B)*.

NOTE

All output timing numbers are specified for nominal 50 pF loads.

Table 27. PIO Mode Timing Specifications

Sym	PIO Timing Parameter	Min/Max (ns)	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	SpecID
t_0	Cycle Time	min	600	383	240	180	120	A8.1
t_1	Address valid to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	70	50	30	30	25	A8.2
t_2	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width 16-bit 8-bit	min min	165 290	125 290	100 290	80 80	70 70	A8.3
t_{2i}	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ recovery time	min	—	—	—	70	25	A8.4
t_3	$\overline{\text{DIOW}}$ data setup	min	60	45	30	30	20	A8.5
t_4	$\overline{\text{DIOW}}$ data hold	min	30	20	15	10	10	A8.6
t_5	$\overline{\text{DIOR}}$ data setup	min	50	35	20	20	20	A8.7
t_6	$\overline{\text{DIOR}}$ data hold	min	5	5	5	5	5	A8.8
t_9	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to address valid hold	min	20	15	10	10	10	A8.9
t_A	IORDY setup	max	35	35	35	35	35	A8.10
t_B	IORDY pulse width	max	1250	1250	1250	1250	1250	A8.11

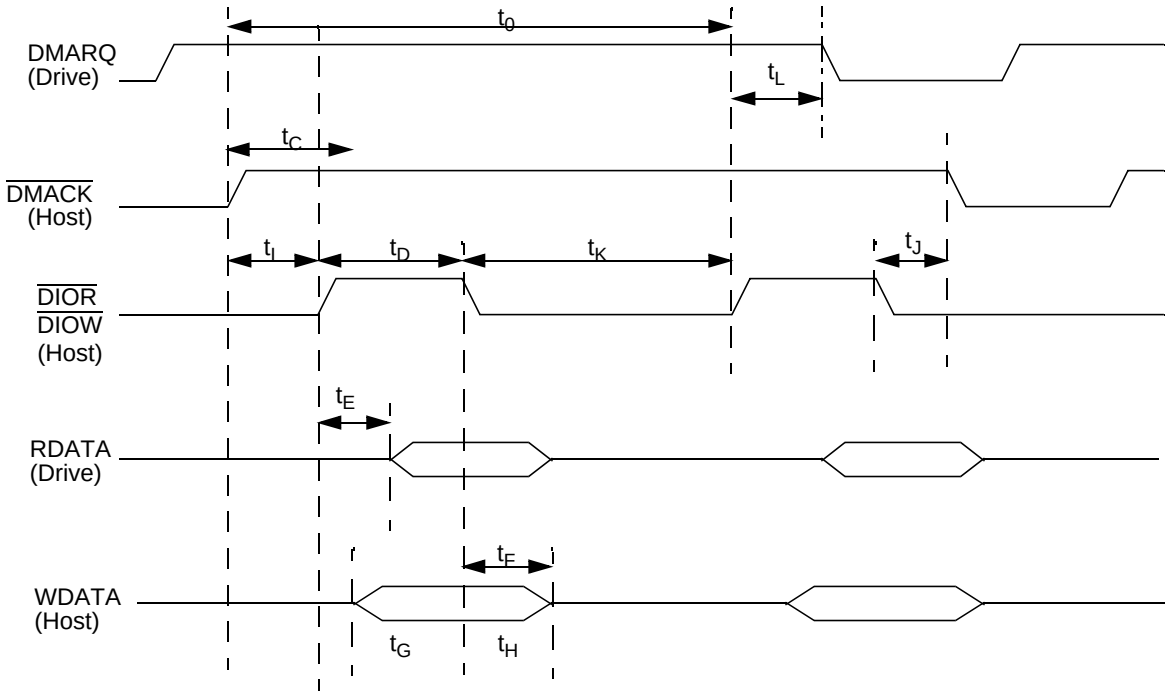

Figure 15. Multiword DMA Timing

NOTE

The direction of signal assertion is towards the top of the page, and the direction of negation is towards the bottom of the page, irrespective of the electrical properties of the signal.

Table 29. Ultra DMA Timing Specification

Sym	MODE 0 (ns)		MODE 1 (ns)		MODE 2 (ns)		Comment	SpecID
	Min	Max	Min	Max	Min	Max		
t_{CYC}	114	—	75	—	55	—	Cycle time allowing for asymmetry and clock variations from STROBE edge to STROBE edge	A8.26
t_{2CYC}	235	—	156	—	117	—	Two-cycle time allowing for clock variations, from rising edge to next rising edge or from falling edge to next falling edge of STROBE.	A8.27
t_{DS}	15	—	10	—	7	—	Data setup time at recipient.	A8.28
t_{DH}	5	—	5	—	5	—	Data hold time at recipient.	A8.29
t_{DVS}	70	—	48	—	34	—	Data valid setup time at sender, to STROBE edge.	A8.30
t_{DVH}	6	—	6	—	6	—	Data valid hold time at sender, from STROBE edge.	A8.31
t_{FS}	0	230	0	200	0	170	First STROBE time for drive to first negate DSTROBE from STOP during a data-in burst.	A8.32
t_{LI}	0	150	0	150	0	150	Limited Interlock time.	A8.33
t_{MLI}	20	—	20	—	20	—	Interlock time with minimum.	A8.34
t_{UI}	0	—	0	—	0	—	Unlimited interlock time.	A8.35

Table 30. Timing Specification ata_isolation

Sym	Description	Min	Max	Units	SpecID
1	ata_isolation setup time	7	—	IP Bus cycles	A8.48
2	ata_isolation hold time	—	19	IP Bus cycles	A8.49

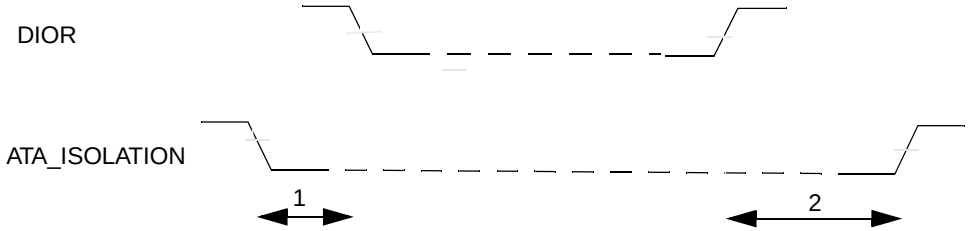

Figure 26. Timing Diagram—ATA-ISOLATION

1.3.10 Ethernet

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 31. MII Rx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	10	—	ns	A9.1
t_2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	10	—	ns	A9.2
t_3	RX_CLK pulse width high	35%	65%	RX_CLK Period(1)	A9.3
t_4	RX_CLK pulse width low	35%	65%	RX_CLK Period(1)	A9.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

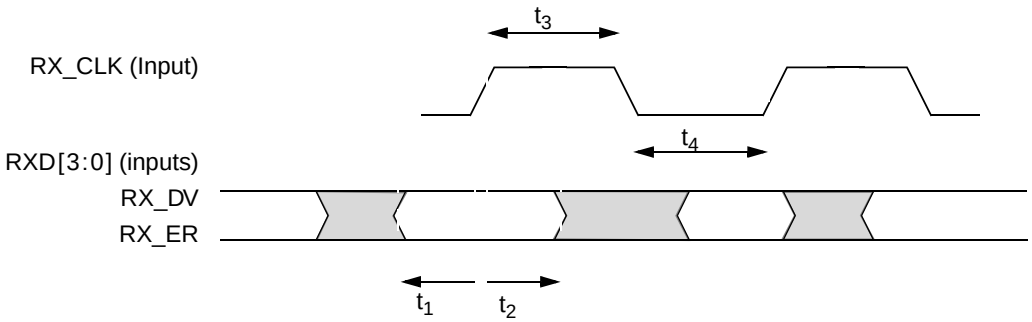

Figure 27. Ethernet Timing Diagram—MII Rx Signal

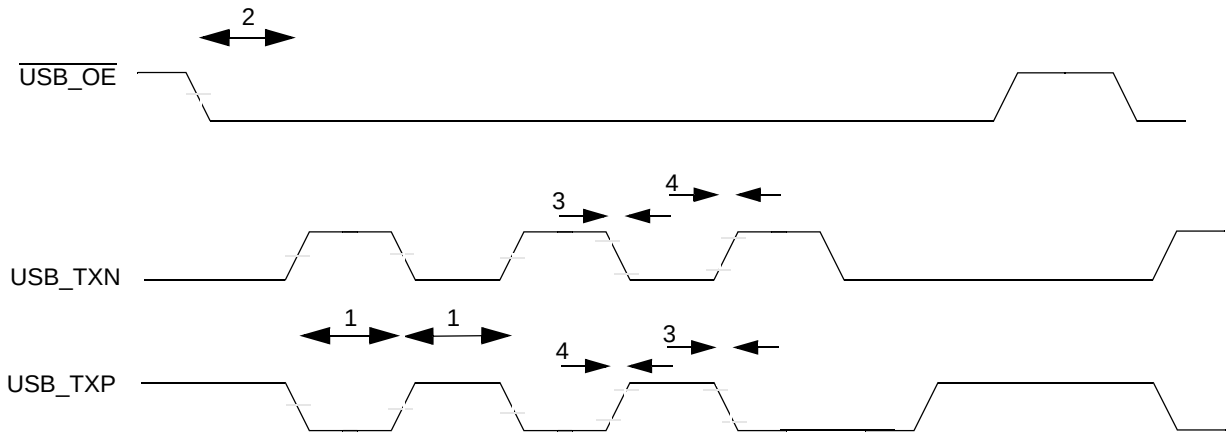

Figure 31. Timing Diagram—USB Output Line

1.3.12 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle(1)	A11.1
2	Clock high or low time	2	512	IP-Bus Cycle(1)	A11.2
3	Slave select to clock delay	15.0	—	ns	A11.3
4	Output Data valid after Slave Select ($\overline{SS}$)	—	20.0	ns	A11.4
5	Output Data valid after SCK	—	20.0	ns	A11.5
6	Input Data setup time	20.0	—	ns	A11.6
7	Input Data hold time	20.0	—	ns	A11.7
8	Slave disable lag time	15.0	—	ns	A11.8
9	Sequential transfer delay	1	—	IP-Bus Cycle(1)	A11.9
10	Clock falling time	—	7.9	ns	A11.10
11	Clock rising time	—	7.9	ns	A11.11

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

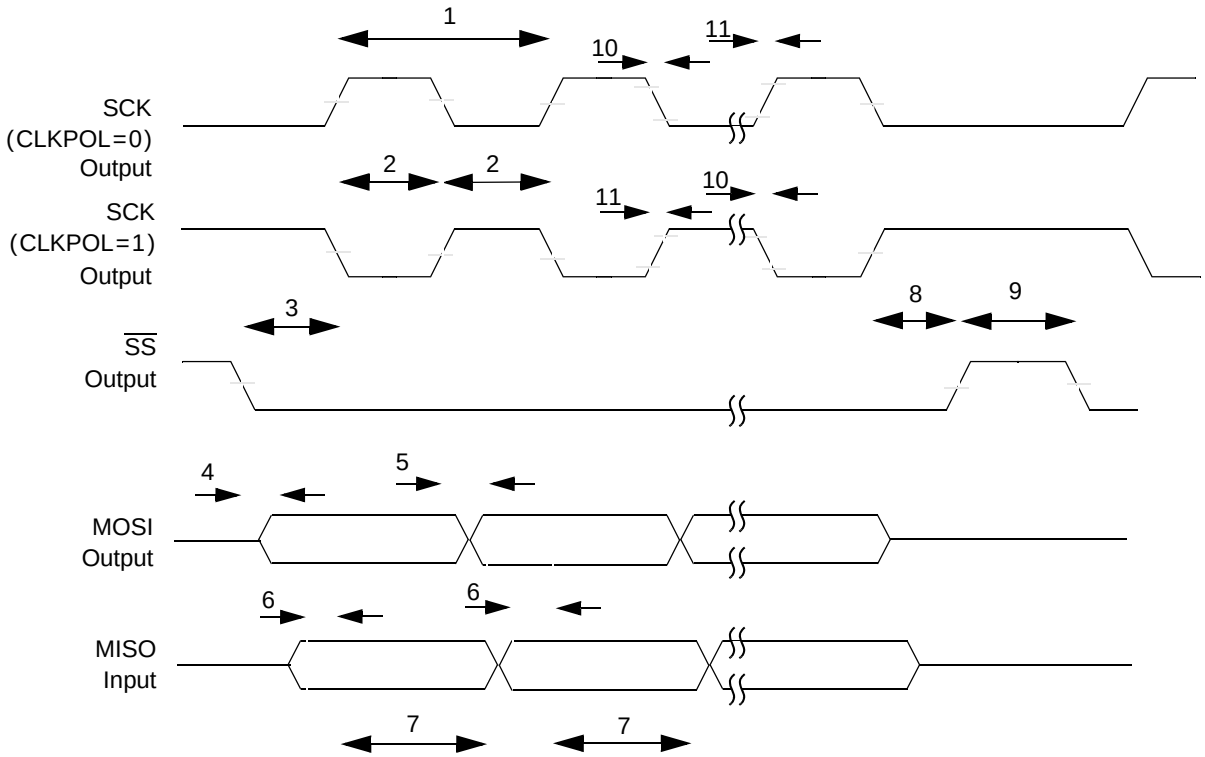

Figure 32. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 37. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle(1)	A11.12
2	Clock high or low time	2	512	IP-Bus Cycle(1)	A11.13
3	Slave select to clock delay	15.0	—	ns	A11.14
4	Output Data valid after Slave Select ($\overline{SS}$)	—	50.0	ns	A11.15
5	Output Data valid after SCK	—	50.0	ns	A11.16
6	Input Data setup time	50.0	—	ns	A11.17
7	Input Data hold time	0.0	—	ns	A11.18
8	Slave disable lag time	15.0	—	ns	A11.19
9	Sequential Transfer delay	1	—	IP-Bus Cycle(1)	A11.20

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

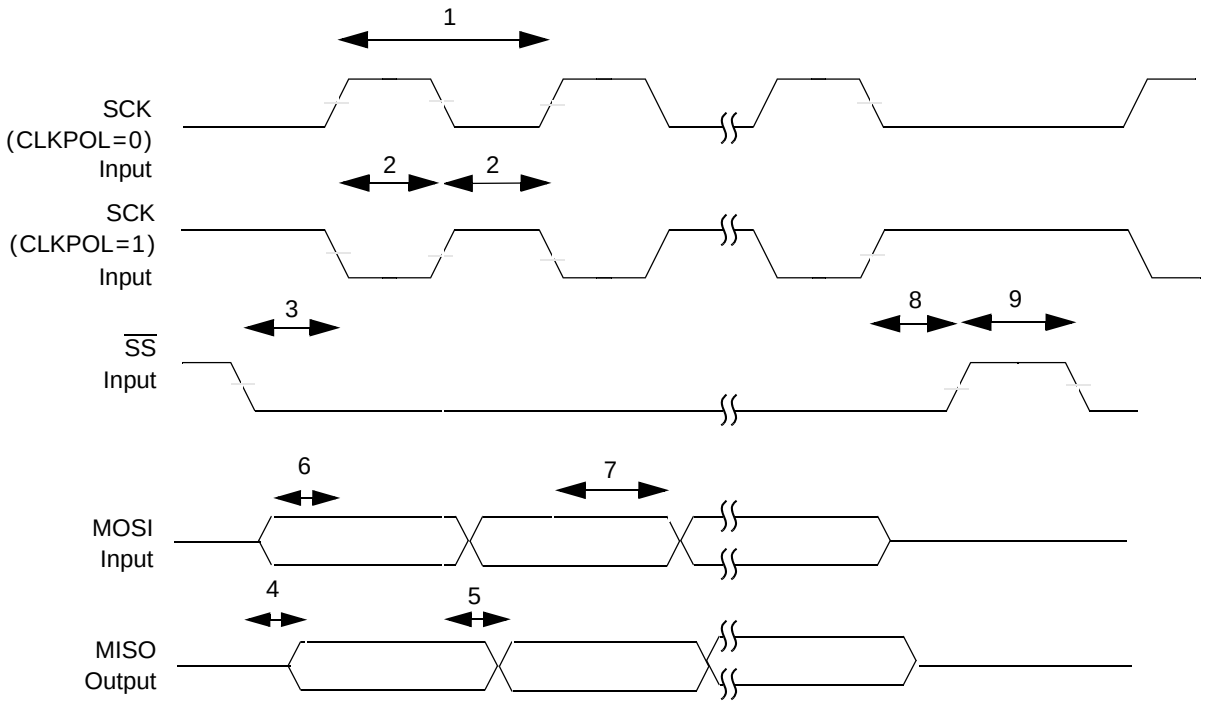

Figure 33. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 38. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.21
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.22
3	Slave select to clock delay	15.0	—	ns	A11.23
4	Output data valid	—	20.0	ns	A11.24
5	Input Data setup time	20.0	—	ns	A11.25
6	Input Data hold time	20.0	—	ns	A11.26
7	Slave disable lag time	15.0	—	ns	A11.27
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.28
9	Clock falling time	—	7.9	ns	A11.29
10	Clock rising time	—	7.9	ns	A11.30

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

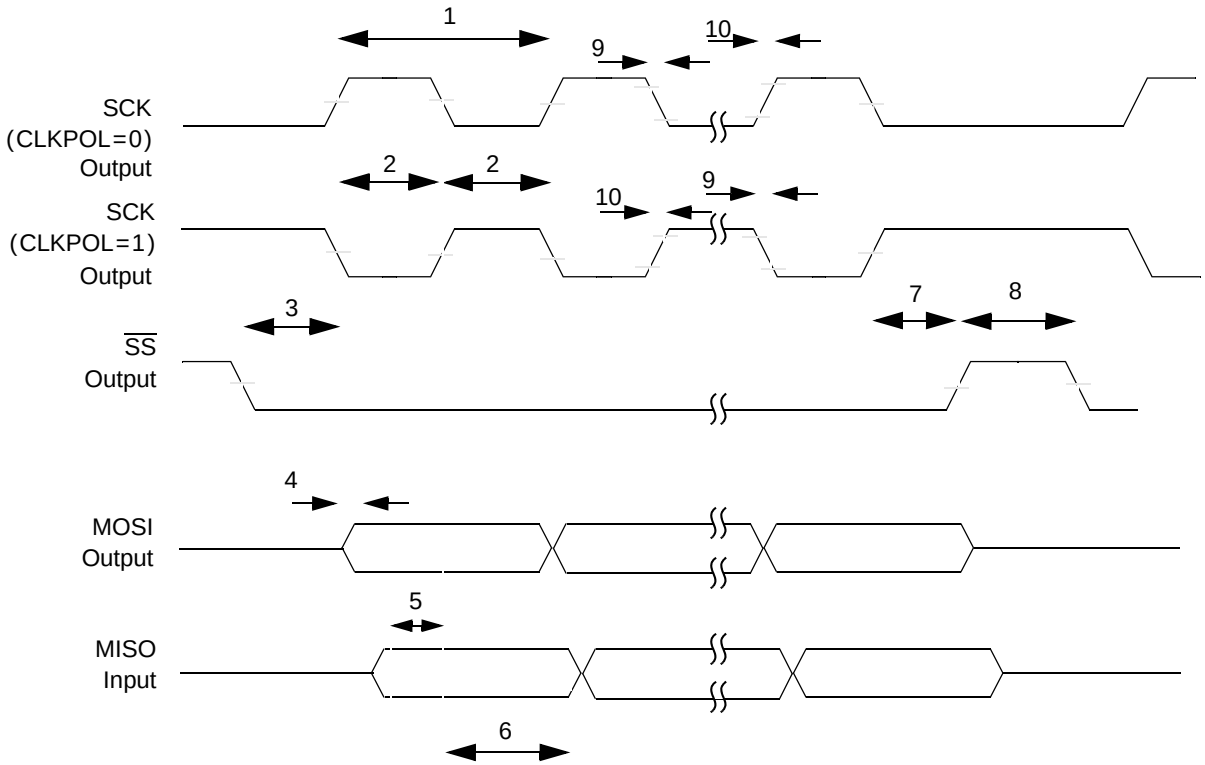

Figure 34. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 39. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.31
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.32
3	Slave select to clock delay	15.0	—	ns	A11.33
4	Output data valid	—	50.0	ns	A11.34
5	Input Data setup time	50.0	—	ns	A11.35
6	Input Data hold time	0.0	—	ns	A11.36
7	Slave disable lag time	15.0	—	ns	A11.37
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.38

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

1.3.16 PSC

1.3.16.1 Codec Mode (8-,16-, 24-, and 32-bit)/I²S Mode

Table 42. Timing Specifications—8-, 16-, 24-, and 32-bit CODEC / I²S Master Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A15.1
2	Clock duty cycle	—	50	—	%(1)	A15.2
3	Bit Clock fall time	—	—	7.9	ns	A15.3
4	Bit Clock rise time	—	—	7.9	ns	A15.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A15.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A15.6
7	Output Data valid after clock edge	—	—	9.3	ns	A15.7
8	Input Data setup time	6.0	—	—	ns	A15.8

1 Bit Clock cycle time.

NOTE

Output timing is specified at a nominal 50 pF load.

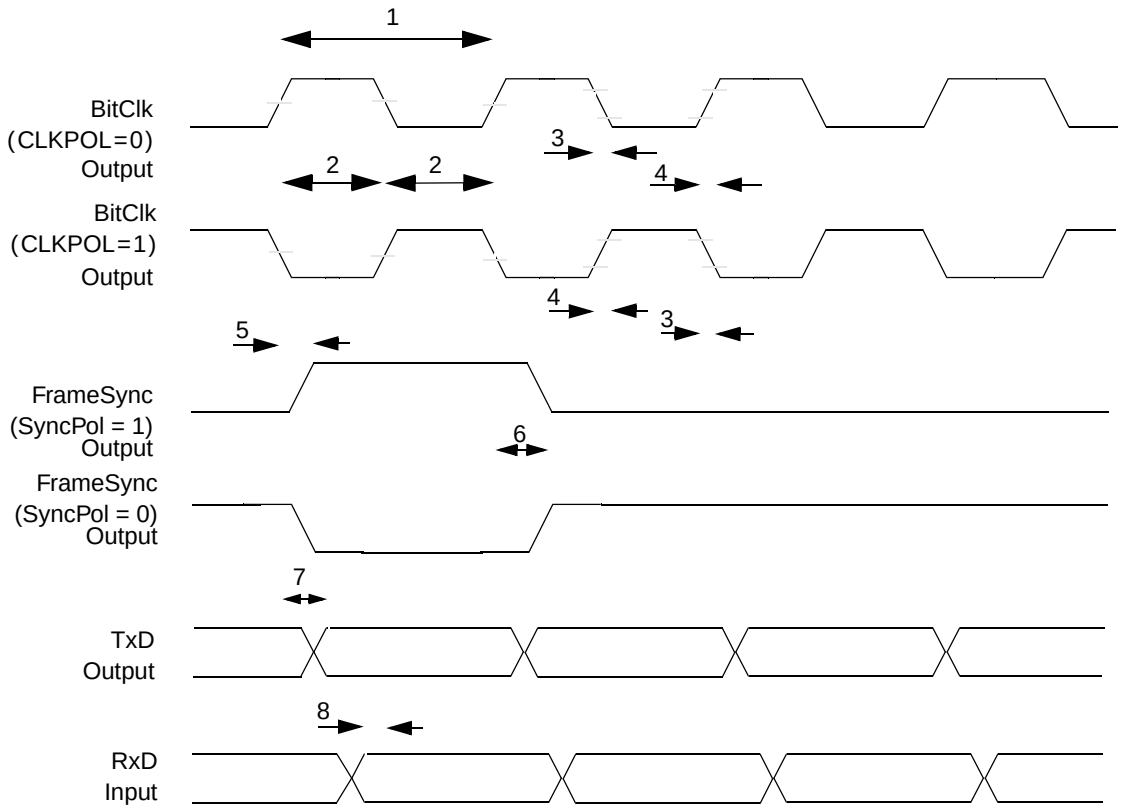

Figure 37. Timing Diagram — 8-, 16-, 24-, and 32-bit CODEC / I²S Master Mode

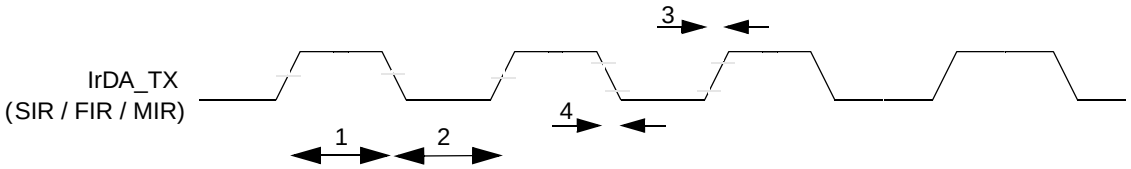

Figure 40. Timing Diagram — IrDA Transmit Line

1.3.16.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing is specified at a nominal 50 pF load.

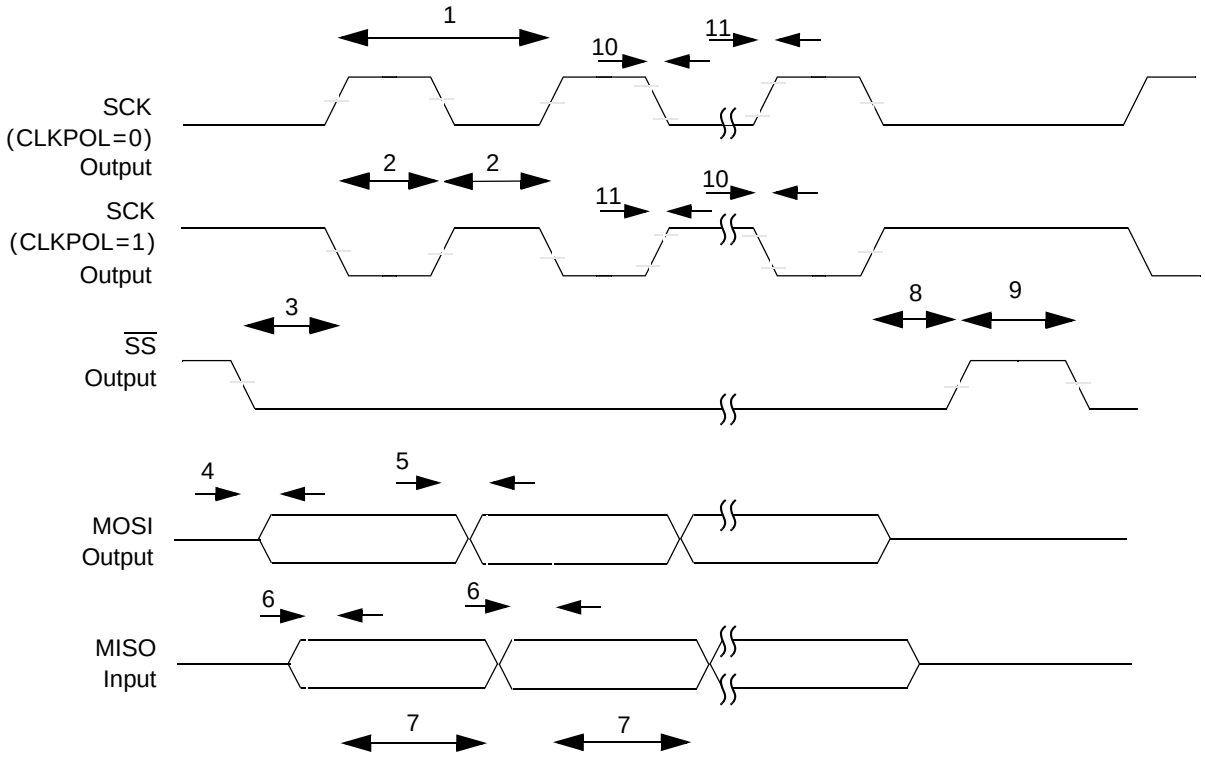

Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.38
3	Slave select clock delay	1.0	—	ns	A15.39
4	Input Data setup time	1.0	—	ns	A15.40
5	Input Data hold time	1.0	—	ns	A15.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A15.42
7	Output data valid after SCK	—	14.0	ns	A15.43
8	Slave disable lag time	0.0	—	ns	A15.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A15.45

NOTE

Output timing is specified at a nominal 50 pF load.

1.3.18 IEEE 1149.1 (JTAG) AC Specifications

Table 51. JTAG Timing Specification

Sym	Characteristic	Min	Max	Unit	SpecID
—	TCK frequency of operation.	0	25	MHz	A17.1
1	TCK cycle time.	40	—	ns	A17.2
2	TCK clock pulse width measured at 1.5V.	1.08	—	ns	A17.3
3	TCK rise and fall times.	0	3	ns	A17.4
4	$\overline{\text{TRST}}$ setup time to tck falling edge(1).	10	—	ns	A17.5
5	$\overline{\text{TRST}}$ assert time.	5	—	ns	A17.6
6	Input data setup time(2).	5	—	ns	A17.7
7	Input data hold time(2).	15	—	ns	A17.8
8	TCK to output data valid(3).	0	30	ns	A17.9
9	TCK to output high impedance(3).	0	30	ns	A17.10
10	TMS, TDI data setup time.	5	—	ns	A17.11
11	TMS, TDI data hold time.	1	—	ns	A17.12
12	TCK to TDO data valid.	0	15	ns	A17.13
13	TCK to TDO high impedance.	0	15	ns	A17.14

1 $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

2 Non-test, other than TDI and TMS, signal input timing with respect to TCK.

3 Non-test, other than TDO, signal output timing with respect to TCK.

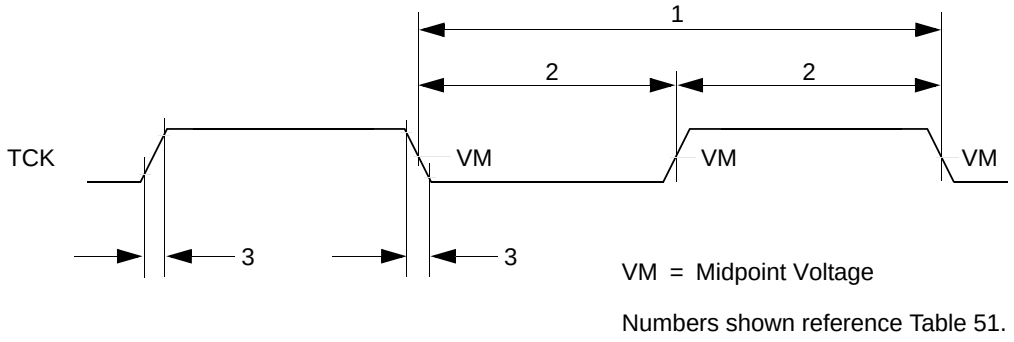

Figure 46. Timing Diagram—JTAG Clock Input

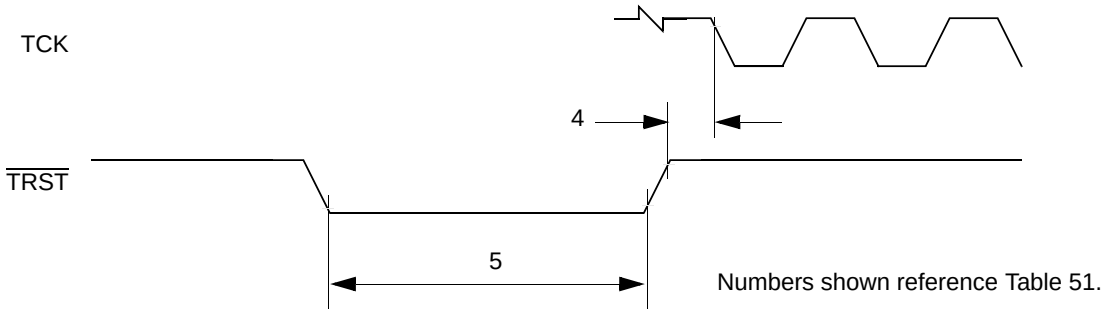

Figure 47. Timing Diagram—JTAG TRST

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
TIMER_1		I/O	VDD_IO	DRV4	TTL	
TIMER_2	MOSI	I/O	VDD_IO	DRV4	TTL	
TIMER_3	MISO	I/O	VDD_IO	DRV4	TTL	
TIMER_4	SS	I/O	VDD_IO	DRV4	TTL	
TIMER_5	SCK	I/O	VDD_IO	DRV4	TTL	
TIMER_6		I/O	VDD_IO	DRV4	TTL	
TIMER_7		I/O	VDD_IO	DRV4	TTL	
Clock						
SYS_XTAL_IN		Input	VDD_IO			
SYS_XTAL_OUT		Output	VDD_IO			
RTC_XTAL_IN		Input	VDD_IO			
RTC_XTAL_OUT		Output	VDD_IO			
Misc						
PORRESET		Input	VDD_IO	DRV4	Schmitt	
HRESET		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
SRESET		I/O	VDD_IO	DRV8_OD[1]	Schmitt	
IRQ0		I/O	VDD_IO	DRV4	TTL	
IRQ1		I/O	VDD_IO	DRV4	TTL	
IRQ2		I/O	VDD_IO	DRV4	TTL	
IRQ3		I/O	VDD_IO	DRV4	TTL	
Test/Configuration						
SYS_PLL_TPA		I/O	VDD_IO	DRV4	TTL	
TEST_MODE_0		Input	VDD_IO	DRV4	TTL	
TEST_MODE_1		Input	VDD_IO	DRV4	TTL	
TEST_SEL_0		I/O	VDD_IO	DRV4	TTL	PULLUP
TEST_SEL_1		I/O	VDD_IO	DRV8	TTL	
JTAG_TCK	TCK	Input	VDD_IO	DRV4	Schmitt	PULLUP
JTAG_TDI	TDI	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TDO	TDO	I/O	VDD_IO	DRV8	TTL	
JTAG_TMS	TMS	Input	VDD_IO	DRV4	TTL	PULLUP
JTAG_TRST	TRST	Input	VDD_IO	DRV4	TTL	PULLUP
Power and Ground						
VDD_IO		—				

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200B.

3.4.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

3.4.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5200B functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200B I/O Pin	BDM Connector	Internal Pull Up/Down	External Pull Up/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset	—	10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset	—	10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O
8	—	N/C	—	—	—
7	JTAG_TCK	tck	100k Pull-Up	10k Pull-Up	O
6	—	VDD[2]	—	—	—
5	—	halted[3]	—	—	I
4	JTAG_TRST	trst	100k Pull-Up	10k Pull-Up	O
3	JTAG_TDI	tdi	100k Pull-Up	10k Pull-Up	O
2	—	qack[4]	—	—	O
1	JTAG_TDO	tdo	—	—	I

1 With respect to the emulator tool's perspective, Input is really an output from the embedded e300 core and output is really an input to the core.

2 From the board under test, power sense for chip power.

3 HALTED is not available from e300 core.

4 Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5200B internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector, which accesses the JTAG interface and which needs to reset the JTAG module, simply wiring $\overline{\text{JTAG\_TRST}}$ and $\overline{\text{PORRESET}}$ is not recommended.

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