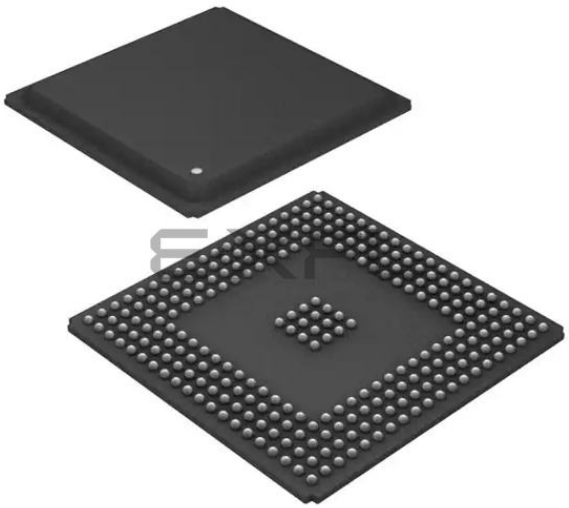

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5200vr400br2

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor — memory I/O buffers	PULLUP_MEM $VDD\_IO\_MEM_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin(3)		I_{CS}	–1.0	1.0	mA	D3.23
Capacitance	Vin = 0 V, f = 1 MHz	C_{in}	—	15	pF	D3.24

1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.

3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200B Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3 V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3 V	8	8	mA	D3.26
DRV8_OD	VDD_IO = 3.3 V	—	8	mA	D3.27
DRV16_MEM	VDD_IO_MEM = 3.3 V	16	16	mA	D3.28
DRV16_MEM	VDD_IO_MEM = 2.5 V	16	16	mA	D3.29
PCI	VDD_IO = 3.3 V	16	16	mA	D3.30

Table 6. Power Dissipation

Core Power Supply (VDD_CORE)					
Mode	SYS_XTAL/XLB/PCI/IPB/CORE (MHz)		Unit	Notes	SpecID
	33/66/33/33/264	33/132/66/132/396			
	Typ	Typ			
Operational	727.5	1080	mW	(1),(2)	D5.1
Doze	—	600	mW	(1),(3)	D5.2
Nap	—	225	mW	(1),(4)	D5.3
Sleep	—	225	mW	(1),(5)	D5.4
Deep-Sleep	52.5	52.5	mW	(1),(6)	D5.5
PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)					
Mode	**Typ**		**Unit**	**Notes**	
Typical	2		mW	(7)	D5.6
Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8])					
Mode	**Typ**		**Unit**	**Notes**	
Typical	33		mW	(9)	D5.7

1 Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 °C

2 Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.

3 Doze power is measured with the e300 core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

4 Nap power is measured with the e300 core in Nap mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

5 Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

6 Deep-Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL, Core PLL and all other system modules are inactive

7 Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 °C

8 IO power figures given in the table represent the worst case scenario. For the VDD_MEM_IO rail connected to 2.5 V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3 V.

9 Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD\_MEM\_IO_{SDR}$= 3.3 V, Tj = 25 °C

1.1.6 Thermal Characteristics

Table 7. Thermal Resistance Data

Rating	Board Layers	Sym	Value	Unit	Notes	SpecID
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	30	°C/W	(1),(2)	D6.1
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	(1),(3)	D6.2
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W	(1),(3)	D6.3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	19	°C/W	(1),(3)	D6.4
Junction to Board	—	$R_{\theta JB}$	14	°C/W	(4)	D6.5
Junction to Case	—	$R_{\theta JC}$	8	°C/W	(5)	D6.6
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	(6)	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

1.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

1.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	10	ms	O1.2

1.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

1.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	(1)	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	t_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	(2)	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	(3)	—	—	100	µs	O3.5

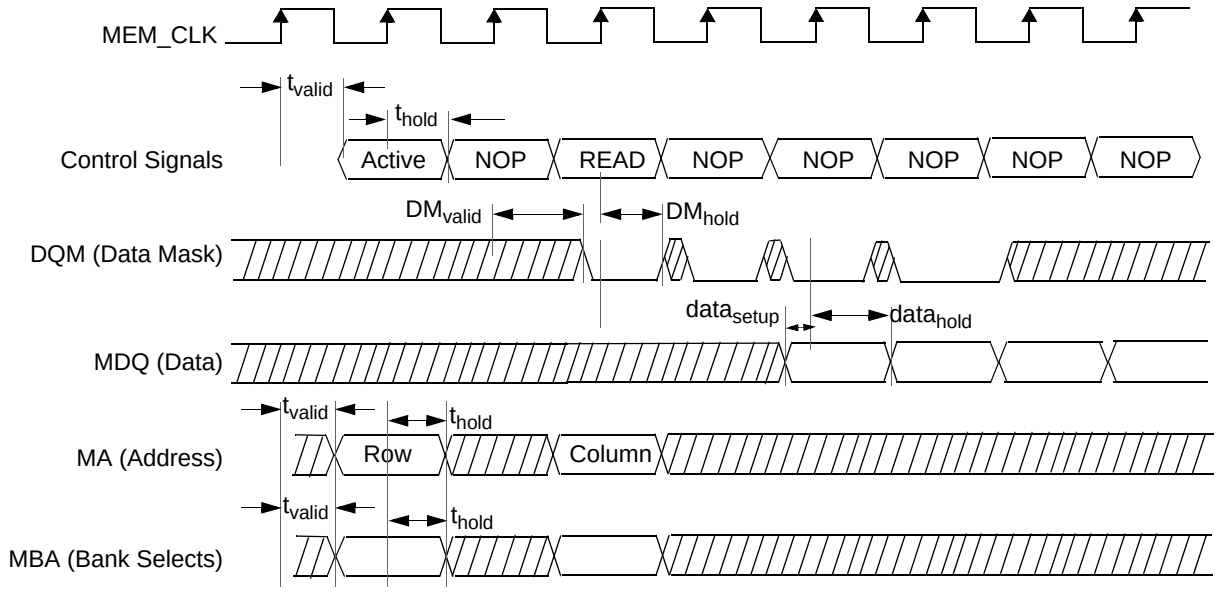
1 The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLKare reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

1.3.6.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the MEM_CLK from the Memory Controller and captured on the MEM_CLK clock at the memory device.

Table 19. Standard SDRAM Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.8
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.9
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.10
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.25 + 0.4$	ns	A5.11
DM_{hold}	DQM hold after rising edge of Mem_clk	$t_{mem\_clk} \times 0.25 – 0.7$	—	ns	A5.12
$data_{valid}$	MDQ valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.75 + 0.4$	ns	A5.13
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.75 – 0.7$	—	ns	A5.14

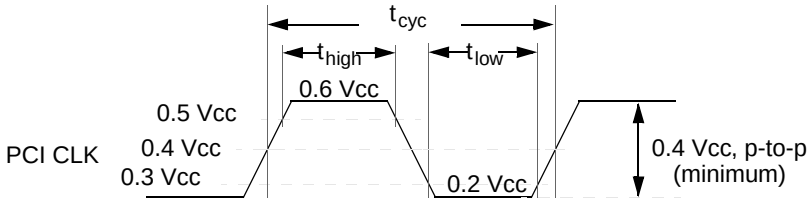


Figure 9. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{cyc}	PCI CLK Cycle Time	15	30	30	—	ns	(1),(3)	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	—	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	—	A6.3
—	PCI CLK Slew Rate	1.5	4	1	4	V/ns	(2)	A6.4
—	PCI Clock Jitter (peak to peak)	—	200	—	200	ps	—	—

NOTES:
1. In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{val}	CLK to Signal Valid Delay — bused signals	2	6	2	11	ns	(1),(2),(3)	A6.5
t_{val}(ptp)	CLK to Signal Valid Delay — point to point	2	6	2	12	ns	(1),(2),(3)	A6.6
t_{on}	Float to Active Delay	2	—	2	—	ns	(1)	A6.7
t_{off}	Active to Float Delay		14		28	ns	(1)	A6.8
t_{su}	Input Setup Time to CLK — bused signals	3	—	7	—	ns	(3),(4)	A6.9
t_{su}(ptp)	Input Setup Time to CLK — point to point	5	—	10,12	—	ns	(3),(4)	A6.10
t_h	Input Hold Time from CLK	0	—	0	—	ns	(4)	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

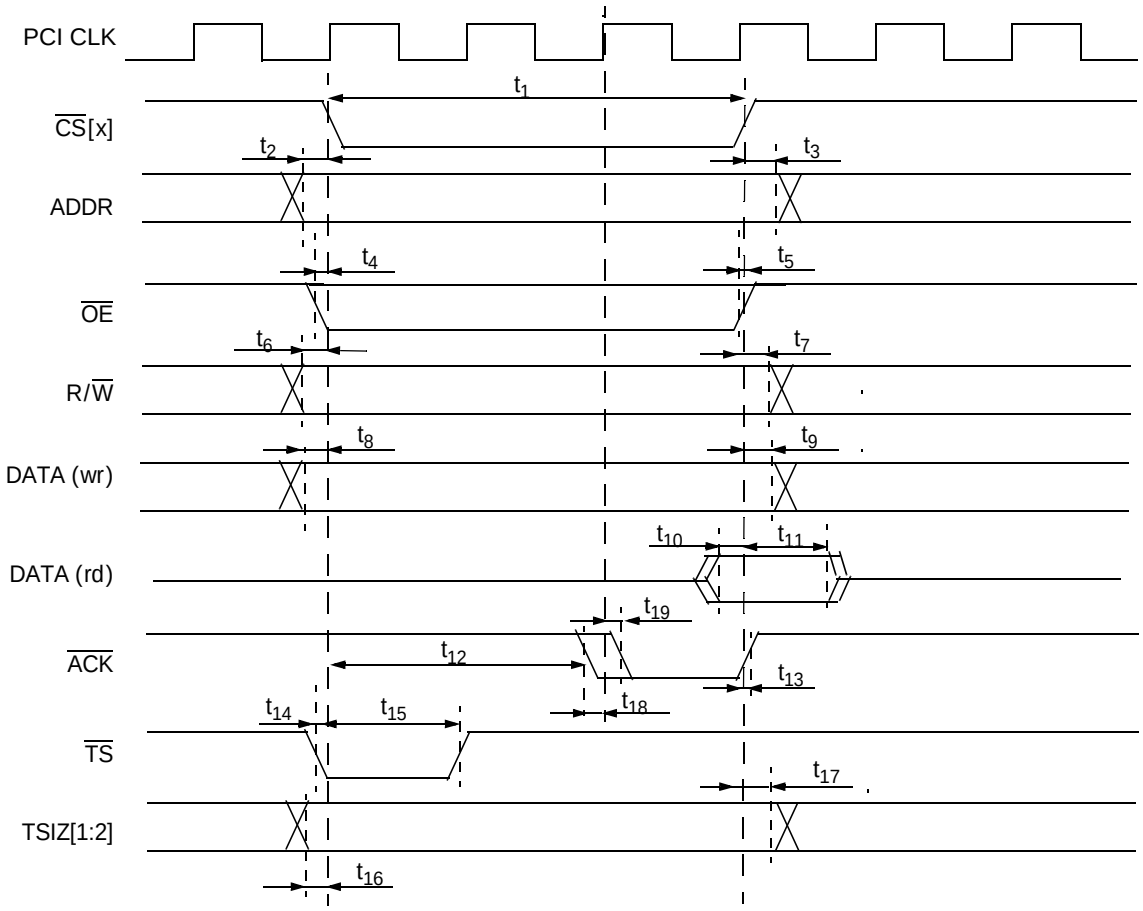


Figure 11. Timing Diagram—Non-MUXed Mode

1.3.8.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.22
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.23
t_1	CS pulse width	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	ns	(1),(2)	A7.24
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.25
t_3	ADDR hold after CS negation	–0.7	—	ns	—	A7.26
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.27
t_5	OE negation before CS negation	—	2.7	ns	—	A7.28
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.29
t_7	RW hold after CS negation	t_{PCIck}	—	ns	—	A7.30
t_8	DATA setup before rising edge of PCI clock	3.6	—	ns	—	A7.31

Table 25. Burst Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_9	DATA hold after rising edge of PCI clock	0	—	ns	—	A7.32
t_{10}	DATA hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(4)	A7.33
t_{11}	ACK assertion after CS assertion	—	(WS + 1) × t_{PCIck}	ns	—	A7.34
t_{12}	ACK negation before CS negation	—	7.0	ns	(3)	A7.35
t_{13}	ACK pulse width	4^{LB} × 2 × (32/DS) × t_{PCIck}	4^{LB} × 2 × (32/DS) × t_{PCIck}	ns	(2),(3)	A7.36
t_{14}	CS assertion after TS assertion	—	2.5	ns	—	A7.37
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	—	A7.38

NOTES:

1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => 4^1 × 2 × (32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1 + 10 + 32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.
4. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

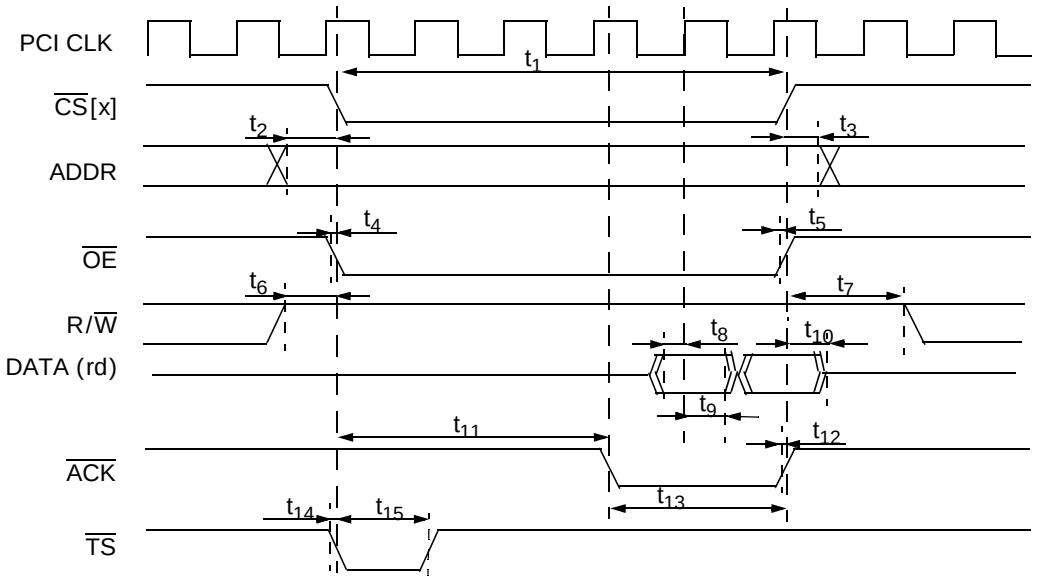


Figure 12. Timing Diagram—Burst Mode

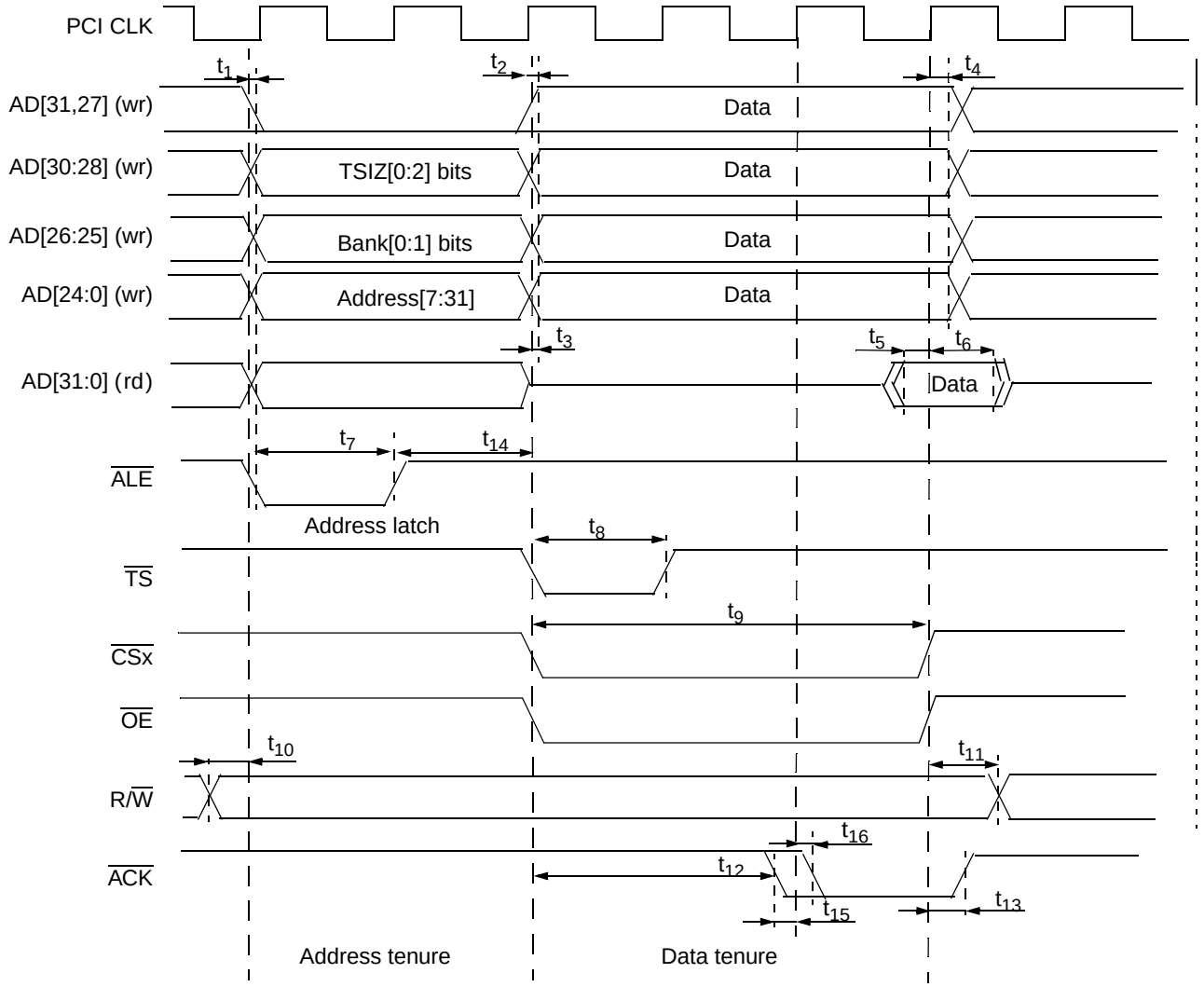


Figure 13. Timing Diagram—MUXed Mode

1.3.9 ATA

The MPC5200B ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5200B User's Manual (MPC5200BUM)*.

The MPC5200B ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold time beyond that required by the ATA-4 specification.

Table 32. MII Tx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns	A9.5
t_6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A9.6
t_7	TX_CLK pulse width high	35%	65%	TX_CLK Period(1)	A9.7
t_8	TX_CLK pulse width low	35%	65%	TX_CLK Period(1)	A9.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

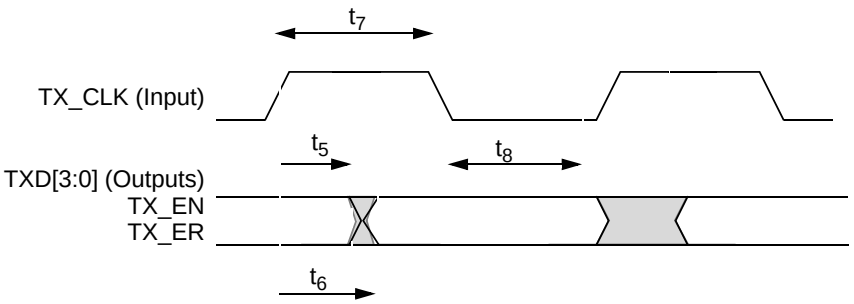


Figure 28. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A9.9

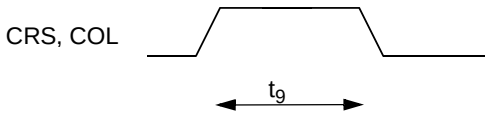


Figure 29. Ethernet Timing Diagram—MII Async

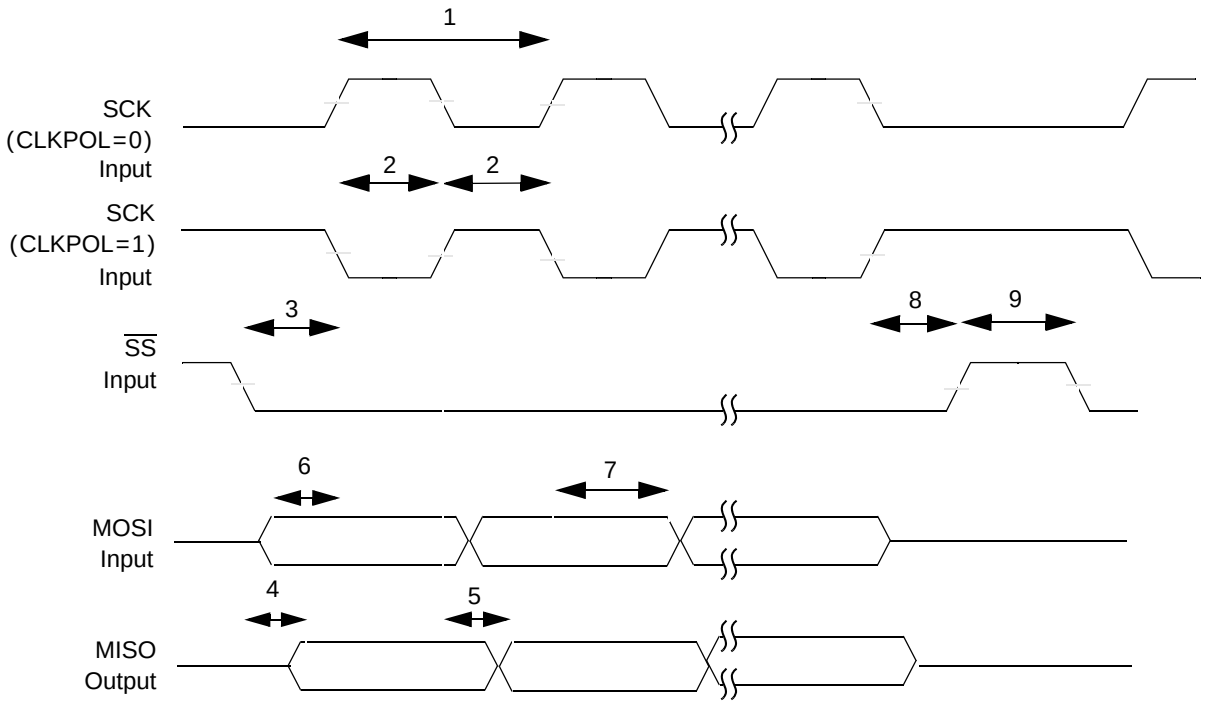


Figure 33. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 38. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.21
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.22
3	Slave select to clock delay	15.0	—	ns	A11.23
4	Output data valid	—	20.0	ns	A11.24
5	Input Data setup time	20.0	—	ns	A11.25
6	Input Data hold time	20.0	—	ns	A11.26
7	Slave disable lag time	15.0	—	ns	A11.27
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.28
9	Clock falling time	—	7.9	ns	A11.29
10	Clock rising time	—	7.9	ns	A11.30

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

Table 41. I²C Output Timing Specifications—SCL and SDA

Sym	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[3]	A13.8
2[1]	Clock low time	10	—	IP-Bus Cycle[3]	A13.9
3[2]	SCL/SDA rise time	—	7.9	ns	A13.10
4[1]	Data hold time	7	—	IP-Bus Cycle[3]	A13.11
5[1]	SCL/SDA fall time	—	7.9	ns	A13.12
6[1]	Clock high time	10	—	IP-Bus Cycle[3]	A13.13
7[1]	Data setup time	2	—	IP-Bus Cycle[3]	A13.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[3]	A13.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[3]	A13.16

1 Programming IFDR with the maximum frequency (IFDR=0x20) results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

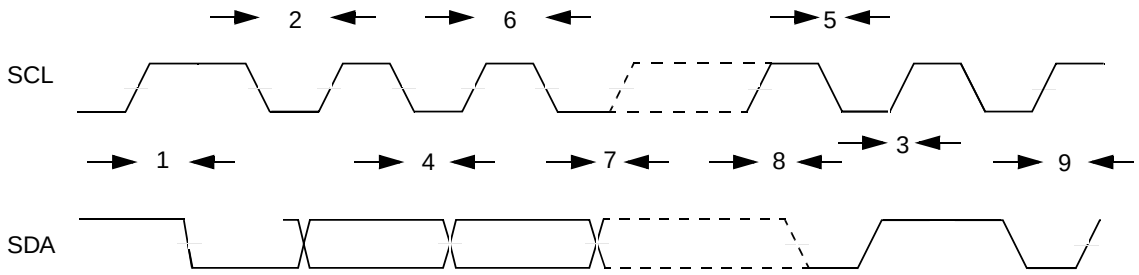


Figure 36. Timing Diagram—I²C Input/Output

1.3.15 J1850

See the *MPC5200B User's Manual (MPC5200BUM)*.

Table 43. Timing Specifications — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	40.0	—	—	ns	A15.9
2	Clock duty cycle	—	50	—	%(1)	A15.10
3	FrameSync setup time	1.0	—	—	ns	A15.11
4	Output Data valid after clock edge	—	—	14.0	ns	A15.12
5	Input Data setup time	1.0	—	—	ns	A15.13
6	Input Data hold time	1.0	—	—	ns	A15.14

1 Bit Clock cycle time.

NOTE

Output timing is specified at a nominal 50 pF load.

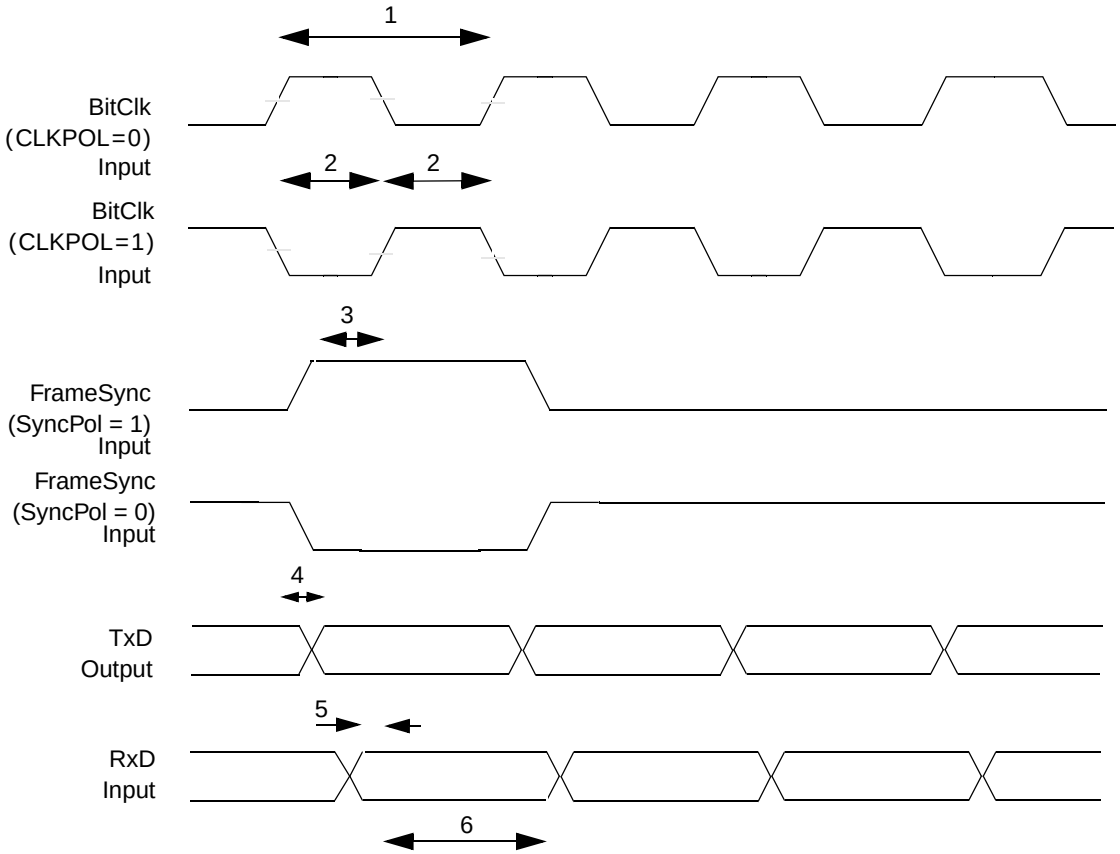


Figure 38. Timing Diagram — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

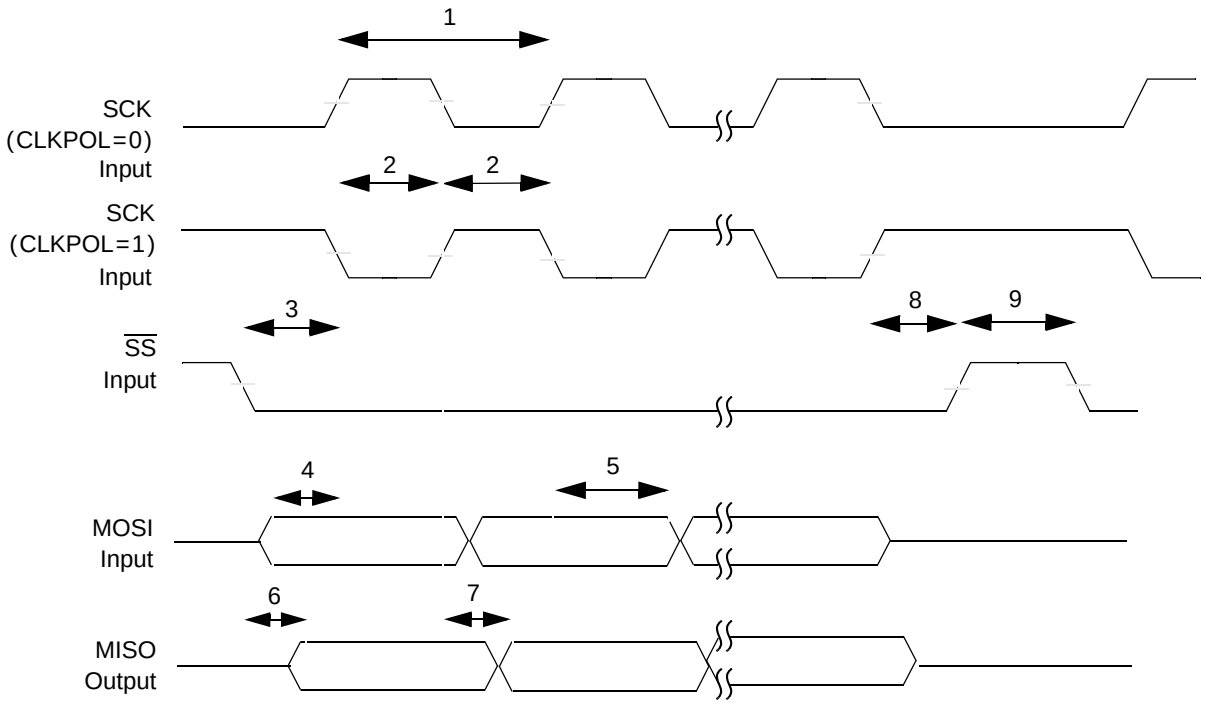


Figure 42. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 48. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.46
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.47
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.48
4	Output data valid	—	8.9	ns	A15.49
5	Input Data setup time	6.0	—	ns	A15.50
6	Input Data hold time	1.0	—	ns	A15.51
7	Slave disable lag time	—	8.9	ns	A15.52
8	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.53
9	Clock falling time	—	7.9	ns	A15.54
10	Clock rising time	—	7.9	ns	A15.55

NOTE

Output timing is specified at a nominal 50 pF load.

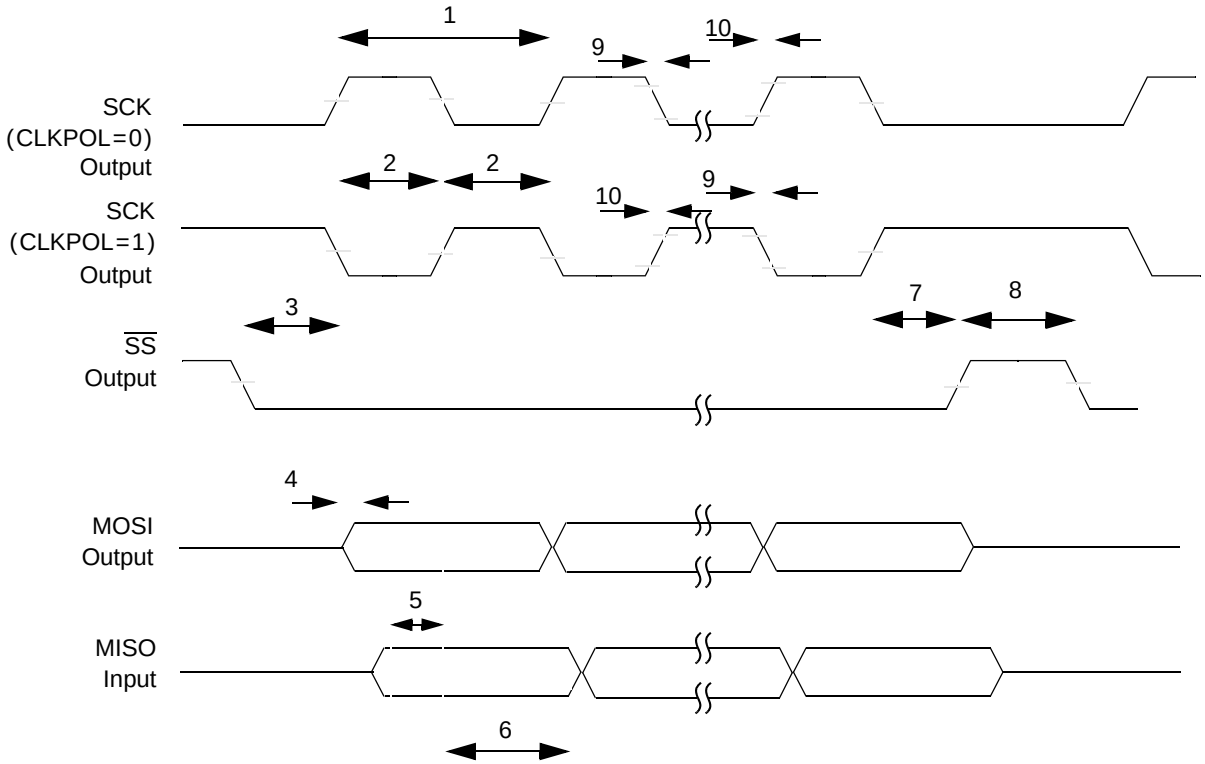


Figure 43. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.56
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.57
3	Slave select clock delay	0.0	—	ns	A15.58
4	Output data valid	—	14.0	ns	A15.59
5	Input Data setup time	2.0	—	ns	A15.60
6	Input Data hold time	1.0	—	ns	A15.61
7	Slave disable lag time	0.0	—	ns	A15.62
8	Minimum Sequential Transfer delay = 2 × IP-Bus clock cycle time	30.0	—	ns	A15.63

NOTE

Output timing is specified at a nominal 50 pF load.

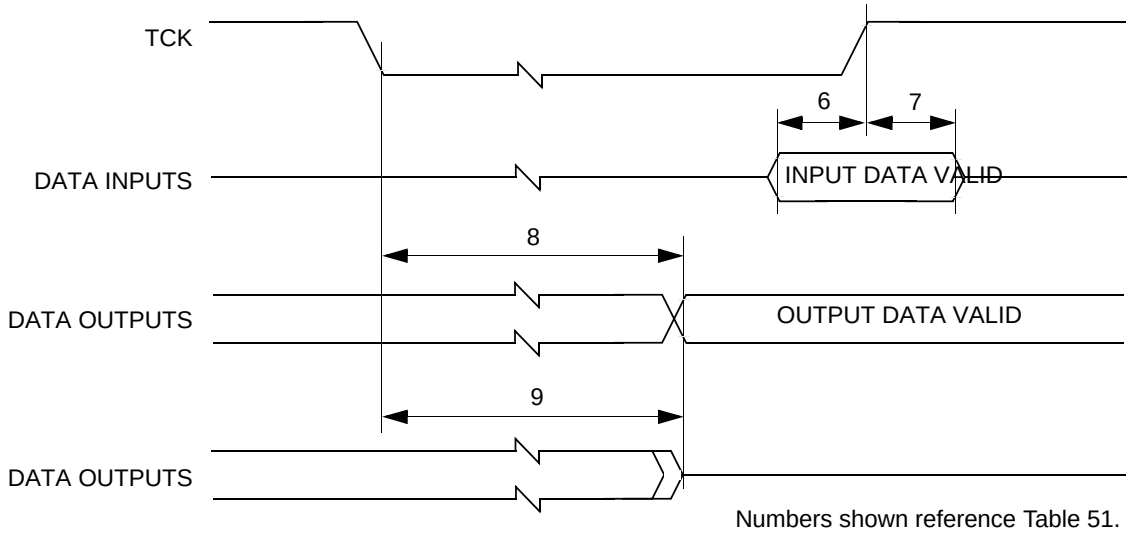


Figure 48. Timing Diagram—JTAG Boundary Scan

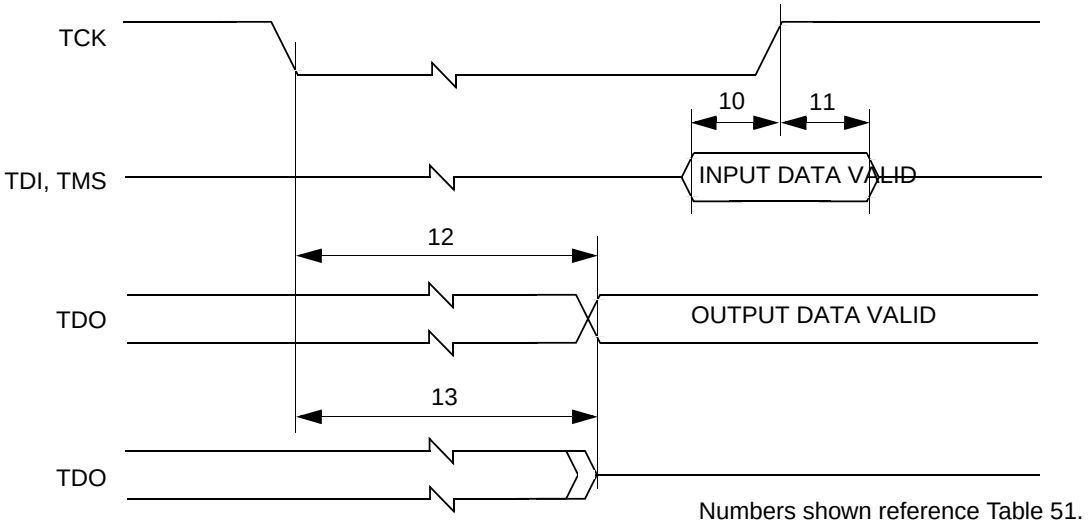


Figure 49. Timing Diagram—Test Access Port

2 Package Description

2.1 Package Parameters

The MPC5200B uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline: 27 mm x 27 mm
- Interconnects: 2
- Pitch: 1.27 mm

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, RTX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200B.

3.4.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

3.4.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5200B functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale (formerly Motorola) standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5200B I/O Pin	BDM Connector	Internal Pull Up/Down	External Pull Up/Down	I/O[1]
16	—	GND	—	—	—
15	TEST_SEL_0	ckstp_out	—	—	I
14	—	KEY	—	—	—
13	HRESET	hreset	—	10k Pull-Up	O
12	—	GND	—	—	—
11	SRESET	sreset	—	10k Pull-Up	O
10	—	N/C	—	—	—
9	JTAG_TMS	tms	100k Pull-Up	10k Pull-Up	O
8	—	N/C	—	—	—
7	JTAG_TCK	tck	100k Pull-Up	10k Pull-Up	O
6	—	VDD[2]	—	—	—
5	—	halted[3]	—	—	I
4	JTAG_TRST	trst	100k Pull-Up	10k Pull-Up	O
3	JTAG_TDI	tdi	100k Pull-Up	10k Pull-Up	O
2	—	qack[4]	—	—	O
1	JTAG_TDO	tdo	—	—	I

1 With respect to the emulator tool's perspective, Input is really an output from the embedded e300 core and output is really an input to the core.

2 From the board under test, power sense for chip power.

3 HALTED is not available from e300 core.

4 Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5200B internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector, which accesses the JTAG interface and which needs to reset the JTAG module, simply wiring $\overline{\text{JTAG\_TRST}}$ and $\overline{\text{PORRESET}}$ is not recommended.

To reset the MPC5200B via the COP connector, the HRESET pin of the COP should be connected to the HRESET pin of the MPC5200B. The circuitry shown in Figure 54 allows the COP to assert HRESET or JTAG_TRST separately, while any other board sources can drive PORRESET.

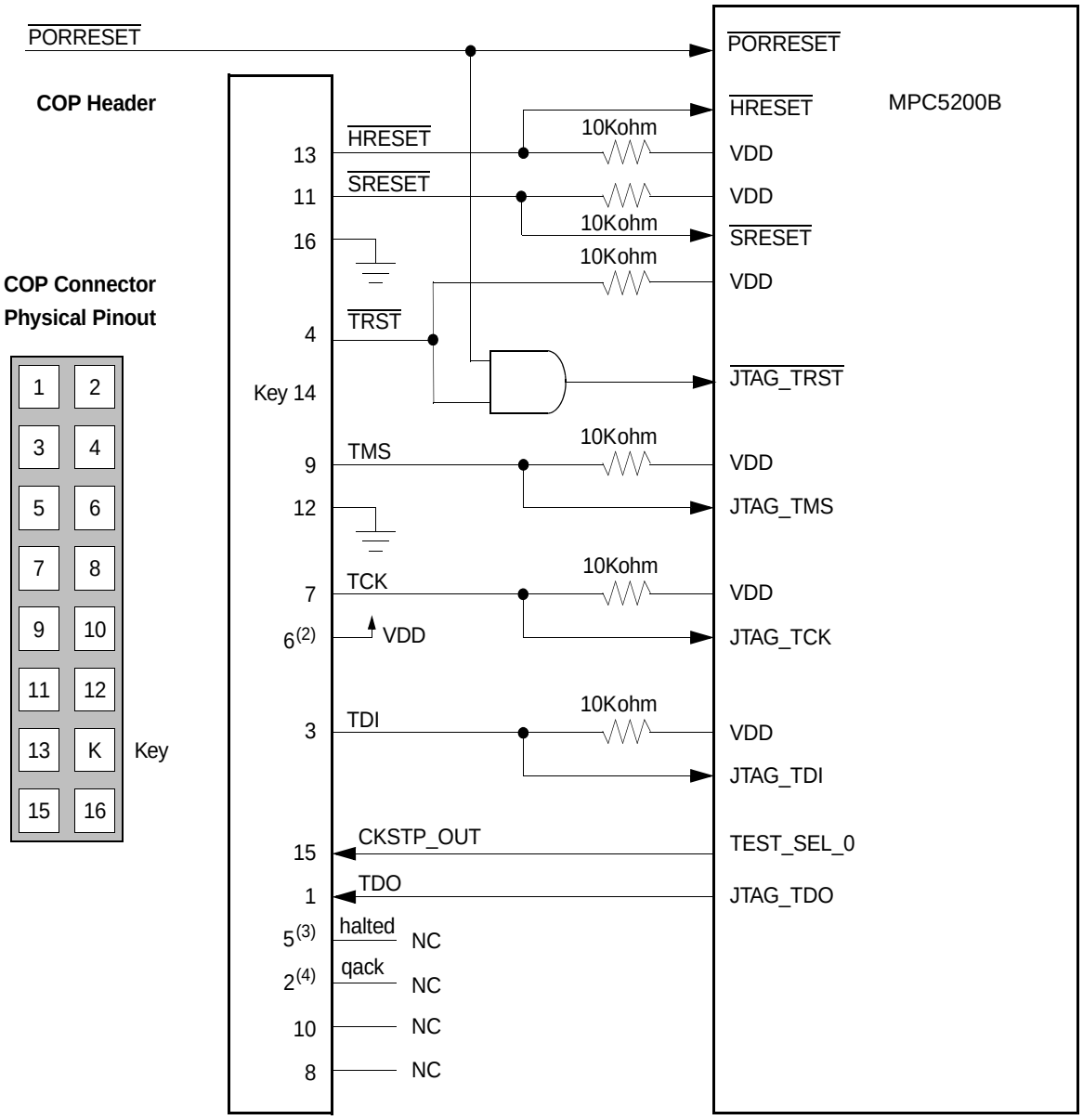


Figure 54. COP Connector Diagram

3.4.2.2 Boards Without COP Connector

If the JTAG interface is not used, JTAG_TRST should be tied to PORRESET, so that it is asserted when the system reset signal (PORRESET) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 55 shows the connection of the JTAG interface without COP connector.