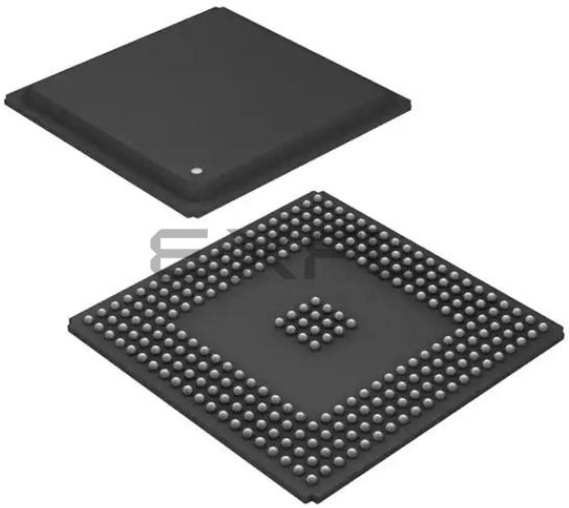

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cbv400b

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Table 2. Recommended Operating Conditions (continued)

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Input voltage — standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage — memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8
Input voltage — memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	–40	+85	^oC	D2.10
Die junction operating temperature range	Tj	–40	+115	^oC	D2.12

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 Maximum e300 core operating frequency is 400 MHz.

1.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200B at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12
Input leakage current	Vin = 0 or VDD_IO/$VDD\_IO\_MEM_{SDR}$ (depending on input type[1])	I_{IN}	—	±2	μA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	μA	D3.14

1.1.6 Thermal Characteristics

Table 7. Thermal Resistance Data

Rating	Board Layers	Sym	Value	Unit	Notes	SpecID
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	30	°C/W	(1),(2)	D6.1
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	(1),(3)	D6.2
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W	(1),(3)	D6.3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	19	°C/W	(1),(3)	D6.4
Junction to Board	—	$R_{\theta JB}$	14	°C/W	(4)	D6.5
Junction to Case	—	$R_{\theta JC}$	8	°C/W	(5)	D6.6
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	(6)	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

1.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

1.2 Oscillator and PLL Electrical Characteristics

The MPC5200B System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200B clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

1.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	10	ms	O1.2

1.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

1.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	(1)	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	t_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	(2)	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	(3)	—	—	100	µs	O3.5

1 The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLKare reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

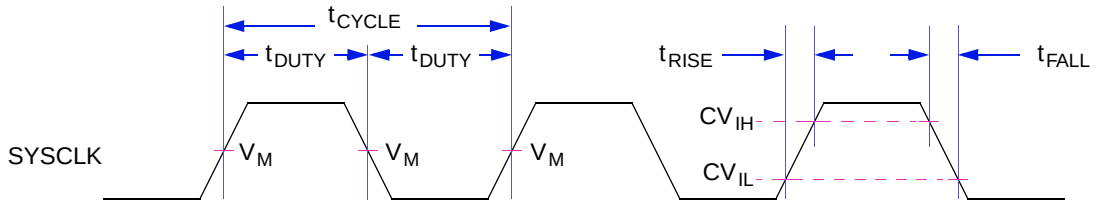


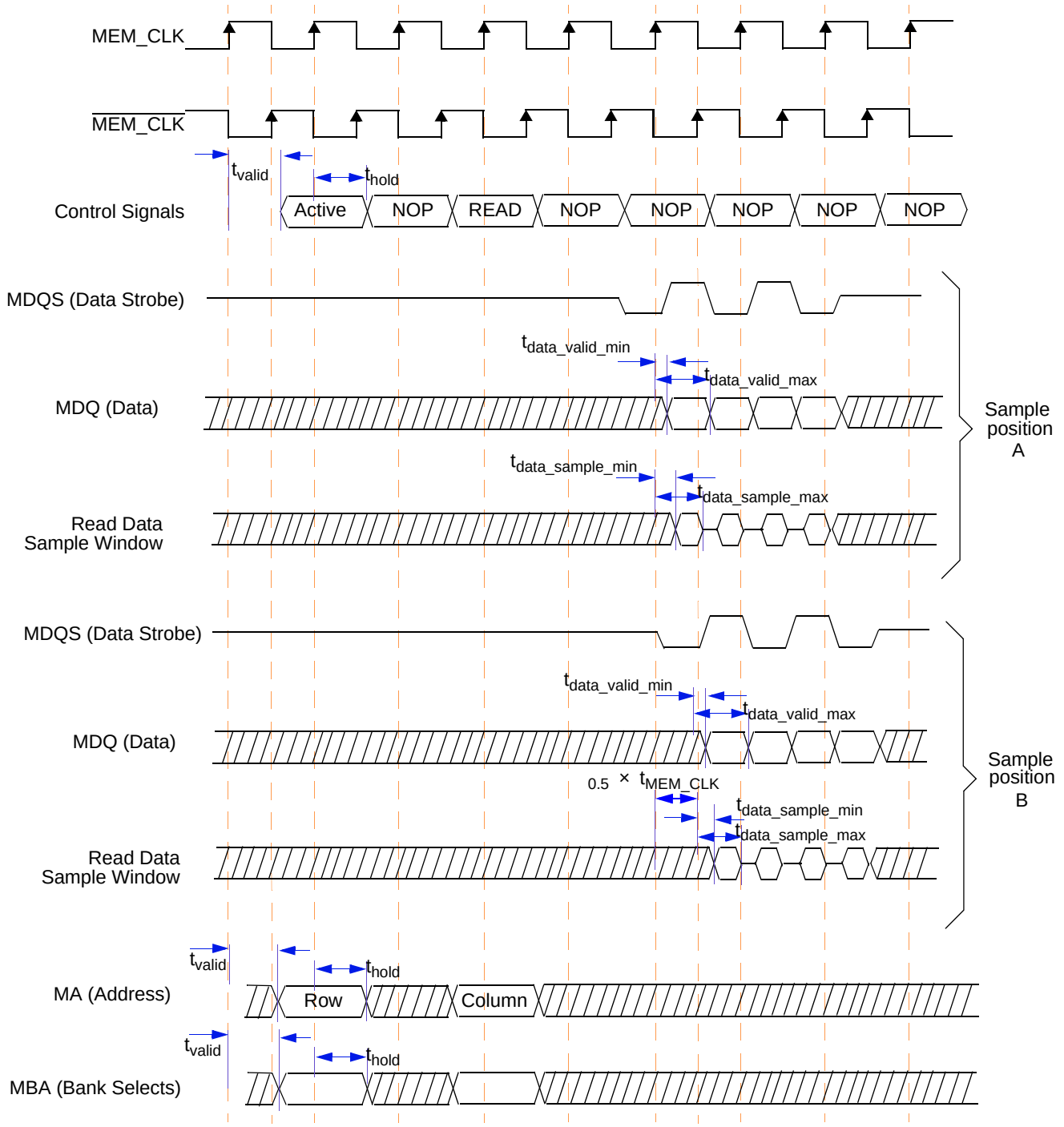
Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.(1)	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).(2)	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data

Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the valid MDQS signal

NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

Table 24. Non-MUXed Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_{10}	DATA input setup before CS negation	8.5	—	ns	—	A7.12
t_{11}	DATA input hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(6)	A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	—	ns	(3)	A7.14
t_{13}	ACK negation after CS negation	—	t_{PCIck}	ns	(3)	A7.15
t_{14}	TS assertion before CS assertion	—	6.9	ns	(4)	A7.16
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	(4)	A7.17
t_{16}	TSIZ valid before CS assertion	t_{IPBIck}	—	ns	(5)	A7.18
t_{17}	TSIZ hold after CS negation	t_{IPBIck}	—	ns	(5)	A7.19
t_{18}	ACK change before PCI clock	—	2.0	ns	(1)	A7.20
t_{19}	ACK change after PCI clock	—	4.4	ns	(1)	A7.21

NOTES:

1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause the address to change before CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.
6. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

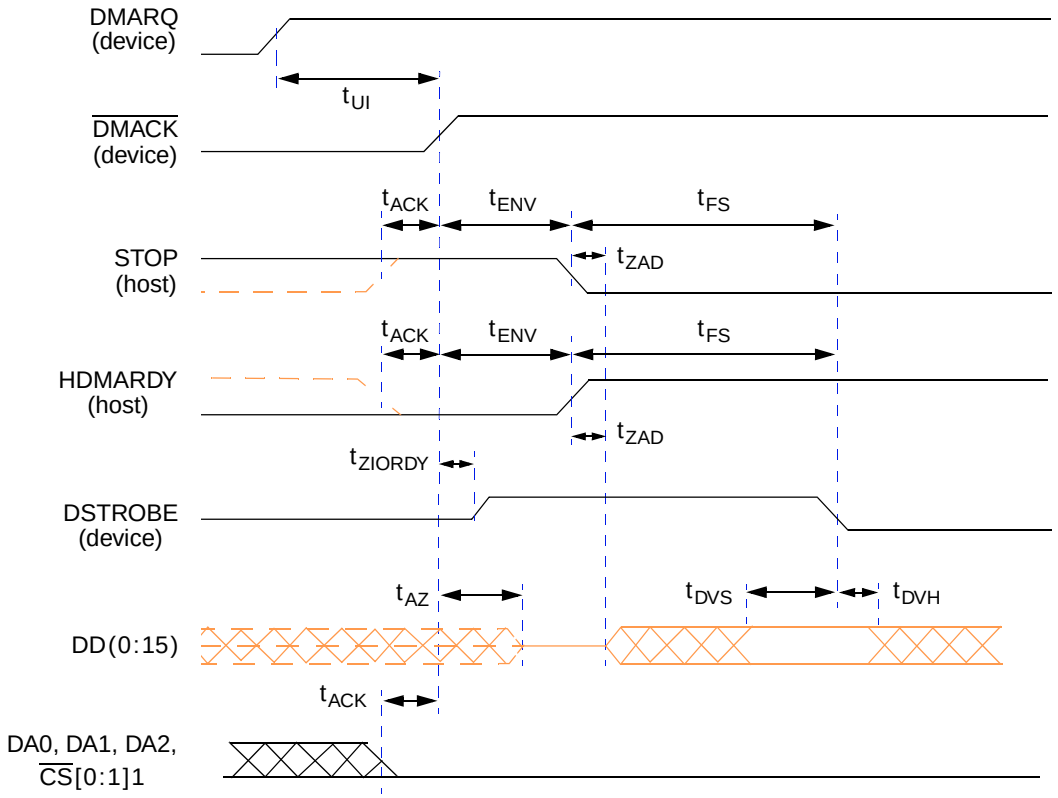


Figure 16. Timing Diagram—Initiating an Ultra DMA Data In Burst

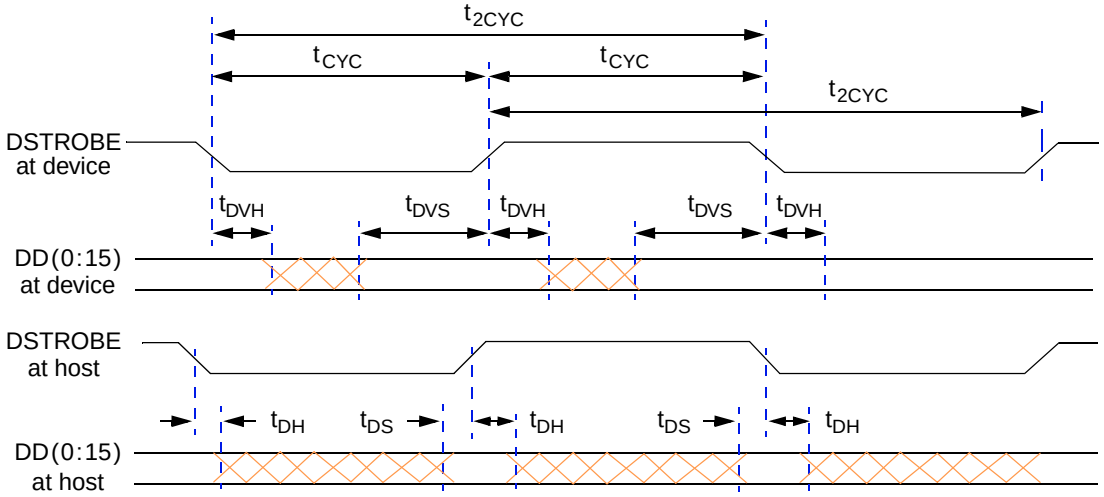


Figure 17. Timing Diagram—Sustained Ultra DMA Data In Burst

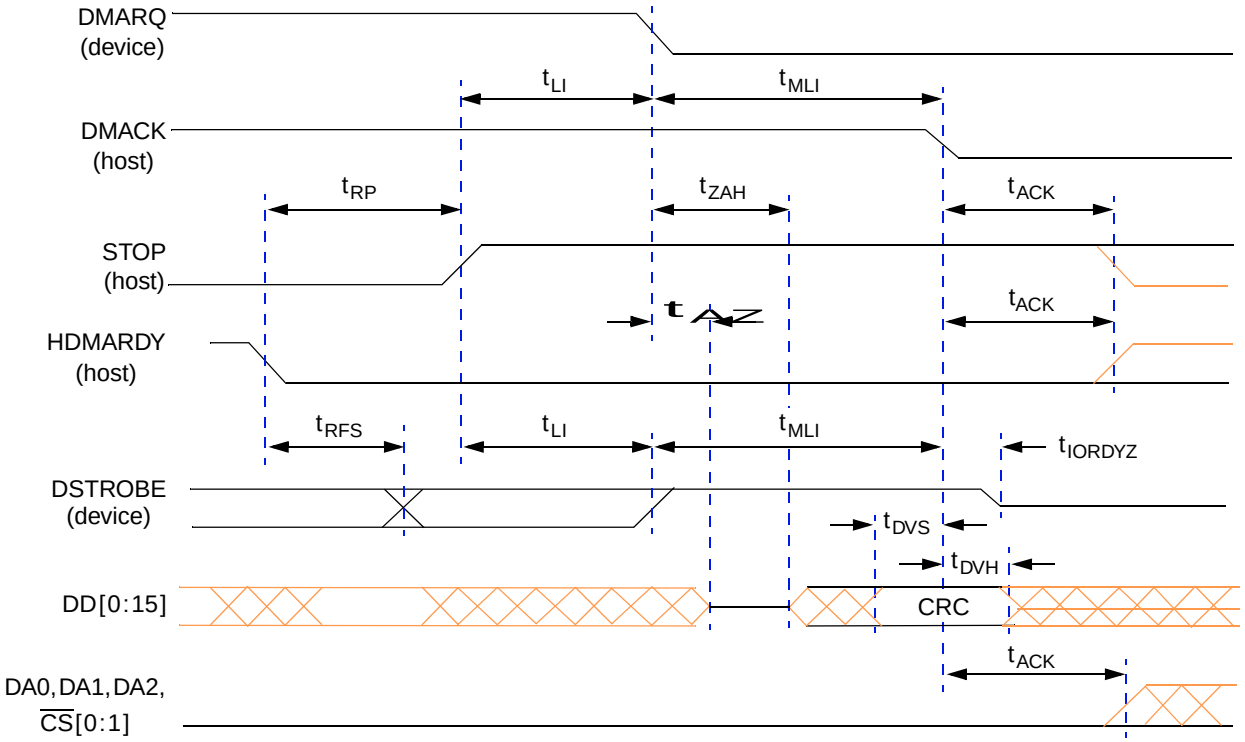


Figure 20. Timing Diagram—Host Terminating Ultra DMA Data In Burst

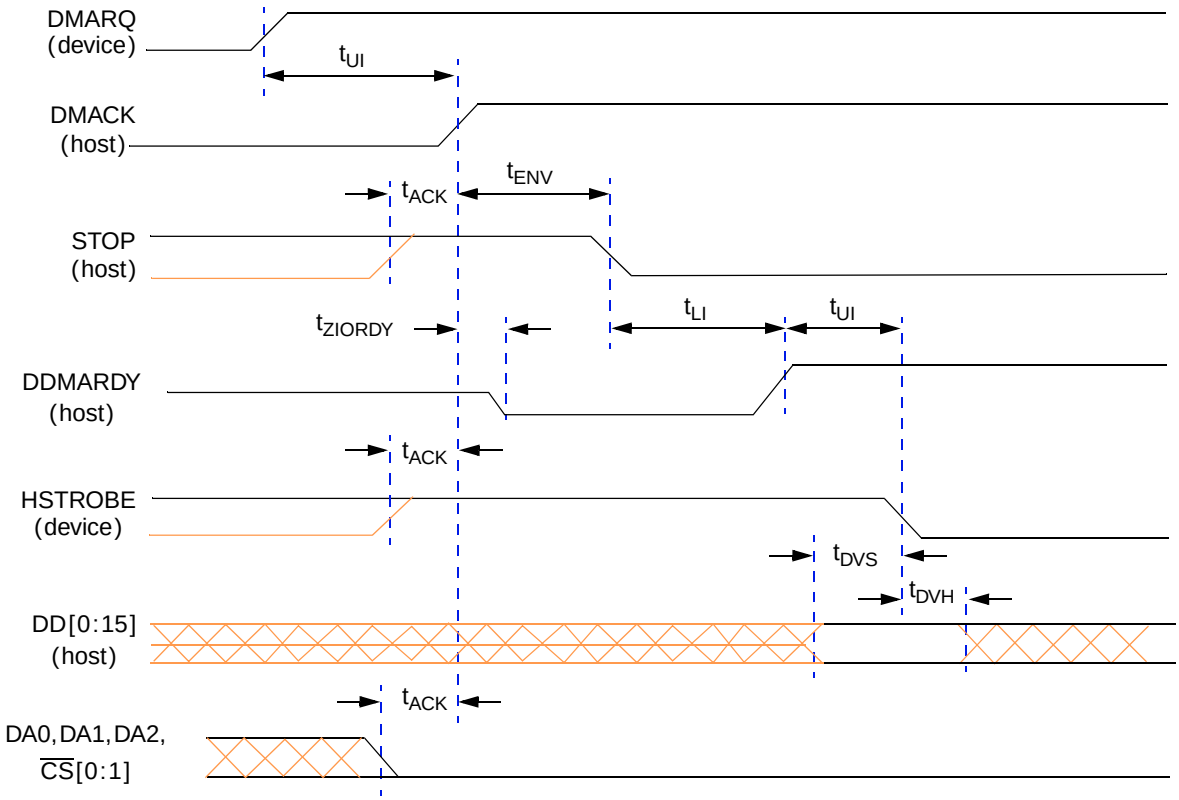


Figure 21. Timing Diagram—Initiating an Ultra DMA Data Out Burst

Table 32. MII Tx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns	A9.5
t_6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A9.6
t_7	TX_CLK pulse width high	35%	65%	TX_CLK Period(1)	A9.7
t_8	TX_CLK pulse width low	35%	65%	TX_CLK Period(1)	A9.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

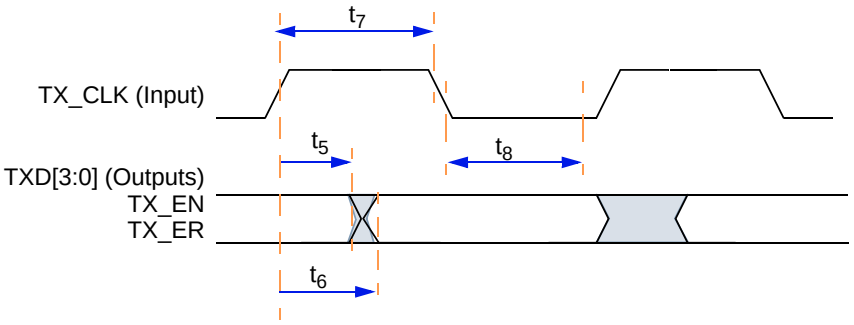


Figure 28. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A9.9

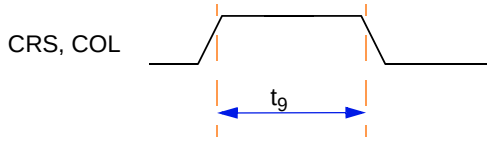


Figure 29. Ethernet Timing Diagram—MII Async

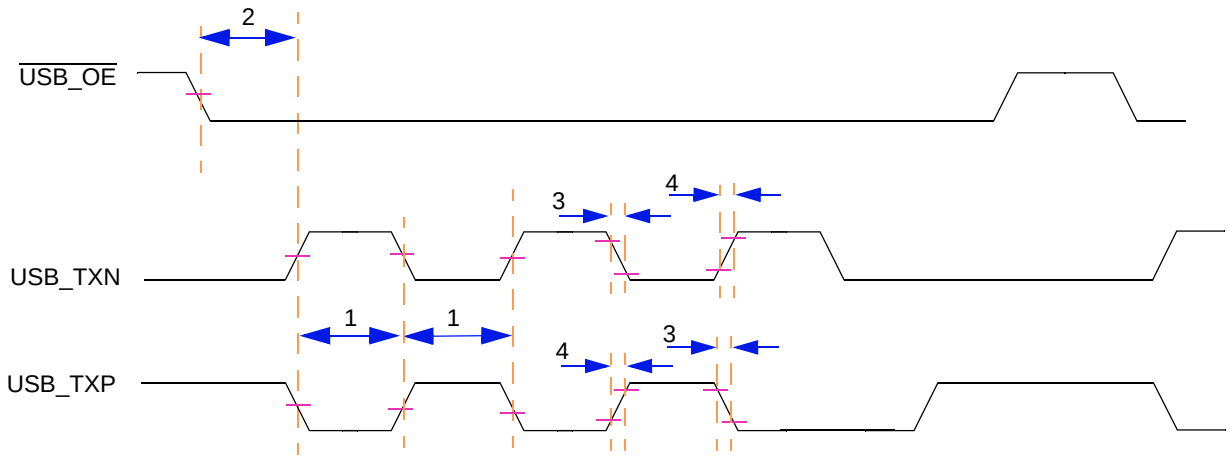


Figure 31. Timing Diagram—USB Output Line

1.3.12 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.1
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.2
3	Slave select to clock delay	15.0	—	ns	A11.3
4	Output Data valid after Slave Select ($\overline{SS}$)	—	20.0	ns	A11.4
5	Output Data valid after SCK	—	20.0	ns	A11.5
6	Input Data setup time	20.0	—	ns	A11.6
7	Input Data hold time	20.0	—	ns	A11.7
8	Slave disable lag time	15.0	—	ns	A11.8
9	Sequential transfer delay	1	—	IP-Bus Cycle[1]	A11.9
10	Clock falling time	—	7.9	ns	A11.10
11	Clock rising time	—	7.9	ns	A11.11

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

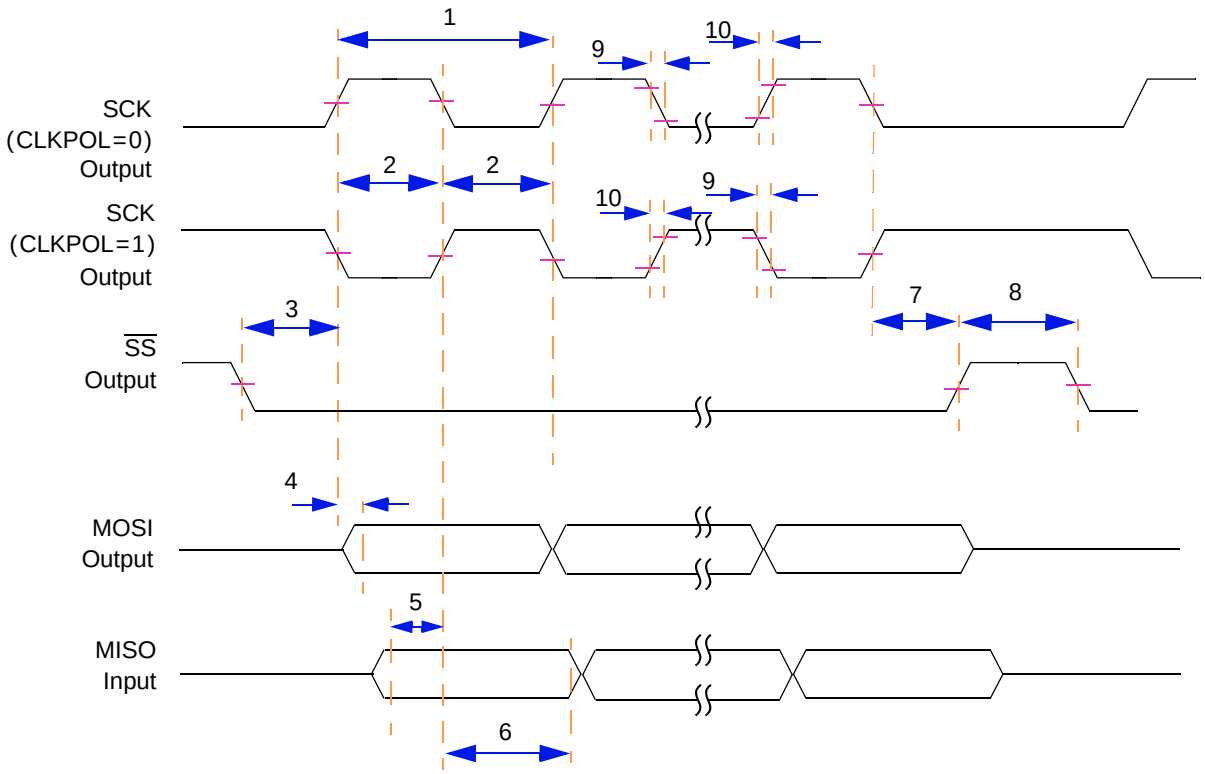


Figure 43. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.56
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.57
3	Slave select clock delay	0.0	—	ns	A15.58
4	Output data valid	—	14.0	ns	A15.59
5	Input Data setup time	2.0	—	ns	A15.60
6	Input Data hold time	1.0	—	ns	A15.61
7	Slave disable lag time	0.0	—	ns	A15.62
8	Minimum Sequential Transfer delay = 2 × IP-Bus clock cycle time	30.0	—	ns	A15.63

NOTE

Output timing is specified at a nominal 50 pF load.

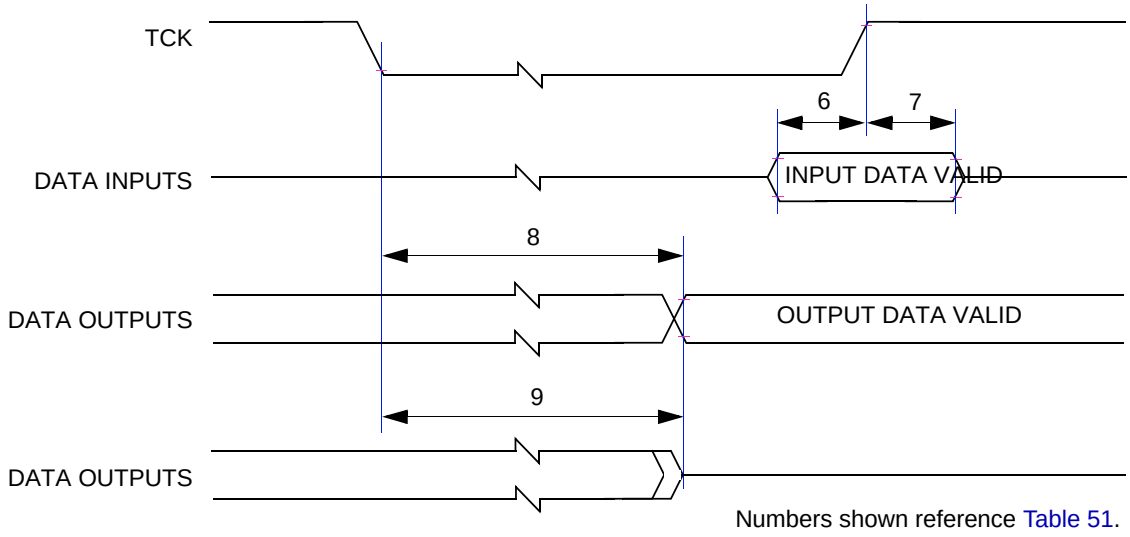


Figure 48. Timing Diagram—JTAG Boundary Scan

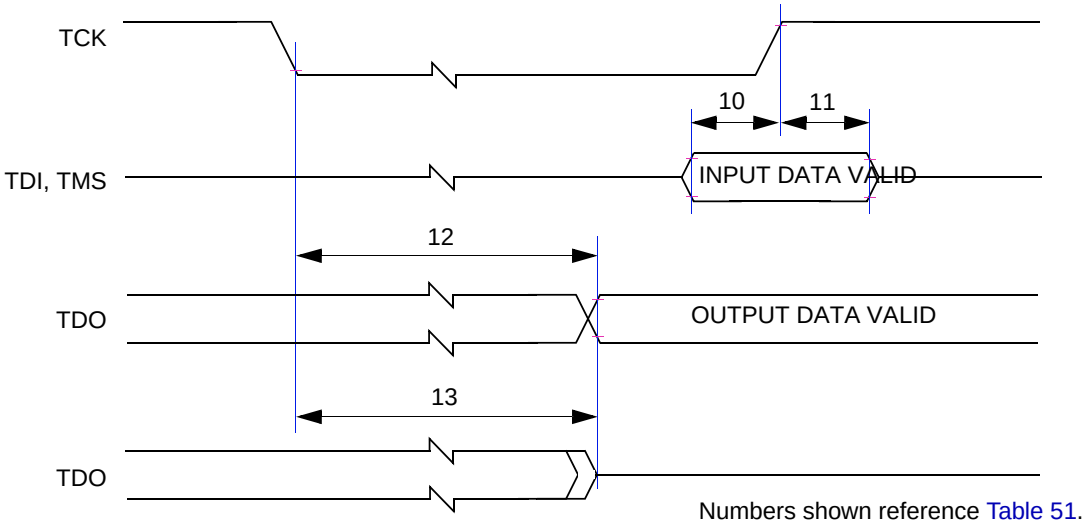


Figure 49. Timing Diagram—Test Access Port

2 Package Description

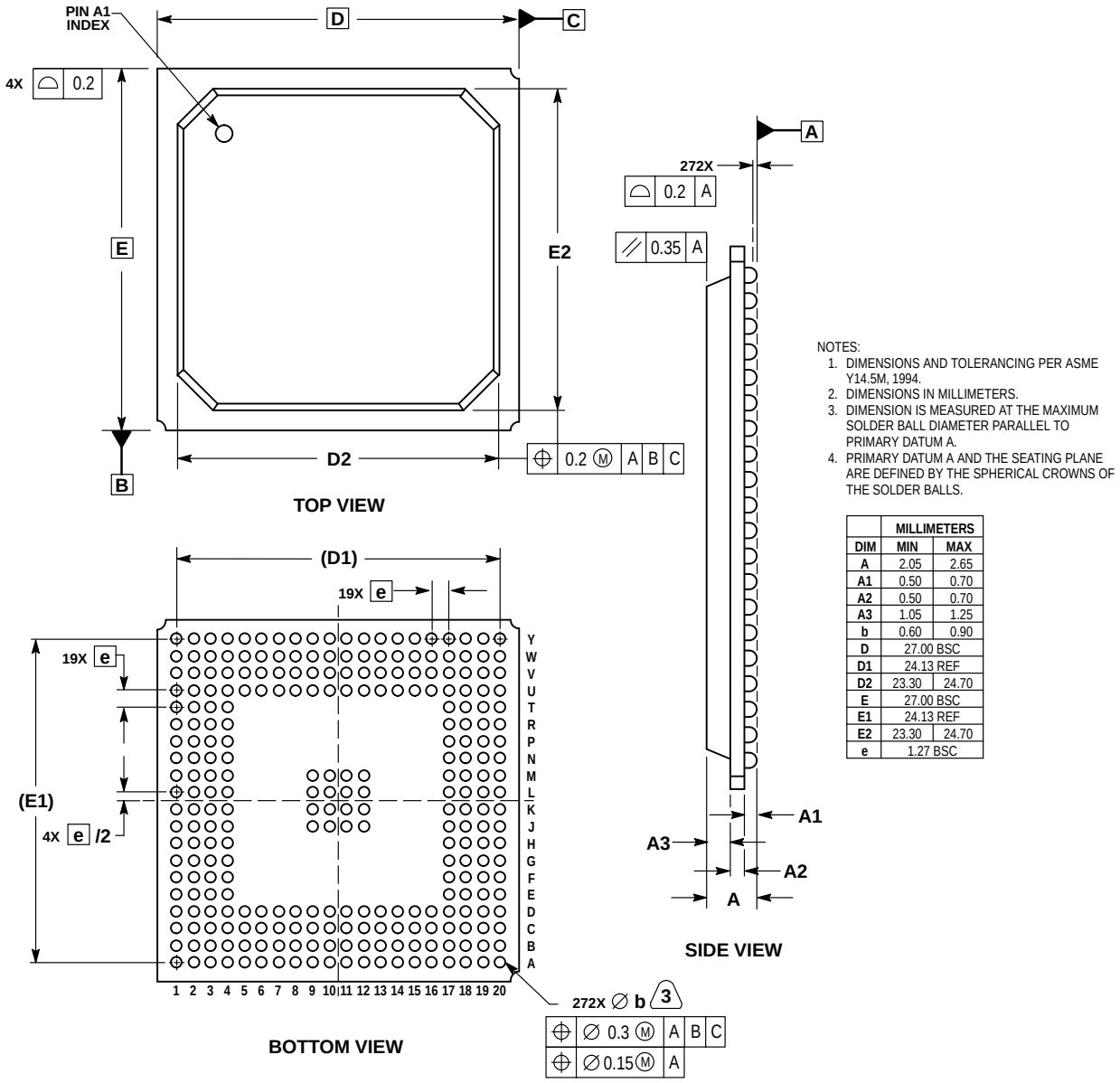
2.1 Package Parameters

The MPC5200B uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline: 27 mm x 27 mm
- Interconnects: 2
- Pitch: 1.27 mm

2.2 Mechanical Dimensions

Figure 50 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC5200B, 272 TE-PBGA package.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135A–01
ISSUE B

Figure 50. Mechanical Dimensions and Pinout Assignments for the MPC5200B, 272 TE-PBGA

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

The relationship between VDD_IO_MEM and VDD_IO is non-critical during power-up and power-down sequences. VDD_IO_MEM (2.5 V or 3.3 V) and VDD_IO are specified relative to VDD_CORE.

3.1.1 Power Up Sequence

If VDD_IO/VDD_IO_MEM are powered up with the VDD_CORE at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the VDD_IO/VDD_IO_MEM to be in a high-impedance state. There is no limit to how long after VDD_IO/VDD_IO_MEM powers up before VDD_CORE must power up. VDD_CORE should not lead the VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

Use one microsecond or slower rise time for all supplies.

VDD_CORE/PLL_AVDD and VDD_IO/VDD_IO_MEM should track up to 0.9 V and then separate for the completion of ramps with VDD_IO/VDD_IO_MEM going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.1.2 Power Down Sequence

If VDD_CORE/PLL_AVDD are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after VDD_CORE and PLL_AVDD power down before VDD_IO or VDD_IO_MEM must power down. VDD_CORE should not lag VDD_IO, VDD_IO_MEM, or PLL_AVDD going low by more than 0.5 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop VDD_CORE/PLL_AVDD to 0 V.
2. Drop VDD_IO/VDD_IO_MEM supplies.

3.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing is a recommendation for the required filter circuit.

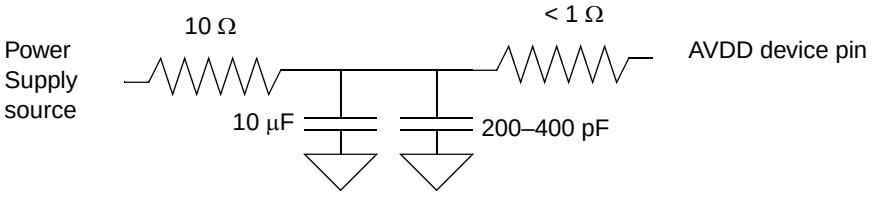


Figure 52. Power Supply Filtering

3.3 Pull-up/Pull-down Resistor Requirements

The MPC5200B requires external pull-up or pull-down resistors on certain pins.

3.3.1 Pull-down Resistor Requirements for TEST pins

The MPC5200B requires pull-down resistors on the test pins TEST_MODE_0, TEST_MODE_1, TEST_SEL_1.

3.3.2 Pull-up Requirements for the PCI Control Lines

If the PCI interface is NOT used (and internally disabled) the PCI control pins must be terminated as indicated by the PCI Local Bus specification. This is also required for MOST/Graphics and Large Flash Mode.

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

3.3.3 Pull-up/Pull-down Requirements for MEM_MDQS Pins (SDRAM)

The MEM_MDQS[3:0] signals are not used with SDR memories and require pull-up or pull-down resistors in SDRAM mode.

3.3.4 Pull-up/Pull-down Requirements for MEM_MDQS Pins (DDR 16-bit Mode)

The MEM_MDQS[1:0] signals are not used in DDR 16-bit mode and require pull-down resistors.

3.4 JTAG

The MPC5200B provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200B's embedded Freescale (formerly Motorola) MPC603e e300 processor. This interface provides a means for executing test routines and for performing software development and debug functions.

3.4.1 $\overline{\text{JTAG\_TRST}}$

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{JTAG\_TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

3.4.1.1 $\overline{\text{JTAG\_TRST}}$ and $\overline{\text{PORRESET}}$

The JTAG interface can control the direction of the MPC5200B I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5200B comes out of power-on reset; do this by asserting JTAG_TRST before $\overline{\text{PORRESET}}$ is released.

For more details refer to the Reset and JTAG Timing Specification.

Figure 53. $\overline{\text{PORRESET}}$ vs. $\overline{\text{JTAG\_TRST}}$

3.4.1.2 Connecting JTAG_TRST

The wiring of the $\overline{\text{JTAG\_TRST}}$ depends on the existence of a board-related debug interface. (see below)

5 Document Revision History

Table 55 provides a revision history for this hardware specification.

Table 55. Document Revision History

Rev. No.	Differences
1	Clock Frequencies table: 466 MHz was changed to 400 MHz for the e300 Processor Core
2	Added description for PCI CLK Slew Rate for PCI CLK Specifications table.
	Added description for minimum rates in the DDR SDRAM Memory Write Timing table.
3	Added one item to table “DDR SDRAM Memory Read Timing.”
4	Updated table “Ordering Information.”