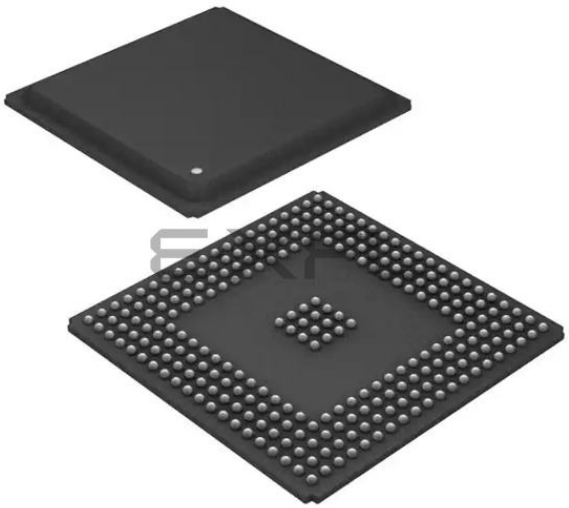

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cbv400br2

Table 2. Recommended Operating Conditions (continued)

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Input voltage — standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage — memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8
Input voltage — memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	–40	+85	^oC	D2.10
Die junction operating temperature range	Tj	–40	+115	^oC	D2.12

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 Maximum e300 core operating frequency is 400 MHz.

1.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200B at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12
Input leakage current	Vin = 0 or VDD_IO/$VDD\_IO\_MEM_{SDR}$ (depending on input type[1])	I_{IN}	—	±2	μA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	μA	D3.14

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor — memory I/O buffers	PULLUP_MEM $VDD\_IO\_MEM_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin(3)		I_{CS}	–1.0	1.0	mA	D3.23
Capacitance	Vin = 0 V, f = 1 MHz	C_{in}	—	15	pF	D3.24

1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.

3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200B Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3 V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3 V	8	8	mA	D3.26
DRV8_OD	VDD_IO = 3.3 V	—	8	mA	D3.27
DRV16_MEM	VDD_IO_MEM = 3.3 V	16	16	mA	D3.28
DRV16_MEM	VDD_IO_MEM = 2.5 V	16	16	mA	D3.29
PCI	VDD_IO = 3.3 V	16	16	mA	D3.30

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

1.2 Oscillator and PLL Electrical Characteristics

The MPC5200B System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200B clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

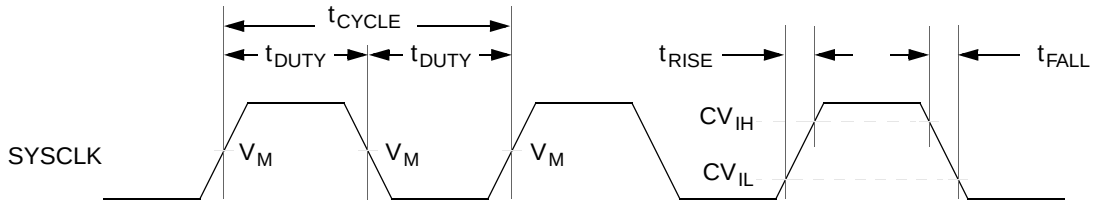


Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.(1)	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).(2)	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 —The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.

1.3.4 Resets

The MPC5200B has three reset pins:

- $\overline{\text{PORRESET}}$—Power on Reset
- $\overline{\text{HRESET}}$—Hard Reset
- $\overline{\text{SRESET}}$—Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200B inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

Table 14. Reset Pulse Width

Name	Description	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
$\overline{\text{PORRESET}}$	Power On Reset	$t_{VDD\_stable} + t_{up\_osc} + t_{lock}$	—	SYS_XTAL_IN	A3.1
$\overline{\text{HRESET}}$	Hardware Reset	4 clock cycles	—	SYS_XTAL_IN	A3.2
$\overline{\text{SRESET}}$	Software Reset	4 clock cycles	—	SYS_XTAL_IN	A3.3

For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.

The t_{VDD_stable} describes the time which is needed to get all power supplies stable.

For t_{lock}, refer to the Oscillator/PLL section of this specification for further details.

For t_{up_osc}, refer to the Oscillator/PLL section of this specification for further details.

Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.

The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

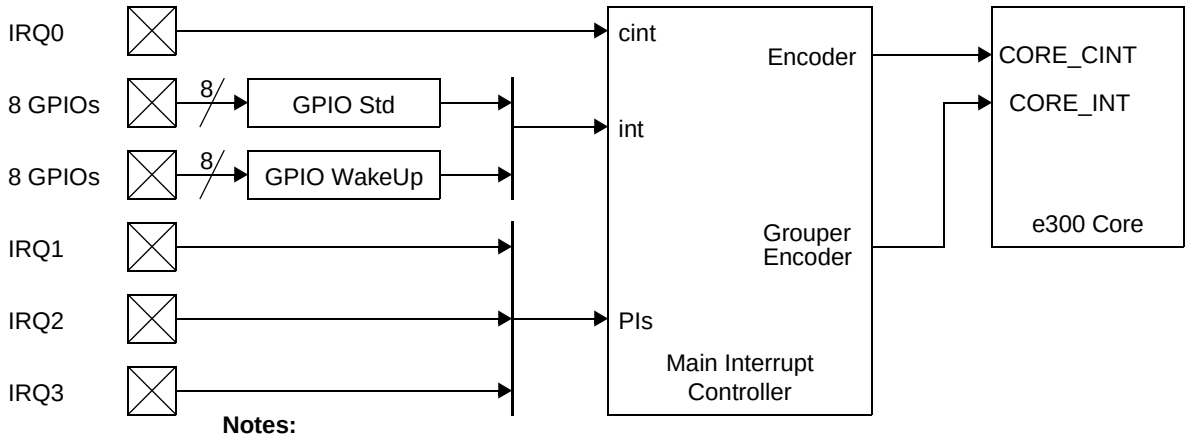
As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 15. Reset Rise/Fall Timing

Description	Min	Max	Unit	SpecID
$\overline{\text{PORRESET}}$ fall time	—	1	ms	A3.4
$\overline{\text{PORRESET}}$ rise time	—	1	ms	A3.5
$\overline{\text{HRESET}}$ fall time	—	1	ms	A3.6
$\overline{\text{HRESET}}$ rise time	—	1	ms	A3.7
$\overline{\text{SRESET}}$ fall time	—	1	ms	A3.8
$\overline{\text{SRESET}}$ rise time	—	1	ms	A3.9

NOTE

Make sure that the $\overline{\text{PORRESET}}$ does not carry any glitches. The MPC5200B has no filter to prevent them from getting into the chip. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time. The assertion of $\overline{\text{HRESET}}$ becomes active at Power on Reset without any SYS_XTAL clock.



Notes:
1. PIs = Programmable Inputs
2. Grouper and Encoder functions imply programmability in software

Figure 4. External Interrupt Scheme

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Table 16).

Table 16. External Interrupt Latencies

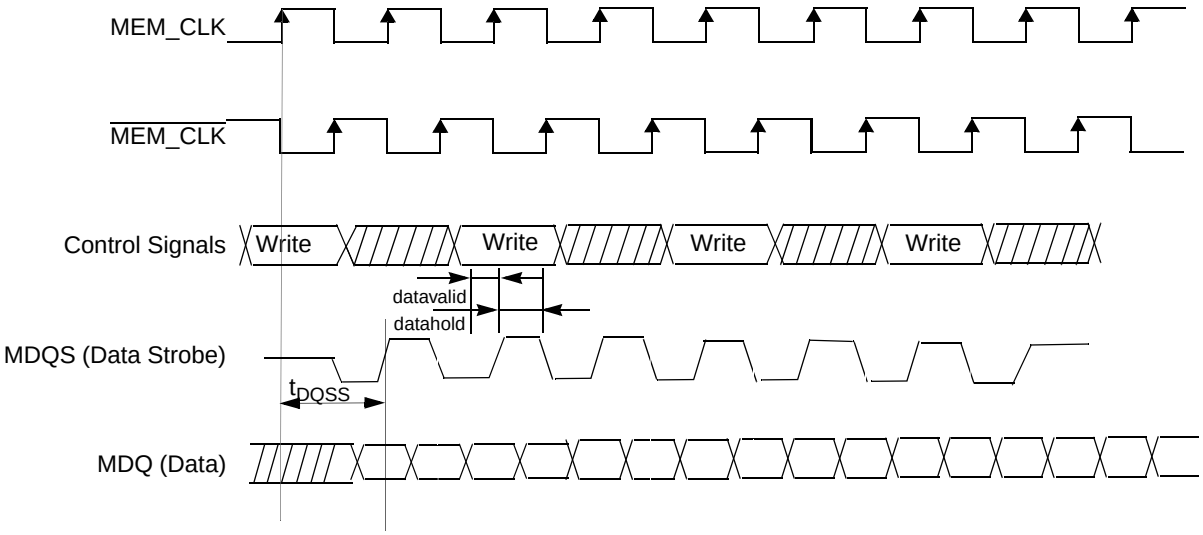
Interrupt Type	Pin Name	Clock Cycles	Reference Clock	Core Interrupt	SpecID
Interrupt Requests	IRQ0	10	IP_CLK	critical (cint)	A4.1
	IRQ0	10	IP_CLK	normal (int)	A4.2
	IRQ1	10	IP_CLK	normal (int)	A4.3
	IRQ2	10	IP_CLK	normal (int)	A4.4
	IRQ3	10	IP_CLK	normal (int)	A4.5
Standard GPIO Interrupts	GPIO_PSC3_4	12	IP_CLK	normal (int)	A4.6
	GPIO_PSC3_5	12	IP_CLK	normal (int)	A4.7
	GPIO_PSC3_8	12	IP_CLK	normal (int)	A4.8
	GPIO_USB_9	12	IP_CLK	normal (int)	A4.9
	GPIO_ETHI_4	12	IP_CLK	normal (int)	A4.10
	GPIO_ETHI_5	12	IP_CLK	normal (int)	A4.11
	GPIO_ETHI_6	12	IP_CLK	normal (int)	A4.12
	GPIO_ETHI_7	12	IP_CLK	normal (int)	A4.13
GPIO WakeUp Interrupts	GPIO_PSC1_4	12	IP_CLK	normal (int)	A4.15
	GPIO_PSC2_4	12	IP_CLK	normal (int)	A4.16
	GPIO_PSC3_9	12	IP_CLK	normal (int)	A4.17
	GPIO_ETHI_8	12	IP_CLK	normal (int)	A4.18
	GPIO_IRDA_0	12	IP_CLK	normal (int)	A4.19
	DGP_IN0	12	IP_CLK	normal (int)	A4.20
	DGP_IN1	12	IP_CLK	normal (int)	A4.21

NOTES:
1) The frequency of IP_CLK depends on register settings in Clock Distribution Module. See the *MPC5200B User's Manual*.

1.3.6.4 Memory Interface Timing-DDR SDRAM Write Command

Table 21. DDR SDRAM Memory Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.20
t_{DQSS}	Delay from write command to first rising edge of MDQS	—	t_{mem_clk} + 0.4	ns	A5.21
$data_{valid}$	MDQ valid before rising edge of MDQS	1.0	—	ns	A5.22
$data_{hold}$	MDQ valid after rising edge of MDQS	1.0	—	ns	A5.23



NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$, and CLK_EN

Figure 8. DDR SDRAM Memory Write Timing

1.3.7 PCI

The PCI interface on the MPC5200B is designed to PCI Version 2.2 and supports 33 MHz and 66 MHz PCI operations. See the PCI Local Bus Specification; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

The MPC5200B is always the source of the PCI CLK. The clock waveform must be delivered to each 33 MHz or 66 MHz PCI component in the system. Figure 9 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.

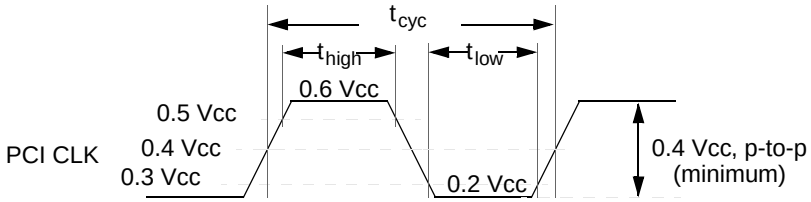


Figure 9. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{cyc}	PCI CLK Cycle Time	15	30	30	—	ns	(1),(3)	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	—	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	—	A6.3
—	PCI CLK Slew Rate	1.5	4	1	4	V/ns	(2)	A6.4
—	PCI Clock Jitter (peak to peak)	—	200	—	200	ps	—	—

NOTES:
1. In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{val}	CLK to Signal Valid Delay — bused signals	2	6	2	11	ns	(1),(2),(3)	A6.5
t_{val}(ptp)	CLK to Signal Valid Delay — point to point	2	6	2	12	ns	(1),(2),(3)	A6.6
t_{on}	Float to Active Delay	2	—	2	—	ns	(1)	A6.7
t_{off}	Active to Float Delay		14		28	ns	(1)	A6.8
t_{su}	Input Setup Time to CLK — bused signals	3	—	7	—	ns	(3),(4)	A6.9
t_{su}(ptp)	Input Setup Time to CLK — point to point	5	—	10,12	—	ns	(3),(4)	A6.10
t_h	Input Hold Time from CLK	0	—	0	—	ns	(4)	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

Table 24. Non-MUXed Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_{10}	DATA input setup before CS negation	8.5	—	ns	—	A7.12
t_{11}	DATA input hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(6)	A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	—	ns	(3)	A7.14
t_{13}	ACK negation after CS negation	—	t_{PCIck}	ns	(3)	A7.15
t_{14}	TS assertion before CS assertion	—	6.9	ns	(4)	A7.16
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	(4)	A7.17
t_{16}	TSIZ valid before CS assertion	t_{IPBIck}	—	ns	(5)	A7.18
t_{17}	TSIZ hold after CS negation	t_{IPBIck}	—	ns	(5)	A7.19
t_{18}	ACK change before PCI clock	—	2.0	ns	(1)	A7.20
t_{19}	ACK change after PCI clock	—	4.4	ns	(1)	A7.21

NOTES:

1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause the address to change before CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.
6. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

Table 25. Burst Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_9	DATA hold after rising edge of PCI clock	0	—	ns	—	A7.32
t_{10}	DATA hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(4)	A7.33
t_{11}	ACK assertion after CS assertion	—	(WS + 1) × t_{PCIck}	ns	—	A7.34
t_{12}	ACK negation before CS negation	—	7.0	ns	(3)	A7.35
t_{13}	ACK pulse width	4^{LB} × 2 × (32/DS) × t_{PCIck}	4^{LB} × 2 × (32/DS) × t_{PCIck}	ns	(2),(3)	A7.36
t_{14}	CS assertion after TS assertion	—	2.5	ns	—	A7.37
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	—	A7.38

NOTES:

1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => 4^1 × 2 × (32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1 + 10 + 32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.
4. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

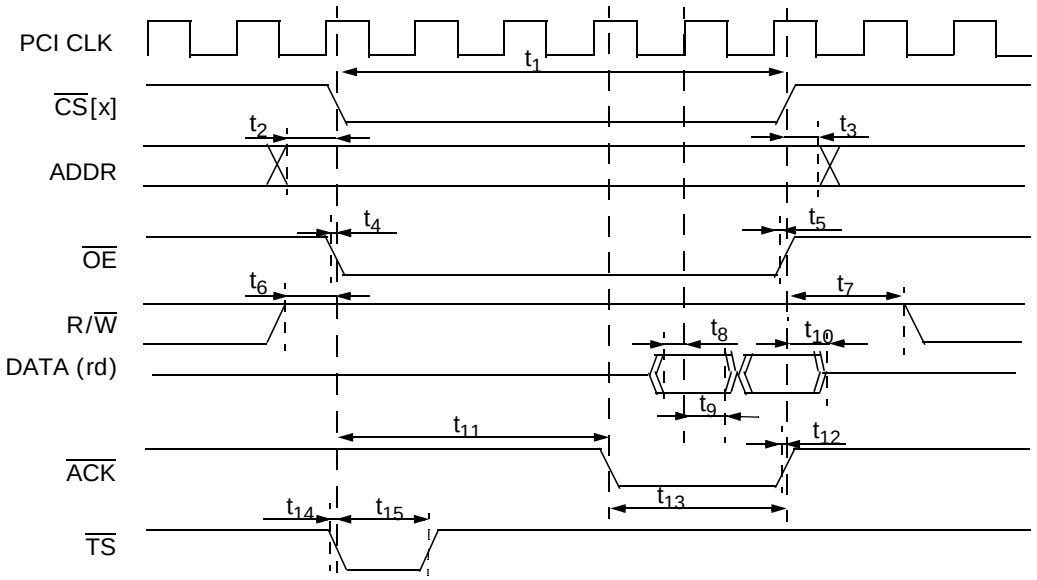


Figure 12. Timing Diagram—Burst Mode

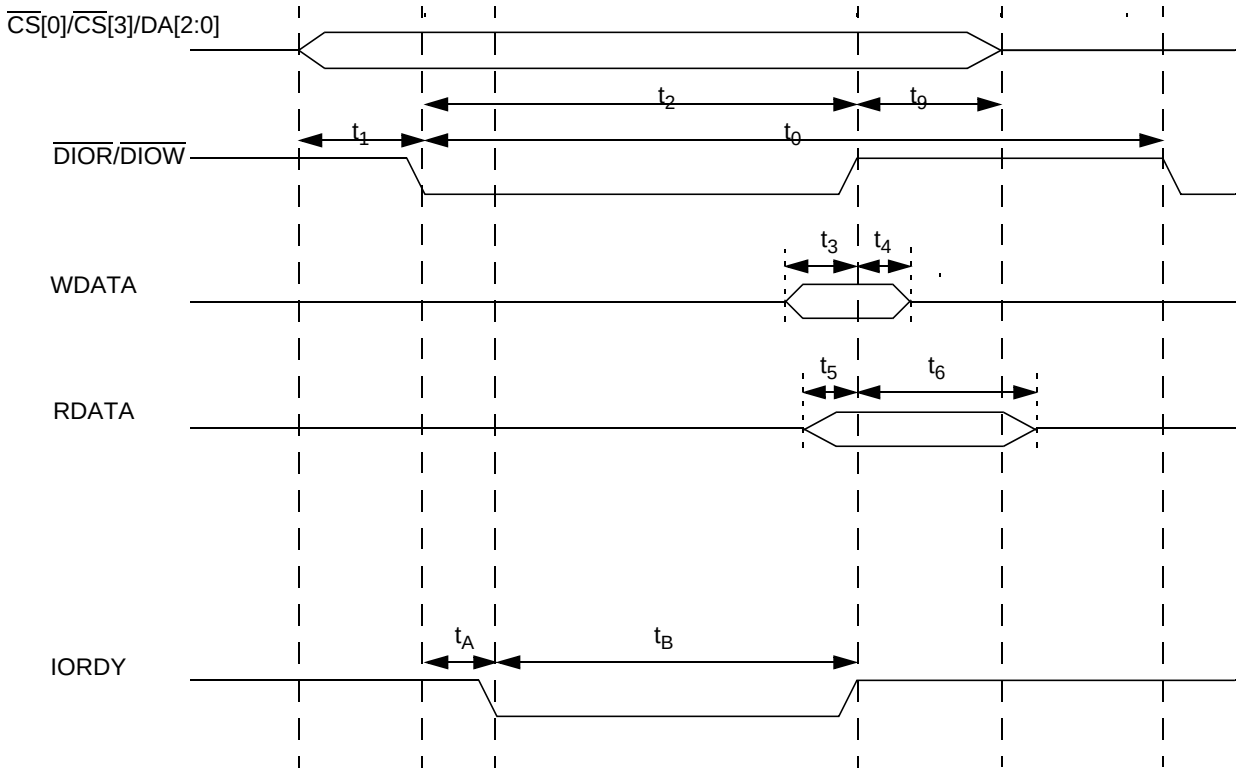


Figure 14. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

Sym	Multiword DMA Timing Parameters	Min/Max	Mode 0(ns)	Mode 1(ns)	Mode 2(ns)	SpecID
t_0	Cycle Time	min	480	150	120	A8.12
t_C	$\overline{\text{DMACK}}$ to DMARQ delay	max	—	—	—	A8.13
t_D	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width (16-bit)	min	215	80	70	A8.14
t_E	$\overline{\text{DIOR}}$ data access	max	150	60	50	A8.15
t_G	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ data setup	min	100	30	20	A8.16
t_F	$\overline{\text{DIOR}}$ data hold	min	5	5	5	A8.17
t_H	$\overline{\text{DIOW}}$ data hold	min	20	15	10	A8.18
t_I	DMACK to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	0	0	0	A8.19
t_J	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to $\overline{\text{DMACK}}$ hold	min	20	5	5	A8.20
t_{Kr}	$\overline{\text{DIOR}}$ negated pulse width	min	50	50	25	A8.21
t_{Kw}	$\overline{\text{DIOW}}$ negated pulse width	min	215	50	25	A8.22
t_{Lr}	$\overline{\text{DIOR}}$ to DMARQ delay	max	120	40	35	A8.23
t_{Lw}	$\overline{\text{DIOW}}$ to DMARQ delay	max	40	40	35	A8.24

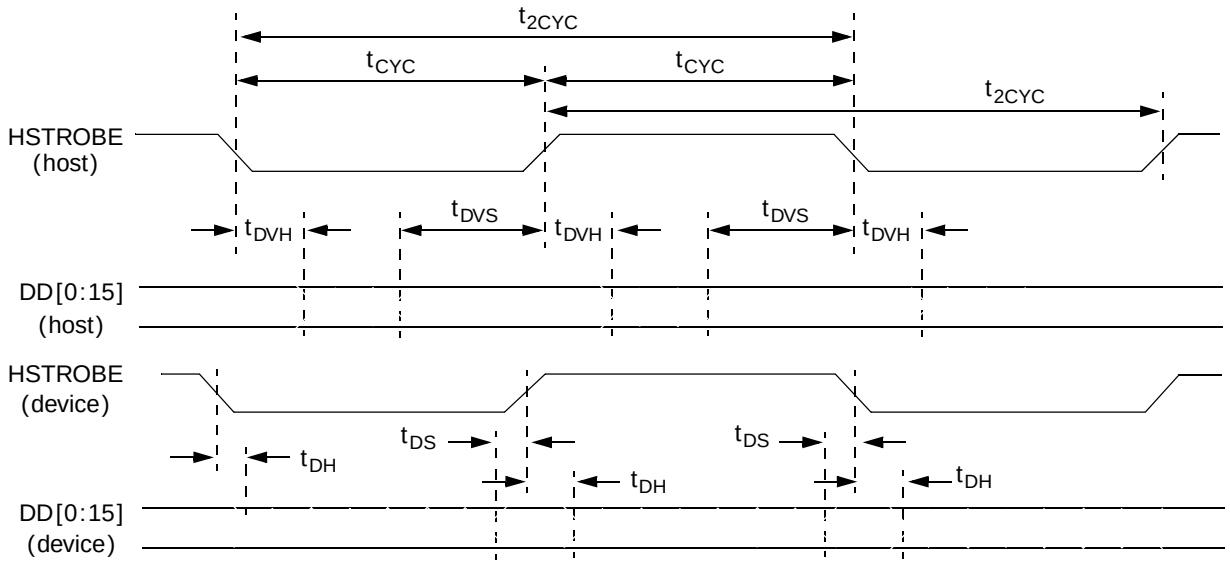


Figure 22. Timing Diagram—Sustained Ultra DMA Data Out Burst

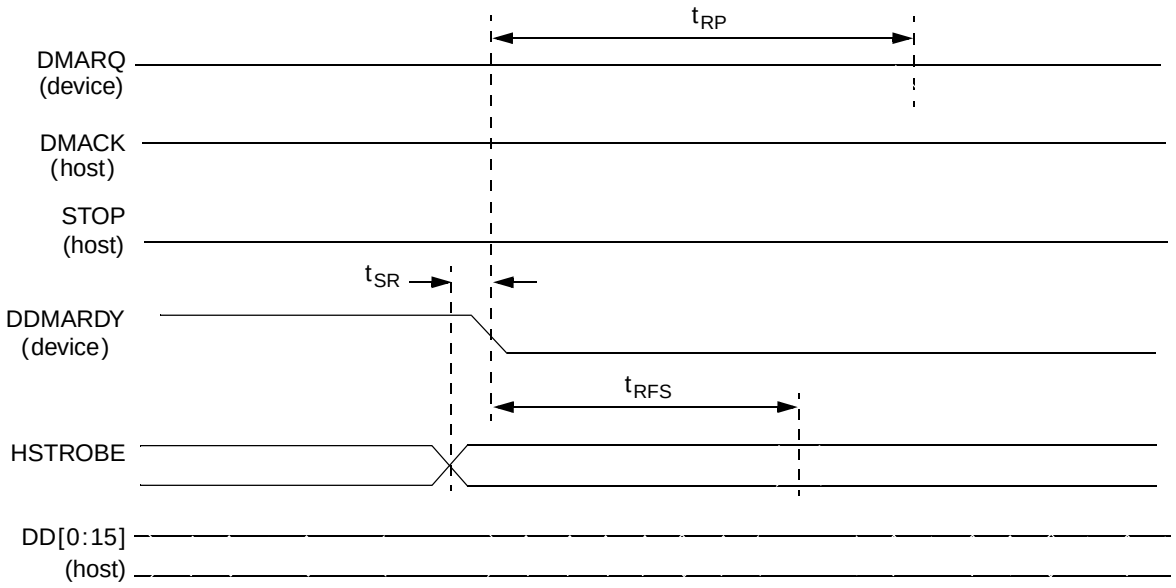


Figure 23. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

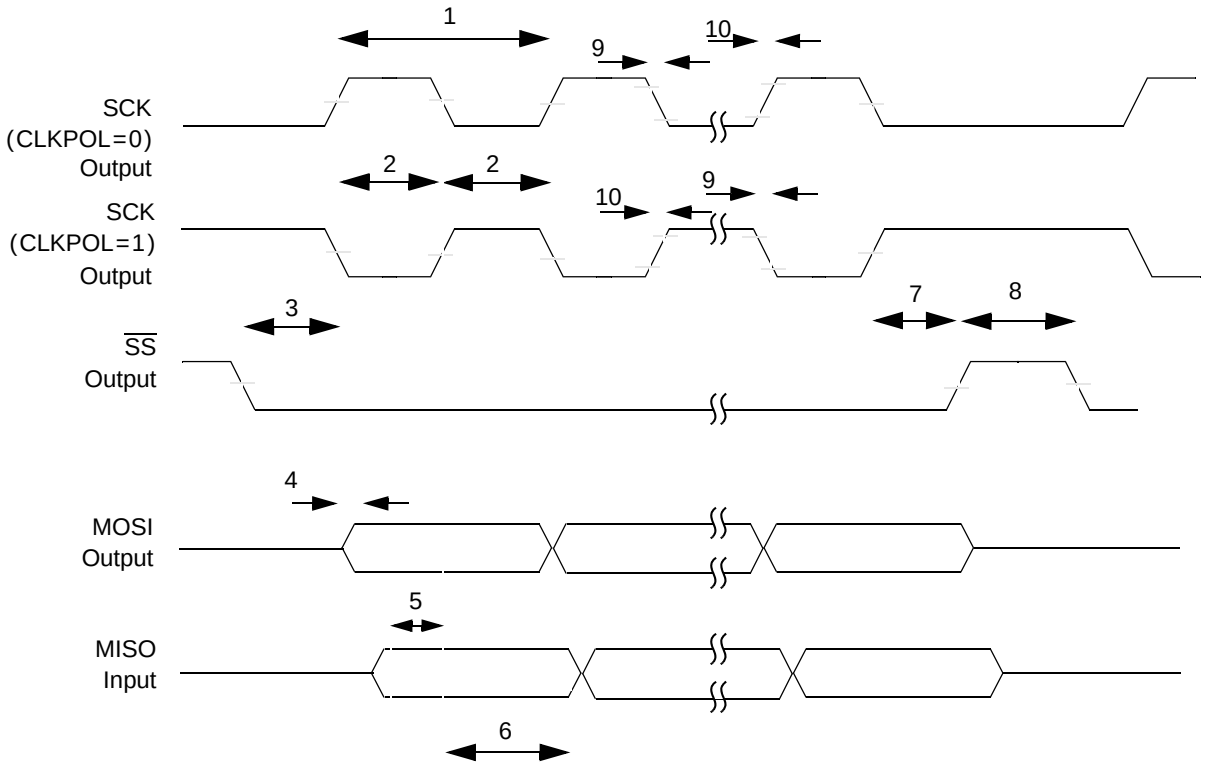


Figure 34. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 39. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle[1]	A11.31
2	Clock high or low time	2	512	IP-Bus Cycle[1]	A11.32
3	Slave select to clock delay	15.0	—	ns	A11.33
4	Output data valid	—	50.0	ns	A11.34
5	Input Data setup time	50.0	—	ns	A11.35
6	Input Data hold time	0.0	—	ns	A11.36
7	Slave disable lag time	15.0	—	ns	A11.37
8	Sequential Transfer delay	1	—	IP-Bus Cycle[1]	A11.38

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

Table 43. Timing Specifications — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	40.0	—	—	ns	A15.9
2	Clock duty cycle	—	50	—	%(1)	A15.10
3	FrameSync setup time	1.0	—	—	ns	A15.11
4	Output Data valid after clock edge	—	—	14.0	ns	A15.12
5	Input Data setup time	1.0	—	—	ns	A15.13
6	Input Data hold time	1.0	—	—	ns	A15.14

1 Bit Clock cycle time.

NOTE

Output timing is specified at a nominal 50 pF load.

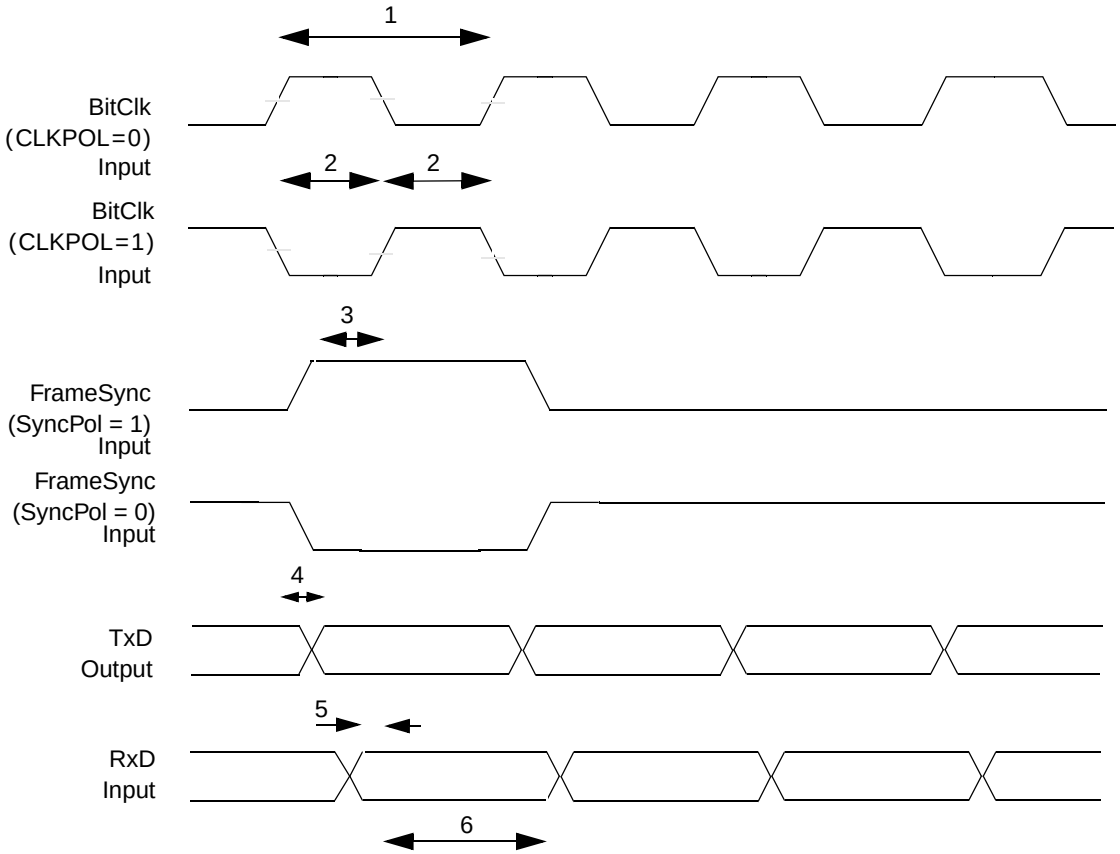


Figure 38. Timing Diagram — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

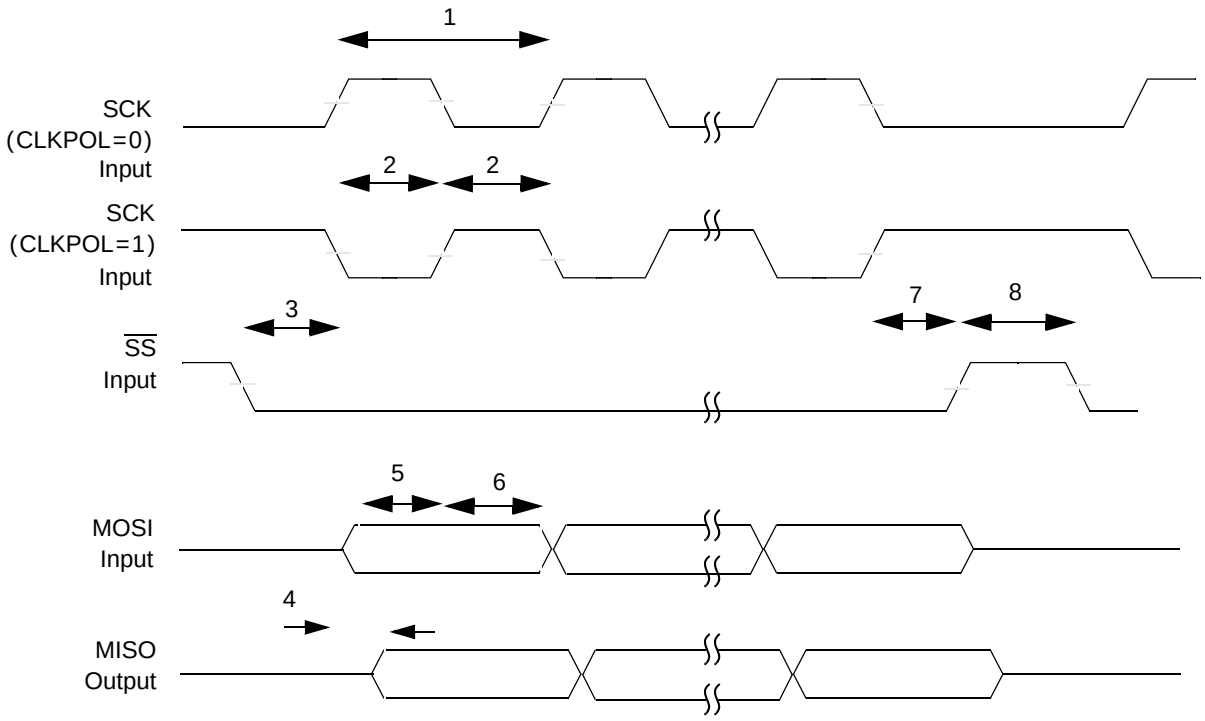


Figure 44. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

1.3.17 GPIOs and Timers

1.3.17.1 General and Asynchronous Signals

The MPC5200B contains several sets if I/Os that do not require special setup, hold, or valid requirements. Most of these are asynchronous to the system clock. The following numbers are provided for test and validation purposes only, and they assume a 133 MHz internal bus frequency.

Figure 45 shows the GPIO Timing Diagram. Table 50 gives the timing specifications.

Table 50. Asynchronous Signals

Sym	Description	Min	Max	Units	SpecID
t_{CK}	Clock Period	7.52	—	ns	A16.1
t_{IS}	Input Setup	12	—	ns	A16.2
t_{IH}	Input Hold	1	—	ns	A16.3
t_{DV}	Output Valid	—	15.33	ns	A16.4
t_{DH}	Output Hold	1	—	ns	A16.5

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, RTX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

3.3.2 Pull-up Requirements for the PCI Control Lines

If the PCI interface is NOT used (and internally disabled) the PCI control pins must be terminated as indicated by the PCI Local Bus specification. This is also required for MOST/Graphics and Large Flash Mode.

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

3.3.3 Pull-up/Pull-down Requirements for MEM_MDQS Pins (SDRAM)

The MEM_MDQS[3:0] signals are not used with SDR memories and require pull-up or pull-down resistors in SDRAM mode.

3.3.4 Pull-up/Pull-down Requirements for MEM_MDQS Pins (DDR 16-bit Mode)

The MEM_MDQS[1:0] signals are not used in DDR 16-bit mode and require pull-down resistors.

3.4 JTAG

The MPC5200B provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200B's embedded Freescale (formerly Motorola) MPC603e e300 processor. This interface provides a means for executing test routines and for performing software development and debug functions.

3.4.1 $\overline{\text{JTAG\_TRST}}$

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{JTAG\_TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

3.4.1.1 $\overline{\text{JTAG\_TRST}}$ and $\overline{\text{PORRESET}}$

The JTAG interface can control the direction of the MPC5200B I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5200B comes out of power-on reset; do this by asserting JTAG_TRST before $\overline{\text{PORRESET}}$ is released.

For more details refer to the Reset and JTAG Timing Specification.

Figure 53. $\overline{\text{PORRESET}}$ vs. $\overline{\text{JTAG\_TRST}}$

3.4.1.2 Connecting JTAG_TRST

The wiring of the $\overline{\text{JTAG\_TRST}}$ depends on the existence of a board-related debug interface. (see below)

To reset the MPC5200B via the COP connector, the HRESET pin of the COP should be connected to the HRESET pin of the MPC5200B. The circuitry shown in Figure 54 allows the COP to assert HRESET or JTAG_TRST separately, while any other board sources can drive PORRESET.

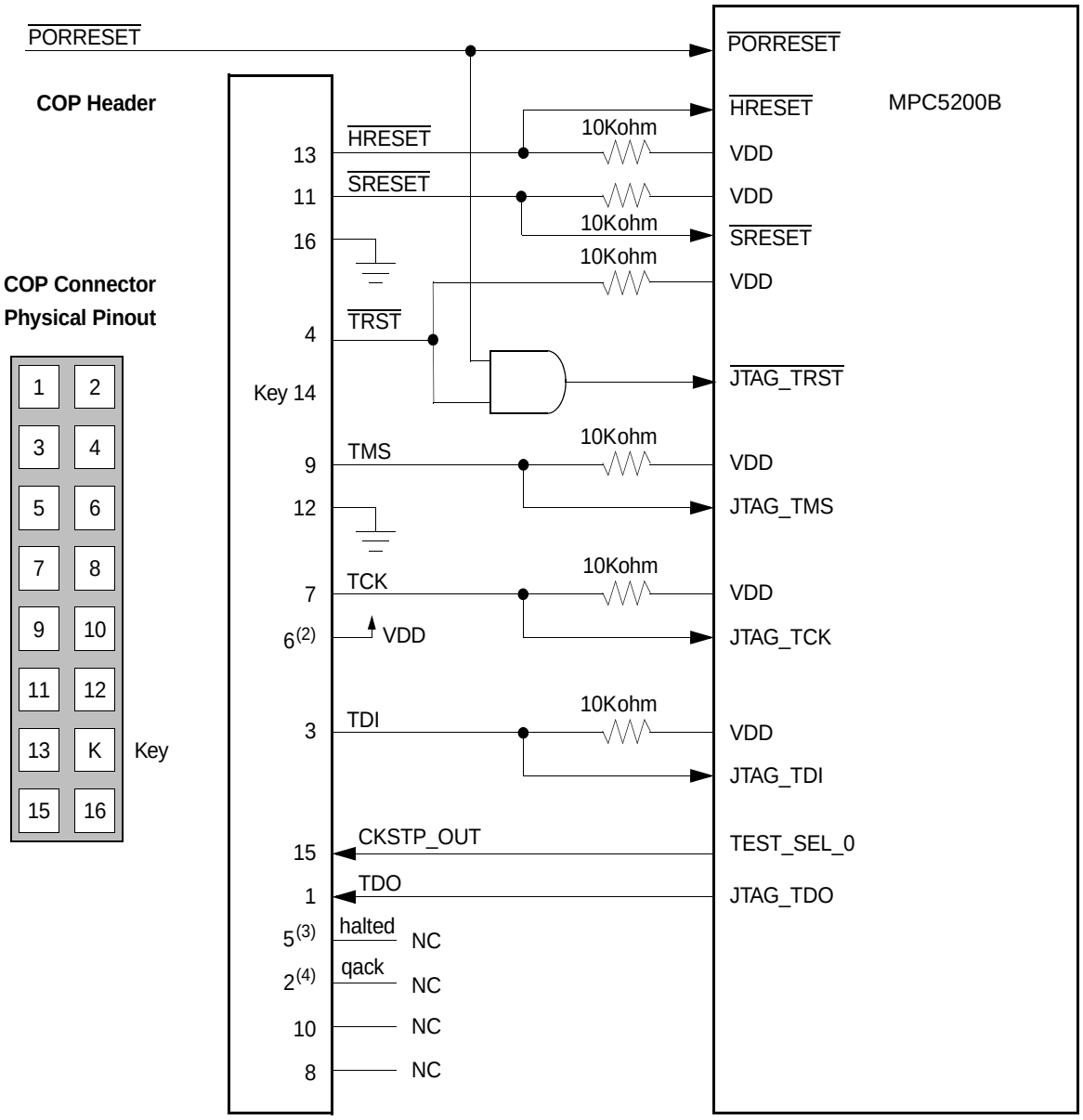


Figure 54. COP Connector Diagram

3.4.2.2 Boards Without COP Connector

If the JTAG interface is not used, JTAG_TRST should be tied to PORRESET, so that it is asserted when the system reset signal (PORRESET) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 55 shows the connection of the JTAG interface without COP connector.