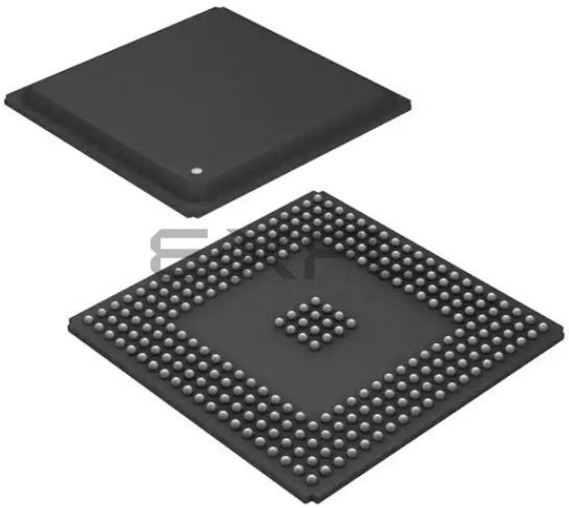

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cvr400b

Figure 1 shows a simplified MPC5200B block diagram.

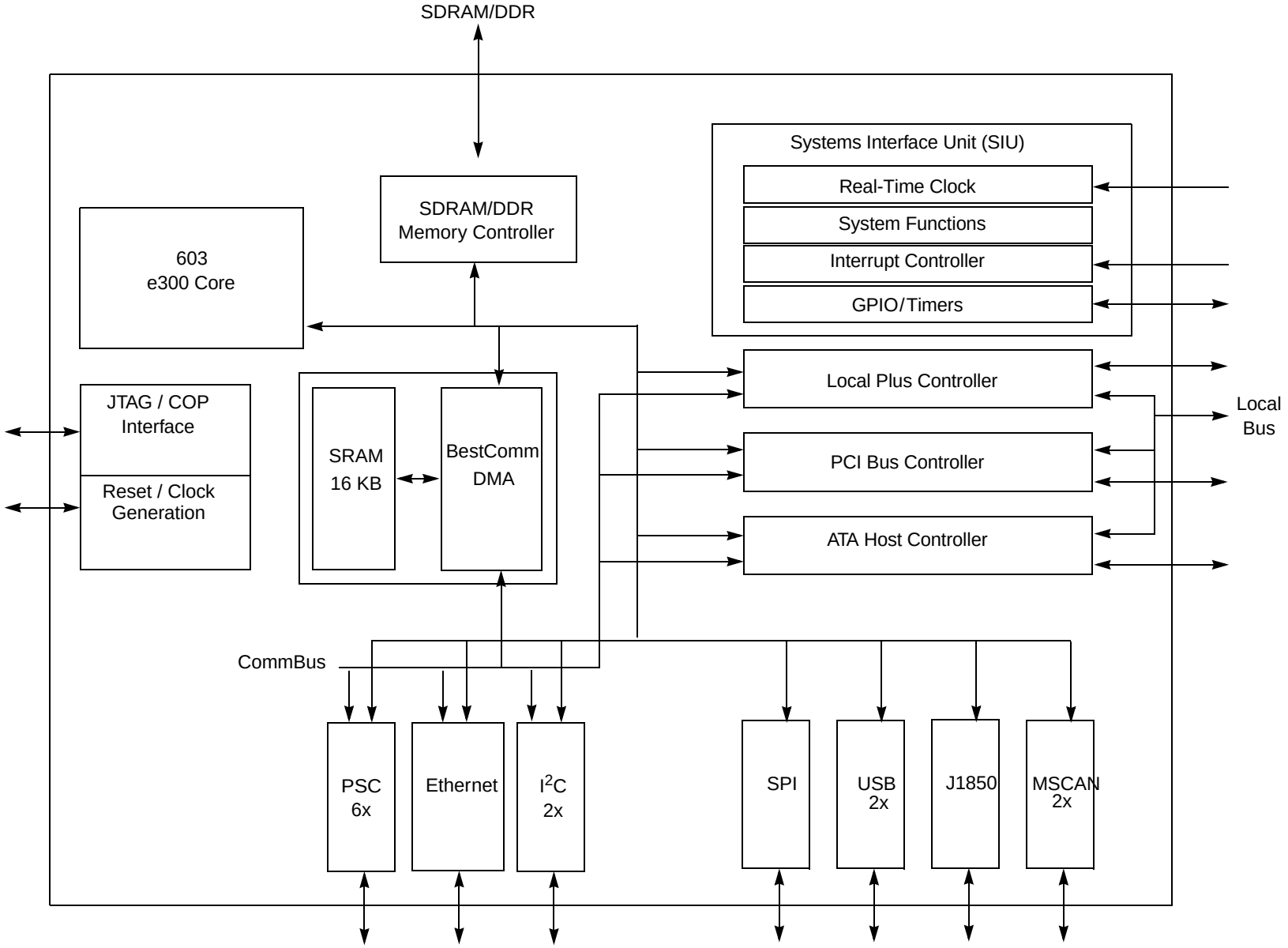


Figure 1. Simplified Block Diagram—MPC5200B

Table 2. Recommended Operating Conditions (continued)

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Input voltage — standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage — memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8
Input voltage — memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	–40	+85	^oC	D2.10
Die junction operating temperature range	Tj	–40	+115	^oC	D2.12

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 Maximum e300 core operating frequency is 400 MHz.

1.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200B at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL VDD_IO/$VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12
Input leakage current	Vin = 0 or VDD_IO/$VDD\_IO\_MEM_{SDR}$ (depending on input type[1])	I_{IN}	—	±2	μA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	μA	D3.14

1.1.6 Thermal Characteristics

Table 7. Thermal Resistance Data

Rating	Board Layers	Sym	Value	Unit	Notes	SpecID
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	30	°C/W	(1),(2)	D6.1
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	(1),(3)	D6.2
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W	(1),(3)	D6.3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	19	°C/W	(1),(3)	D6.4
Junction to Board	—	$R_{\theta JB}$	14	°C/W	(4)	D6.5
Junction to Case	—	$R_{\theta JC}$	8	°C/W	(5)	D6.6
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	(6)	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

1.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

1.2 Oscillator and PLL Electrical Characteristics

The MPC5200B System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200B clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

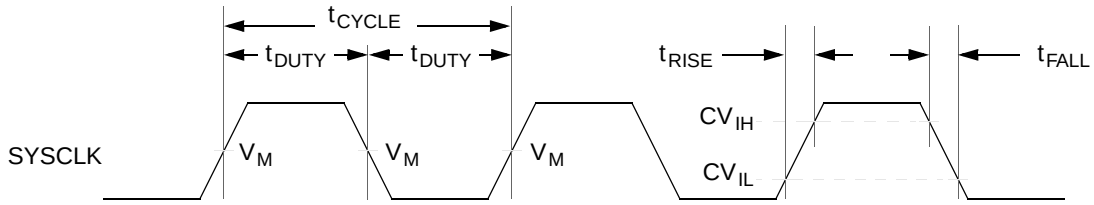


Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.(1)	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).(2)	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 —The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.

For additional information, see the *MPC5200B User's Manual (MPC5200BUM)*.

1.3.4.1 Reset Configuration Word

During reset ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) the Reset Configuration Word is latched in the related Reset Configuration Word Register with each rising edge of the SYS_XTAL signal. If both resets ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) are inactive (high), the contents of this register are locked immediately with the SYS_XTAL clock (see Figure 3).

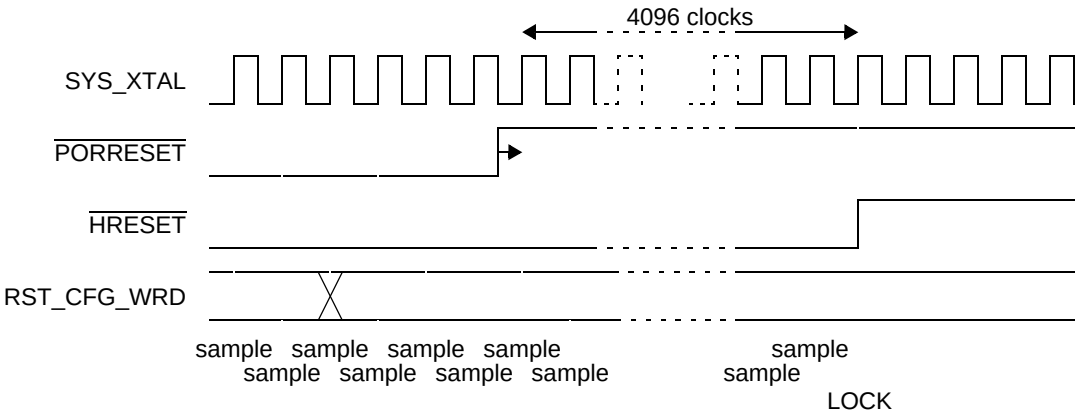


Figure 3. Reset Configuration Word Locking

NOTE

Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

1.3.5 External Interrupts

The MPC5200B provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:

2) The interrupt latency descriptions in the table above are related to non competitive, non masked but enabled external interrupt sources. Take care of interrupt prioritization which may increase the latencies.

Because all external interrupt signals are synchronized into the internal processor bus clock domain, each of these signals has to exceed a minimum pulse width of more than one IP_CLK cycle.

Table 17. Minimum Pulse Width for External Interrupts to be Recognized

Name	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
All external interrupts (IRQs, GPIOs)	> 1 clock cycle	—	IP_CLK	A4.22

NOTES:

1) The frequency of the IP_CLK depends on the register settings in Clock Distribution Module. See the *MPC5200B User's Manual (MPC5200BUM)* for further information.

2) If the same interrupt occurs a second time while its interrupt service routine has not cleared the former one, the second interrupt is not recognized at all.

Besides synchronization, prioritization, and mapping the latency of an external interrupt to the start of its associated interrupt service routine also depends on the following conditions: To get a minimum interrupt service response time, it is recommended to enable the instruction cache and set up the maximum core clock, XL bus, and IP bus frequencies (depending on board design and programming). In addition, it is advisable to execute an interrupt handler, which has been implemented in assembly code.

1.3.6 SDRAM

1.3.6.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.25 + 0.4$	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.25 – 0.7$	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7

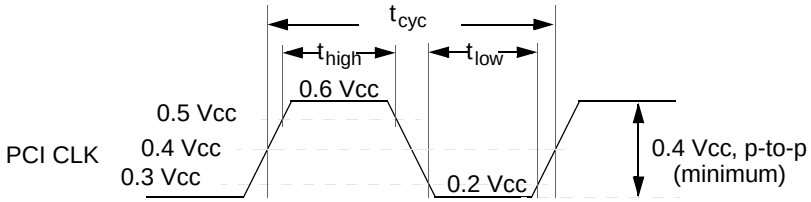


Figure 9. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{cyc}	PCI CLK Cycle Time	15	30	30	—	ns	(1),(3)	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	—	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	—	A6.3
—	PCI CLK Slew Rate	1.5	4	1	4	V/ns	(2)	A6.4
—	PCI Clock Jitter (peak to peak)	—	200	—	200	ps	—	—

NOTES:
1. In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{val}	CLK to Signal Valid Delay — bused signals	2	6	2	11	ns	(1),(2),(3)	A6.5
t_{val}(ptp)	CLK to Signal Valid Delay — point to point	2	6	2	12	ns	(1),(2),(3)	A6.6
t_{on}	Float to Active Delay	2	—	2	—	ns	(1)	A6.7
t_{off}	Active to Float Delay		14		28	ns	(1)	A6.8
t_{su}	Input Setup Time to CLK — bused signals	3	—	7	—	ns	(3),(4)	A6.9
t_{su}(ptp)	Input Setup Time to CLK — point to point	5	—	10,12	—	ns	(3),(4)	A6.10
t_h	Input Hold Time from CLK	0	—	0	—	ns	(4)	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

Table 25. Burst Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_9	DATA hold after rising edge of PCI clock	0	—	ns	—	A7.32
t_{10}	DATA hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(4)	A7.33
t_{11}	ACK assertion after CS assertion	—	(WS + 1) × t_{PCIck}	ns	—	A7.34
t_{12}	ACK negation before CS negation	—	7.0	ns	(3)	A7.35
t_{13}	ACK pulse width	4^{LB} × 2 × (32/DS) × t_{PCIck}	4^{LB} × 2 × (32/DS) × t_{PCIck}	ns	(2),(3)	A7.36
t_{14}	CS assertion after TS assertion	—	2.5	ns	—	A7.37
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	—	A7.38

NOTES:

1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => 4^1 × 2 × (32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1 + 10 + 32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.
4. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

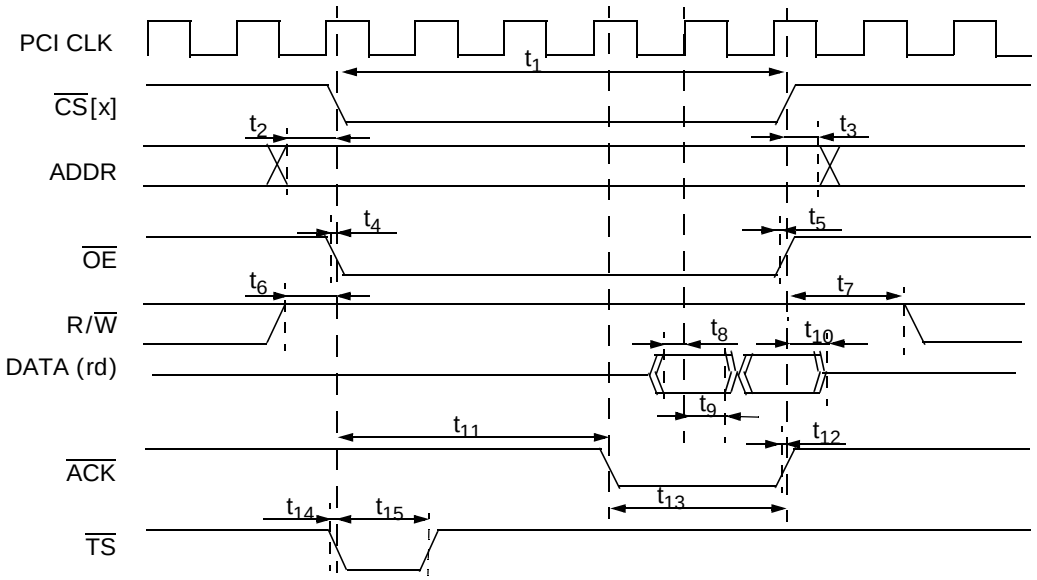


Figure 12. Timing Diagram—Burst Mode

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5200B operating frequency (IP bus clock frequency)
- Internal MPC5200B bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5200B. See the *MPC5200B User's Manual (MPC5200B)*.

NOTE

All output timing numbers are specified for nominal 50 pF loads.

Table 27. PIO Mode Timing Specifications

Sym	PIO Timing Parameter	Min/Max (ns)	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	SpecID
t_0	Cycle Time	min	600	383	240	180	120	A8.1
t_1	Address valid to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	70	50	30	30	25	A8.2
t_2	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width 16-bit 8-bit	min min	165 290	125 290	100 290	80 80	70 70	A8.3
t_{2i}	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ recovery time	min	—	—	—	70	25	A8.4
t_3	$\overline{\text{DIOW}}$ data setup	min	60	45	30	30	20	A8.5
t_4	$\overline{\text{DIOW}}$ data hold	min	30	20	15	10	10	A8.6
t_5	$\overline{\text{DIOR}}$ data setup	min	50	35	20	20	20	A8.7
t_6	$\overline{\text{DIOR}}$ data hold	min	5	5	5	5	5	A8.8
t_9	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to address valid hold	min	20	15	10	10	10	A8.9
t_A	IORDY setup	max	35	35	35	35	35	A8.10
t_B	IORDY pulse width	max	1250	1250	1250	1250	1250	A8.11

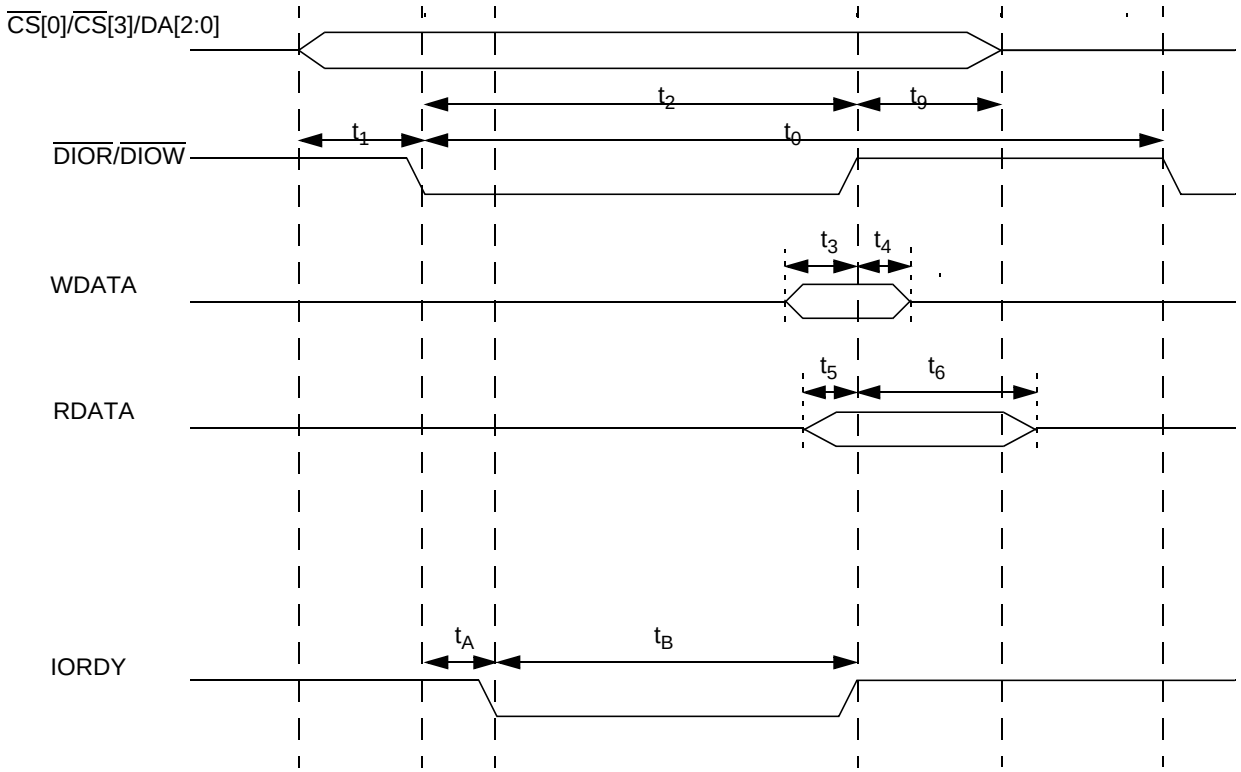


Figure 14. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

Sym	Multiword DMA Timing Parameters	Min/Max	Mode 0(ns)	Mode 1(ns)	Mode 2(ns)	SpecID
t_0	Cycle Time	min	480	150	120	A8.12
t_C	$\overline{\text{DMACK}}$ to DMARQ delay	max	—	—	—	A8.13
t_D	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ pulse width (16-bit)	min	215	80	70	A8.14
t_E	$\overline{\text{DIOR}}$ data access	max	150	60	50	A8.15
t_G	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ data setup	min	100	30	20	A8.16
t_F	$\overline{\text{DIOR}}$ data hold	min	5	5	5	A8.17
t_H	$\overline{\text{DIOW}}$ data hold	min	20	15	10	A8.18
t_I	DMACK to $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ setup	min	0	0	0	A8.19
t_J	$\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ to $\overline{\text{DMACK}}$ hold	min	20	5	5	A8.20
t_{Kr}	$\overline{\text{DIOR}}$ negated pulse width	min	50	50	25	A8.21
t_{Kw}	$\overline{\text{DIOW}}$ negated pulse width	min	215	50	25	A8.22
t_{Lr}	$\overline{\text{DIOR}}$ to DMARQ delay	max	120	40	35	A8.23
t_{Lw}	$\overline{\text{DIOW}}$ to DMARQ delay	max	40	40	35	A8.24

Table 30. Timing Specification ata_isolation

Sym	Description	Min	Max	Units	SpecID
1	ata_isolation setup time	7	—	IP Bus cycles	A8.48
2	ata_isolation hold time	—	19	IP Bus cycles	A8.49

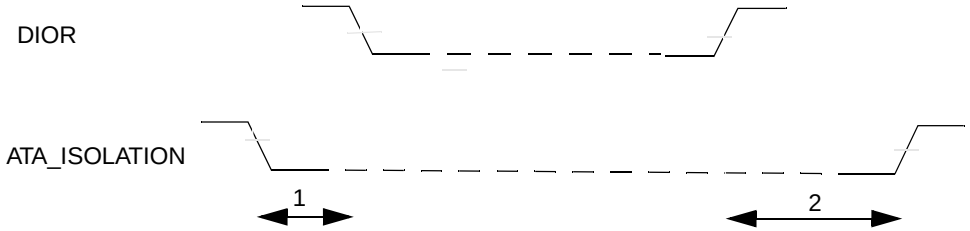


Figure 26. Timing Diagram—ATA-ISOLATION

1.3.10 Ethernet

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 31. MII Rx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	10	—	ns	A9.1
t_2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	10	—	ns	A9.2
t_3	RX_CLK pulse width high	35%	65%	RX_CLK Period(1)	A9.3
t_4	RX_CLK pulse width low	35%	65%	RX_CLK Period(1)	A9.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

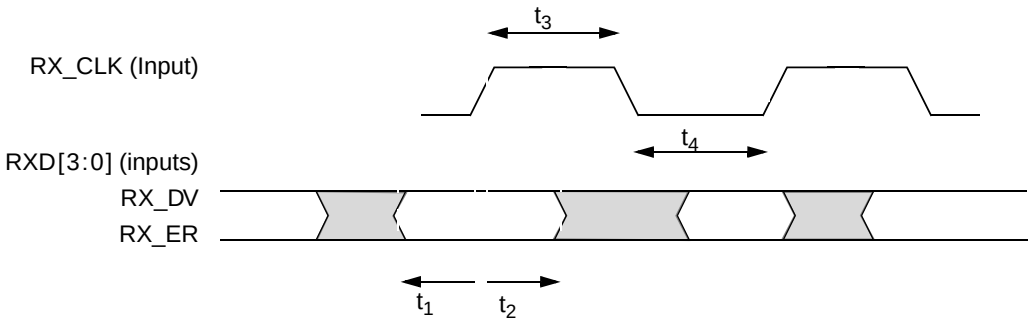


Figure 27. Ethernet Timing Diagram—MII Rx Signal

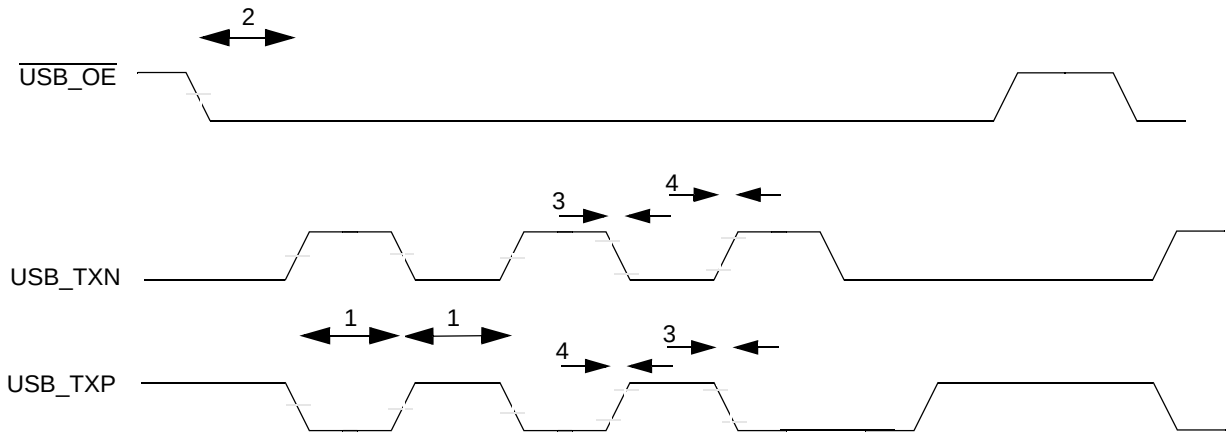


Figure 31. Timing Diagram—USB Output Line

1.3.12 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	Cycle time	4	1024	IP-Bus Cycle(1)	A11.1
2	Clock high or low time	2	512	IP-Bus Cycle(1)	A11.2
3	Slave select to clock delay	15.0	—	ns	A11.3
4	Output Data valid after Slave Select ($\overline{SS}$)	—	20.0	ns	A11.4
5	Output Data valid after SCK	—	20.0	ns	A11.5
6	Input Data setup time	20.0	—	ns	A11.6
7	Input Data hold time	20.0	—	ns	A11.7
8	Slave disable lag time	15.0	—	ns	A11.8
9	Sequential transfer delay	1	—	IP-Bus Cycle(1)	A11.9
10	Clock falling time	—	7.9	ns	A11.10
11	Clock rising time	—	7.9	ns	A11.11

1 Inter Peripheral Clock is defined in the *MPC5200B User's Manual (MPC5200BUM)*.

NOTE

Output timing is specified at a nominal 50 pF load.

Table 43. Timing Specifications — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	40.0	—	—	ns	A15.9
2	Clock duty cycle	—	50	—	%(1)	A15.10
3	FrameSync setup time	1.0	—	—	ns	A15.11
4	Output Data valid after clock edge	—	—	14.0	ns	A15.12
5	Input Data setup time	1.0	—	—	ns	A15.13
6	Input Data hold time	1.0	—	—	ns	A15.14

1 Bit Clock cycle time.

NOTE

Output timing is specified at a nominal 50 pF load.

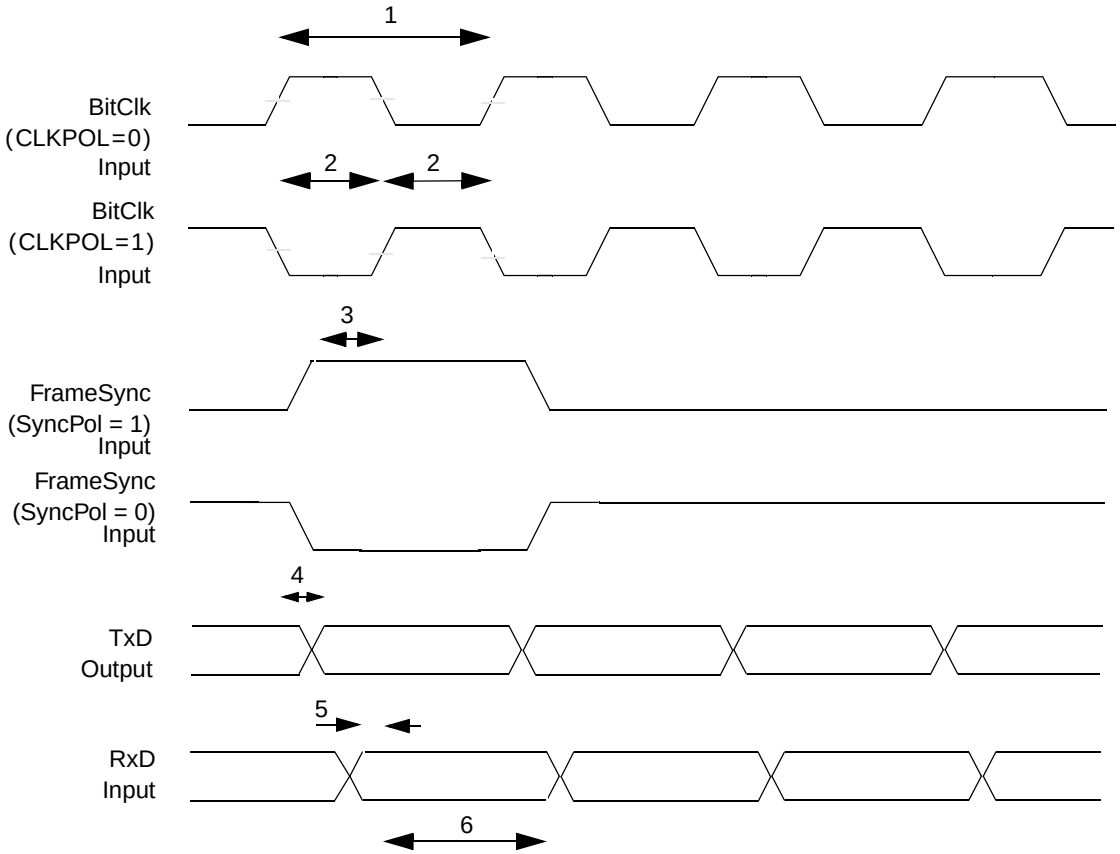


Figure 38. Timing Diagram — 8-, 16-, 24-, and 32-bit CODEC / I²S Slave Mode

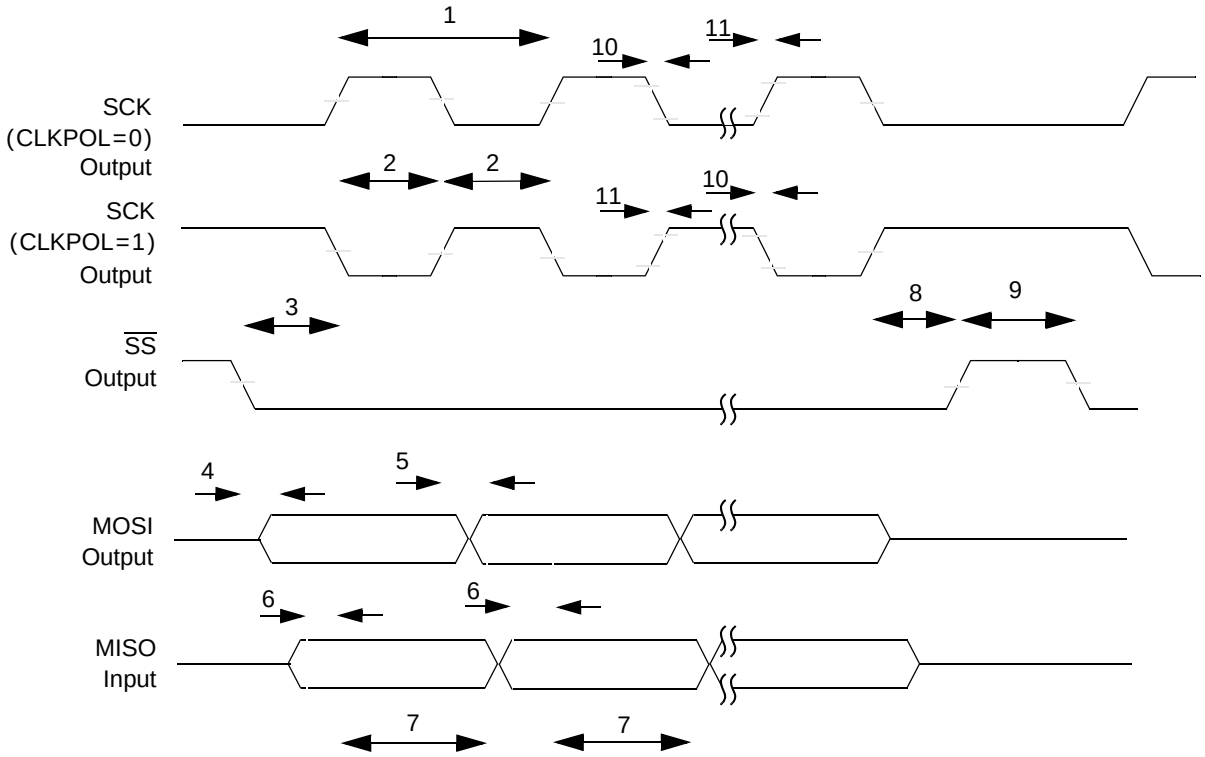


Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.38
3	Slave select clock delay	1.0	—	ns	A15.39
4	Input Data setup time	1.0	—	ns	A15.40
5	Input Data hold time	1.0	—	ns	A15.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A15.42
7	Output data valid after SCK	—	14.0	ns	A15.43
8	Slave disable lag time	0.0	—	ns	A15.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A15.45

NOTE

Output timing is specified at a nominal 50 pF load.

1.3.18 IEEE 1149.1 (JTAG) AC Specifications

Table 51. JTAG Timing Specification

Sym	Characteristic	Min	Max	Unit	SpecID
—	TCK frequency of operation.	0	25	MHz	A17.1
1	TCK cycle time.	40	—	ns	A17.2
2	TCK clock pulse width measured at 1.5V.	1.08	—	ns	A17.3
3	TCK rise and fall times.	0	3	ns	A17.4
4	$\overline{\text{TRST}}$ setup time to tck falling edge(1).	10	—	ns	A17.5
5	$\overline{\text{TRST}}$ assert time.	5	—	ns	A17.6
6	Input data setup time(2).	5	—	ns	A17.7
7	Input data hold time(2).	15	—	ns	A17.8
8	TCK to output data valid(3).	0	30	ns	A17.9
9	TCK to output high impedance(3).	0	30	ns	A17.10
10	TMS, TDI data setup time.	5	—	ns	A17.11
11	TMS, TDI data hold time.	1	—	ns	A17.12
12	TCK to TDO data valid.	0	15	ns	A17.13
13	TCK to TDO high impedance.	0	15	ns	A17.14

1 $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

2 Non-test, other than TDI and TMS, signal input timing with respect to TCK.

3 Non-test, other than TDO, signal output timing with respect to TCK.

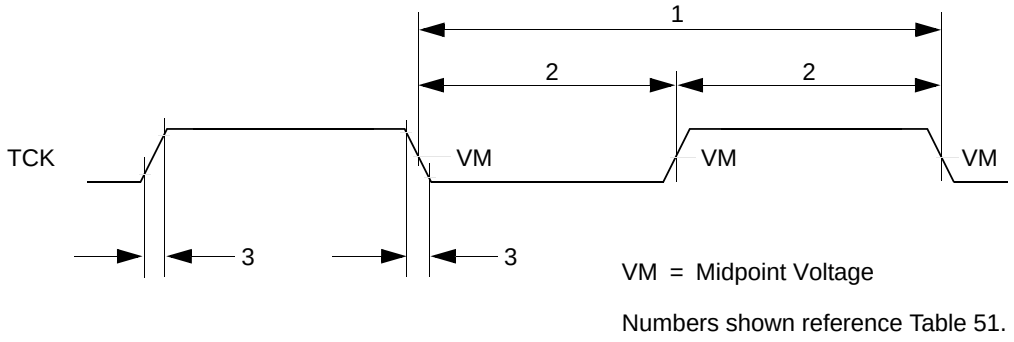


Figure 46. Timing Diagram—JTAG Clock Input

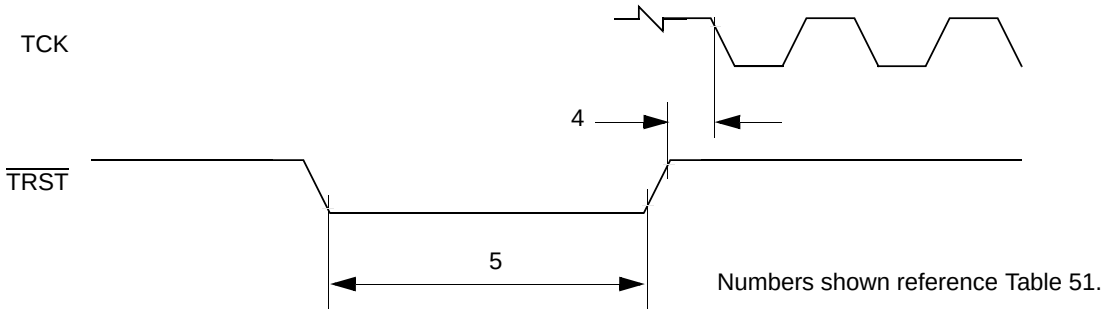
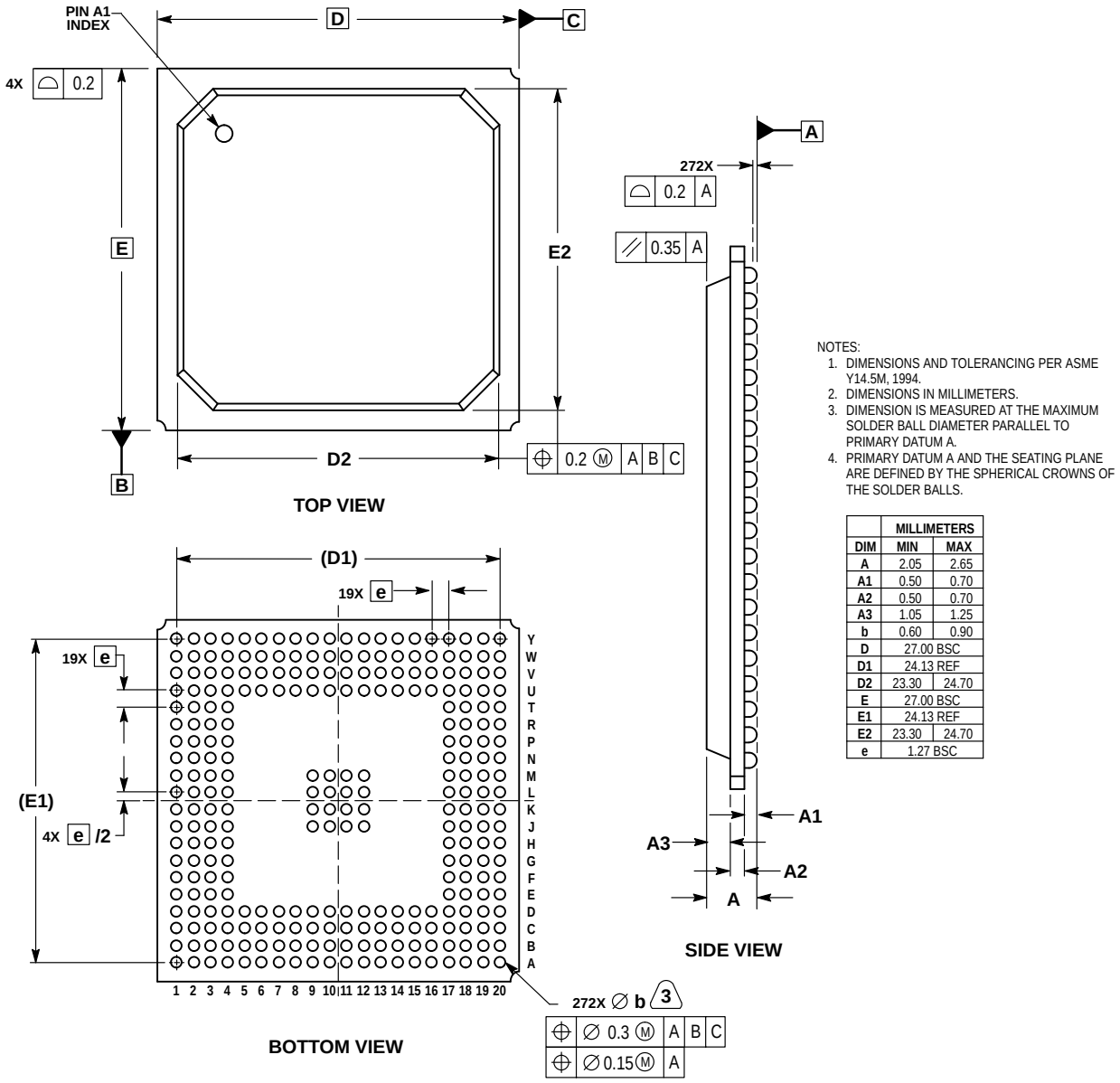


Figure 47. Timing Diagram—JTAG TRST

2.2 Mechanical Dimensions

Figure 50 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC5200B, 272 TE-PBGA package.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135A–01
ISSUE B

Figure 50. Mechanical Dimensions and Pinout Assignments for the MPC5200B, 272 TE-PBGA

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
PCI_TRDY		I/O	VDD_IO	PCI	PCI	
Local Plus						
LP_ACK		I/O	VDD_IO	DRV8	TTL	PULLUP
LP_ALE		I/O	VDD_IO	DRV8	TTL	
LP_OE		I/O	VDD_IO	DRV8	TTL	
LP_RW		I/O	VDD_IO	DRV8	TTL	
LP_TS		I/O	VDD_IO	DRV8	TTL	
LP_CS0		I/O	VDD_IO	DRV8	TTL	
LP_CS1		I/O	VDD_IO	DRV8	TTL	
LP_CS2		I/O	VDD_IO	DRV8	TTL	
LP_CS3		I/O	VDD_IO	DRV8	TTL	
LP_CS4		I/O	VDD_IO	DRV8	TTL	
LP_CS5		I/O	VDD_IO	DRV8	TTL	
ATA						
ATA_DACK		I/O	VDD_IO	DRV8	TTL	
ATA_DRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_INTRQ		I/O	VDD_IO	DRV8	TTL	PULLDOWN
ATA_IOCHRDY		I/O	VDD_IO	DRV8	TTL	PULLUP
ATA_IOR		I/O	VDD_IO	DRV8	TTL	
ATA_IOW		I/O	VDD_IO	DRV8	TTL	
ATA_ISOLATION		I/O	VDD_IO	DRV8	TTL	
Ethernet						
ETH_0	TX, TX_EN	I/O	VDD_IO	DRV4	TTL	
ETH_1	RTS, TXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_2	USB_TXP, RTX, TXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_3	USB_PRTPWR, TXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_4	USB_SPEED, TXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_5	USB_SUPEND, TX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_6	USB_OE, RTS, MDC	I/O	VDD_IO	DRV4	TTL	
ETH_7	TXN, MDIO	I/O	VDD_IO	DRV4	TTL	

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Table 52. MPC5200B Pinout Listing (continued)

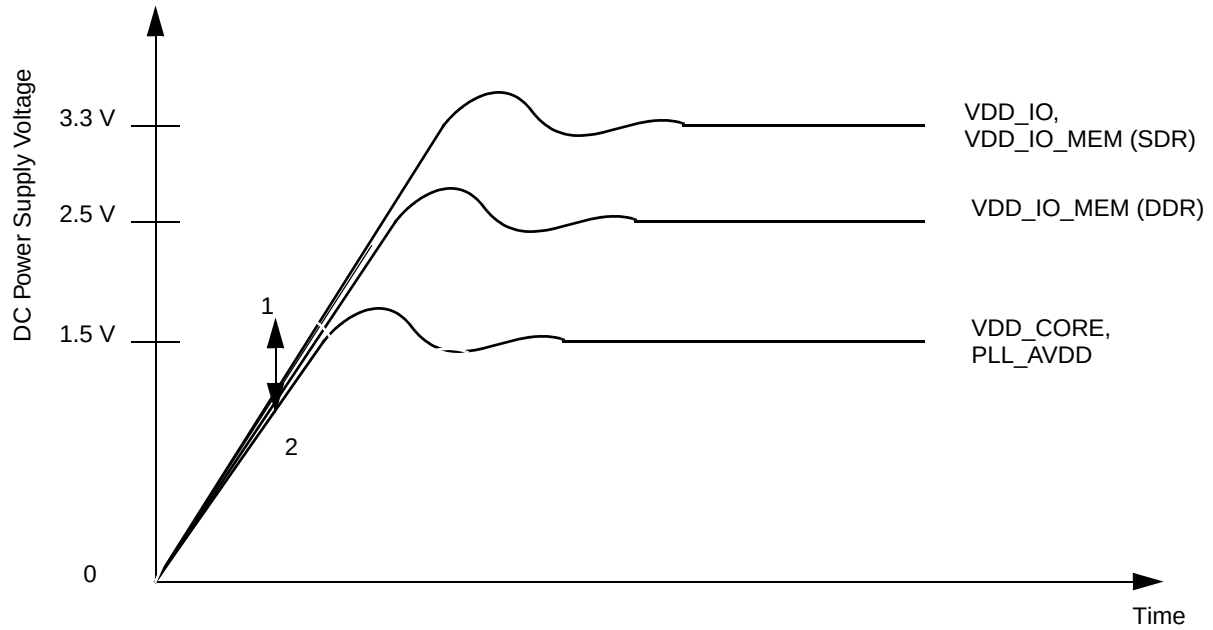
Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
VDD_MEM_IO		—				
VDD_CORE		—				
VSS_IO/CORE		—				
SYS_PLL_AVDD		—				
CORE_PLL_AVDD		—				

1 All “open drain” outputs of the MPC5200B are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200B I/O power rail if the external signal is driven above the MPC5200B I/O power rail voltage.

3 System Design Information

3.1 Power Up/Down Sequencing

Figure 51 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).



Note: VDD_CORE should not exceed VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V at any time, including power-up.

Note: It is recommended that VDD_CORE/PLL_AVDD should track VDD_IO/VDD_IO_MEM up to 0.9 V then separate for completion of ramps.

Note: Input voltage must not be greater than the supply voltage (VDD_IO) VDD_IO_MEM, VDD_CORE, or PLL_AVDD) by more than 0.5 V at any time, including during power-up.

Note: Use 1 microsecond or slower rise time for all supplies.

Figure 51. Supply Voltage Sequencing