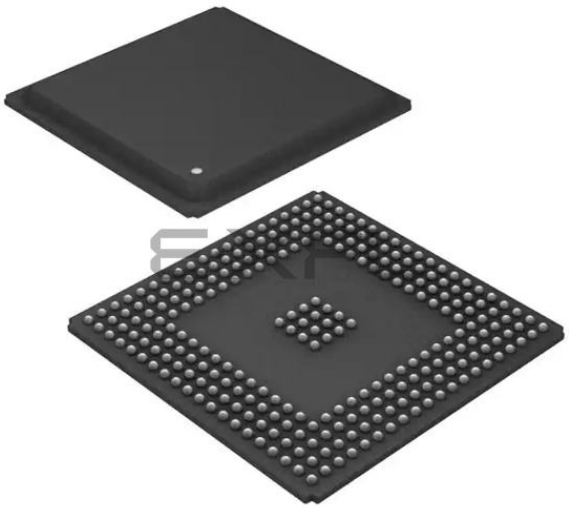

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5200cvr400br2

Figure 1 shows a simplified MPC5200B block diagram.

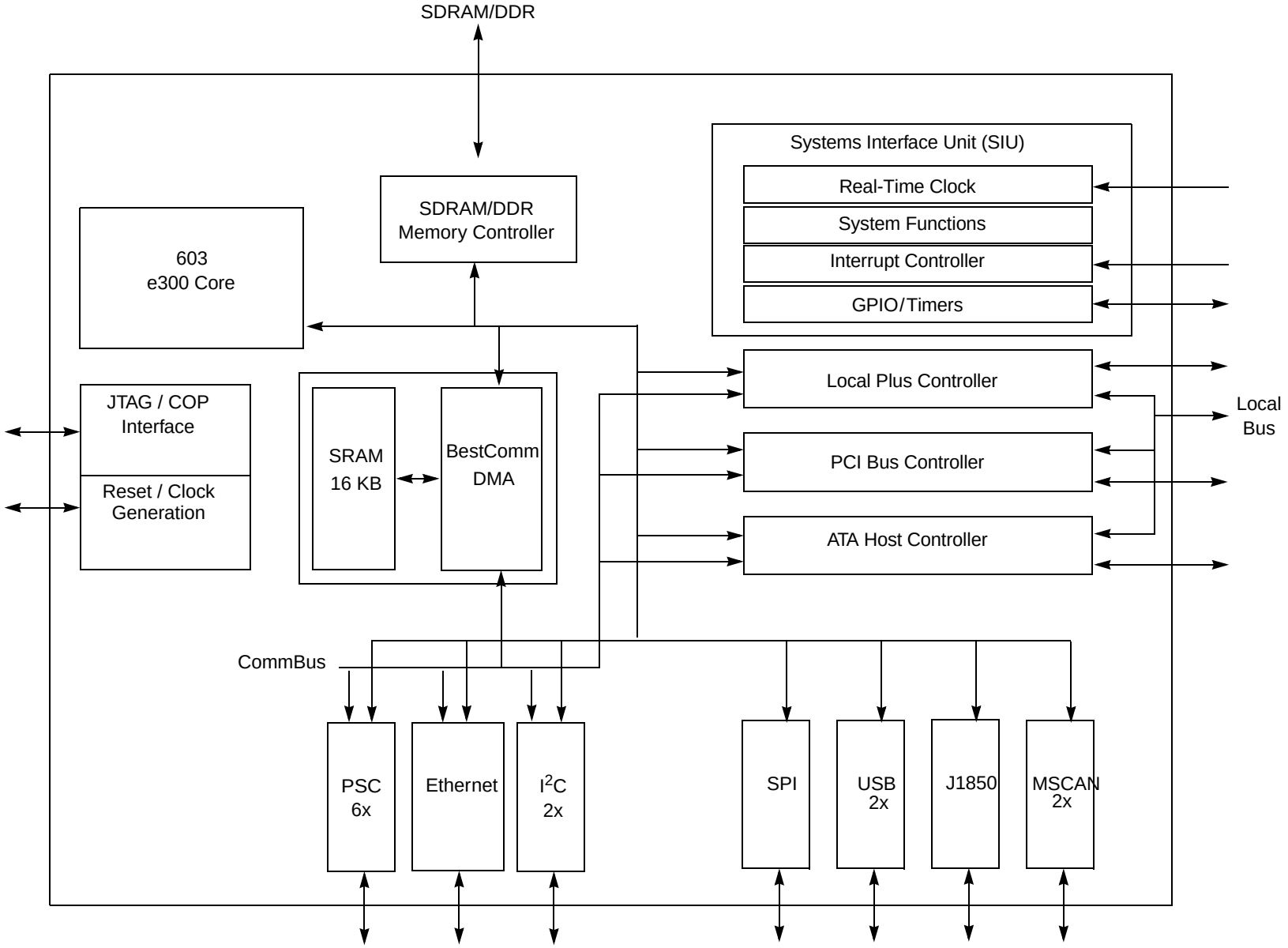


Figure 1. Simplified Block Diagram—MPC5200B

1 Electrical and Thermal Characteristics

1.1 DC Electrical Characteristics

1.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200B DC Electrical characteristics. Table 1 gives the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Sym	Min	Max	Unit	SpecID
Supply voltage — e300 core and peripheral logic	VDD_CORE	–0.3	1.8	V	D1.1
Supply voltage — I/O buffers	VDD_IO, VDD_MEM_IO	–0.3	3.6	V	D1.2
Supply voltage — System APLL	SYS_PLL_AVDD	–0.3	2.1	V	D1.3
Supply voltage — e300 APLL	CORE_PLL_AVDD	–0.3	2.1	V	D1.4
Input voltage (VDD_IO)	Vin	–0.3	VDD_IO + 0.3	V	D1.5
Input voltage (VDD_MEM_IO)	Vin	–0.3	VDD_MEM_IO + 0.3	V	D1.6
Input voltage overshoot	Vinos	—	1.0	V	D1.7
Input voltage undershoot	Vinus	—	1.0	V	D1.8
Storage temperature range	Tstg	–55	150	^{0}C	D1.9

1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

1.1.2 Recommended Operating Conditions

Table 2 gives the recommended operating conditions.

Table 2. Recommended Operating Conditions

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Supply voltage — e300 core and peripheral logic	VDD_CORE	1.42	1.58	V	D2.1
Supply voltage — standard I/O buffers	VDD_IO	3.0	3.6	V	D2.2
Supply voltage — memory I/O buffers (SDR)	$VDD\_MEM\_IO_{SDR}$	3.0	3.6	V	D2.3
Supply voltage — memory I/O buffers (DDR)	$VDD\_MEM\_IO_{DDR}$	2.42	2.63	V	D2.4
Supply voltage — System APLL	SYS_PLL_AVDD	1.42	1.58	V	D2.5
Supply voltage — e300 APLL	CORE_PLL_AVDD	1.42	1.58	V	D2.6

Table 11. e300 PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
e300 frequency	f_{core}	(1)	50	—	550	MHz	O4.1
e300 cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
e300 VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
e300 input clock frequency	f_{XLB_CLK}	—	25	—	367	MHz	O4.4
e300 input clock cycle time	t_{XLB_CLK}	—	2.73	—	50.0	ns	O4.5
e300 input clock jitter	t_{jitter}	(2)	—	—	150	ps	O4.6
e300 PLL relock time	t_{lock}	(3)	—	—	100	µs	O4.7

1 The XLB_CLK frequency and e300 PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in Table 12.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

1.3.1 AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = –40 to 85 ^oC
- Tj = –40 to 115 ^oC
- VDD_CORE = 1.42 to 1.58 V
  VDD_IO = 3.0 to 3.6 V

For additional information, see the *MPC5200B User's Manual (MPC5200BUM)*.

1.3.4.1 Reset Configuration Word

During reset ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) the Reset Configuration Word is latched in the related Reset Configuration Word Register with each rising edge of the SYS_XTAL signal. If both resets ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) are inactive (high), the contents of this register are locked immediately with the SYS_XTAL clock (see Figure 3).

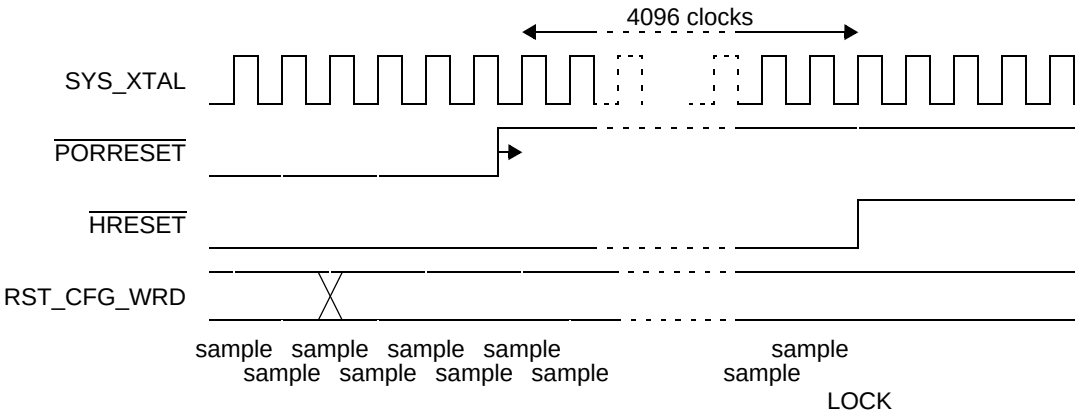


Figure 3. Reset Configuration Word Locking

NOTE

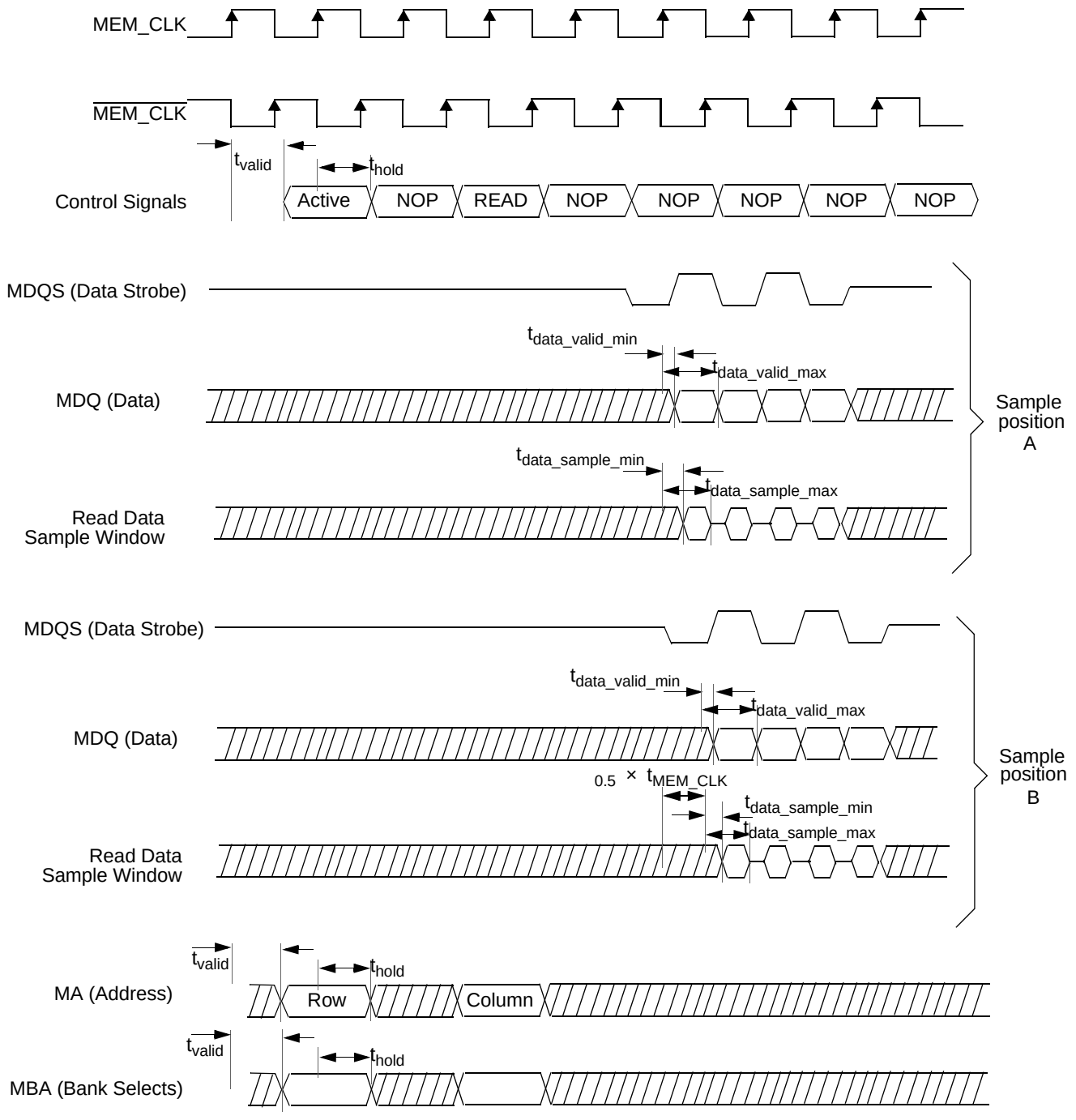
Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

1.3.5 External Interrupts

The MPC5200B provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data
Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the valid MDQS signal

NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

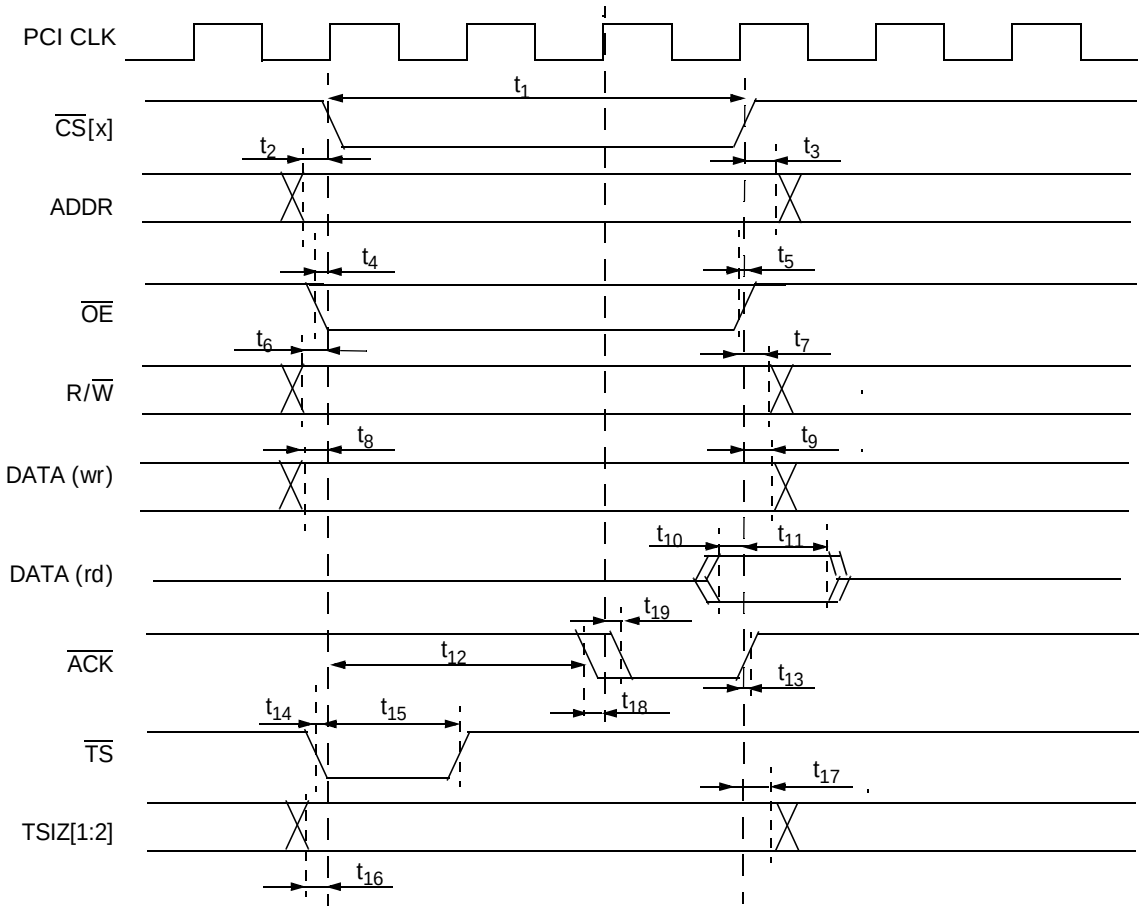


Figure 11. Timing Diagram—Non-MUXed Mode

1.3.8.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.22
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.23
t_1	CS pulse width	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	ns	(1),(2)	A7.24
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.25
t_3	ADDR hold after CS negation	–0.7	—	ns	—	A7.26
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.27
t_5	OE negation before CS negation	—	2.7	ns	—	A7.28
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.29
t_7	RW hold after CS negation	t_{PCIck}	—	ns	—	A7.30
t_8	DATA setup before rising edge of PCI clock	3.6	—	ns	—	A7.31

Table 25. Burst Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_9	DATA hold after rising edge of PCI clock	0	—	ns	—	A7.32
t_{10}	DATA hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(4)	A7.33
t_{11}	ACK assertion after CS assertion	—	(WS + 1) × t_{PCIck}	ns	—	A7.34
t_{12}	ACK negation before CS negation	—	7.0	ns	(3)	A7.35
t_{13}	ACK pulse width	4^{LB} × 2 × (32/DS) × t_{PCIck}	4^{LB} × 2 × (32/DS) × t_{PCIck}	ns	(2),(3)	A7.36
t_{14}	CS assertion after TS assertion	—	2.5	ns	—	A7.37
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	—	A7.38

NOTES:

1. Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. Example:
   Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
   Data bus width is 8 bit. => DS = 8
   => 4^1 × 2 × (32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
   Wait State is set to 10. => WS = 10
   1 + 10 + 32 = 43 => CS is asserted for 43 PCI cycles.
3. ACK is output and indicates the burst.
4. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

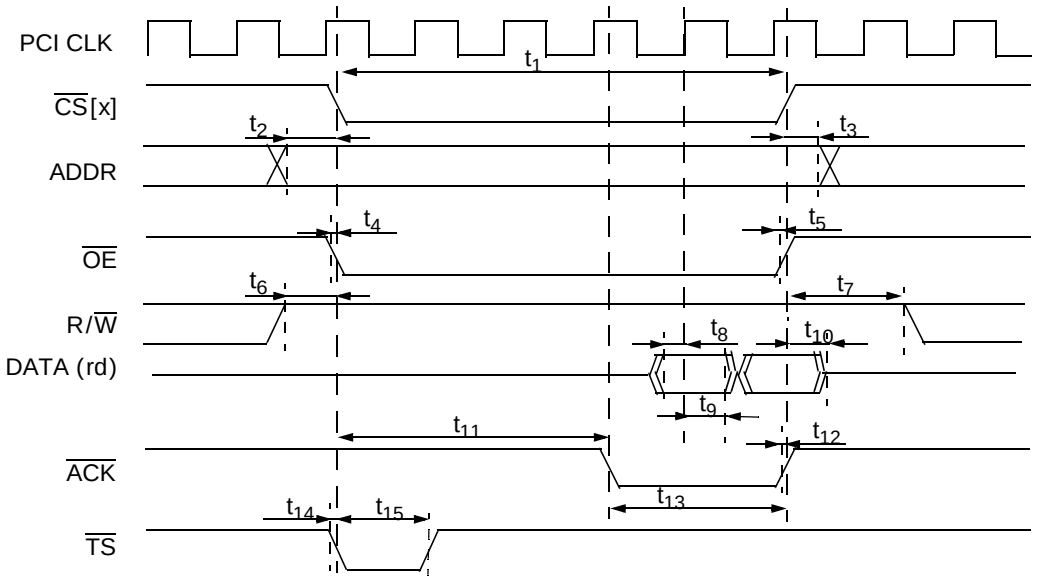


Figure 12. Timing Diagram—Burst Mode

Table 29. Ultra DMA Timing Specification (continued)

Sym	MODE 0 (ns)		MODE 1 (ns)		MODE 2 (ns)		Comment	SpecID
	Min	Max	Min	Max	Min	Max		
t_{AZ}	—	10	—	10	—	10	Maximum time allowed for output drivers to release from being asserted or negated	A8.36
t_{ZAH}	20	—	20	—	20	—	Minimum delay time required for output drivers to assert or negate from released state	A8.37
t_{ZAD}	0	—	0	—	0	—		A8.38
t_{ENV}	20	70	20	70	20	70	Envelope time—from $\overline{\text{DMACK}}$ to STOP and $\overline{\text{HDMARDY}}$ during data out burst initiation.	A8.39
t_{SR}	—	50	—	30	—	20	STROBE to $\overline{\text{DMARDY}}$ time, if $\overline{\text{DMARDY}}$ is negated before this long after STROBE edge, the recipient receives no more than one additional data word.	A8.40
t_{RFS}	—	75	—	60	—	50	Ready-to-Final STROBE time—no STROBE edges are sent this long after negation of $\overline{\text{DMARDY}}$.	A8.41
t_{RP}	160	—	125	—	100	—	Ready-to-Pause time—the time recipient waits to initiate pause after negating $\overline{\text{DMARDY}}$.	A8.42
t_{IORDYZ}	—	20	—	20	—	20	Pull-up time before allowing IORDY to be released.	A8.43
t_{ZIORDY}	0	—	0	—	0	—	Minimum time drive waits before driving IORDY	A8.44
t_{ACK}	20	—	20	—	20	—	Setup and hold times for $\overline{\text{DMACK}}$, before assertion or negation.	A8.45
t_{SS}	50	—	50	—	50	—	Time from STROBE edge to negation of DMARQ or assertion of STOP, when sender terminates a burst.	A8.46

NOTES:

1 t_{UI}, t_{MLI}, t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks. That is, one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding.
- t_{UI} is an unlimited interlock that has no maximum time value.
- t_{MLI} is a limited time-out that has a defined minimum.
- t_{LI} is a limited time-out that has a defined maximum.

2 All timing parameters are measured at the connector of the drive to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after negation of DMARDY. STROBE and DMARDY timing measurements are taken at the connector of the sender. Even though the sender stops generating STROBE edges, the receiver may receive additional STROBE edges due to propagation delays. All timing measurement switching points (low to high and high to low) are taken at 1.5 V.

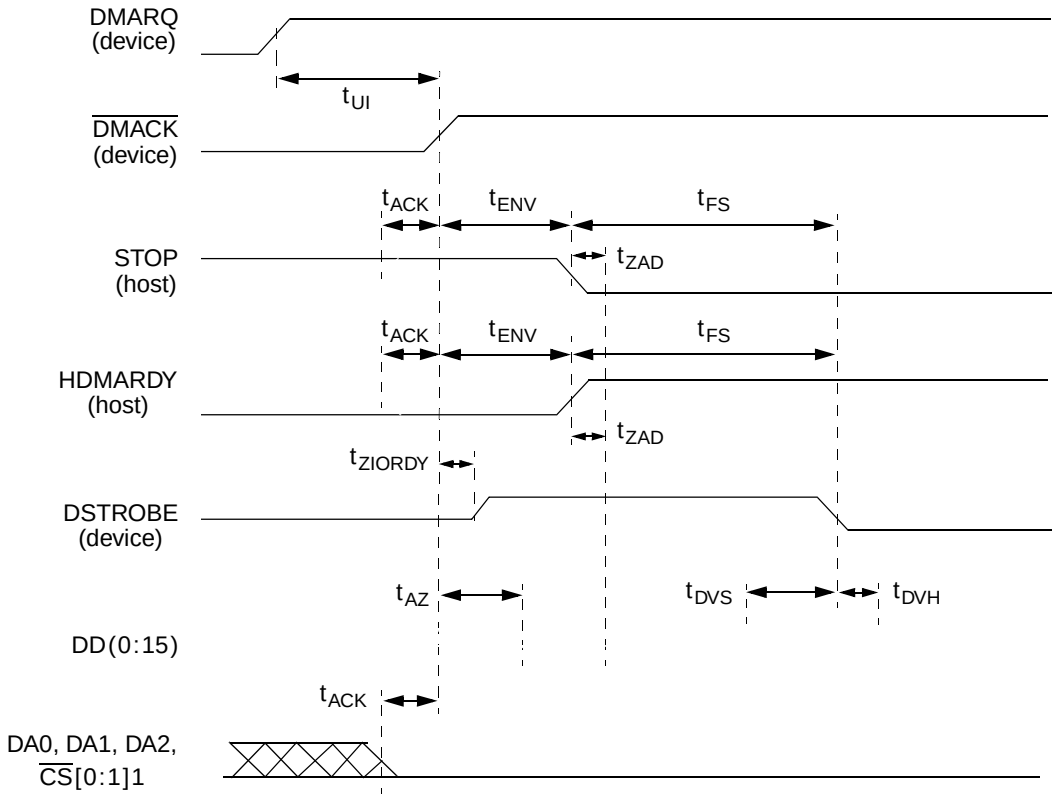


Figure 16. Timing Diagram—Initiating an Ultra DMA Data In Burst

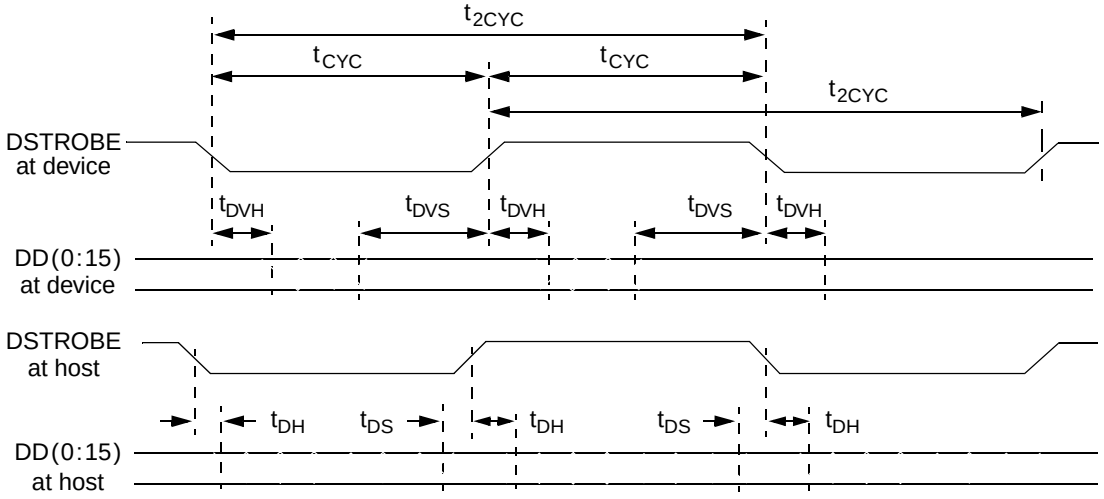


Figure 17. Timing Diagram—Sustained Ultra DMA Data In Burst

Table 32. MII Tx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns	A9.5
t_6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A9.6
t_7	TX_CLK pulse width high	35%	65%	TX_CLK Period(1)	A9.7
t_8	TX_CLK pulse width low	35%	65%	TX_CLK Period(1)	A9.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

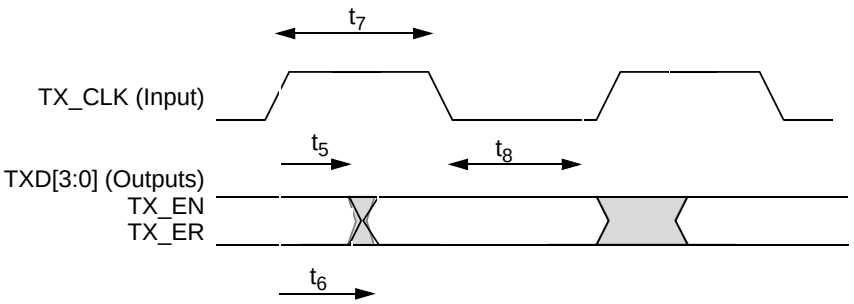


Figure 28. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A9.9

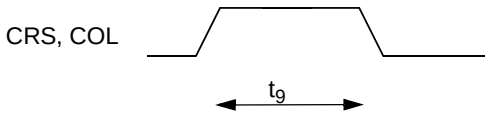


Figure 29. Ethernet Timing Diagram—MII Async

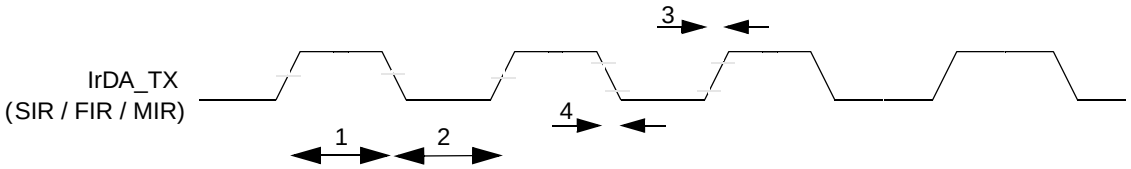


Figure 40. Timing Diagram — IrDA Transmit Line

1.3.16.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A15.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A15.29
5	Output Data valid after SCK	—	8.9	ns	A15.30
6	Input Data setup time	6.0	—	ns	A15.31
7	Input Data hold time	1.0	—	ns	A15.32
8	Slave disable lag time	—	8.9	ns	A15.33
9	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A15.34
10	Clock falling time	—	7.9	ns	A15.35
11	Clock rising time	—	7.9	ns	A15.36

NOTE

Output timing is specified at a nominal 50 pF load.

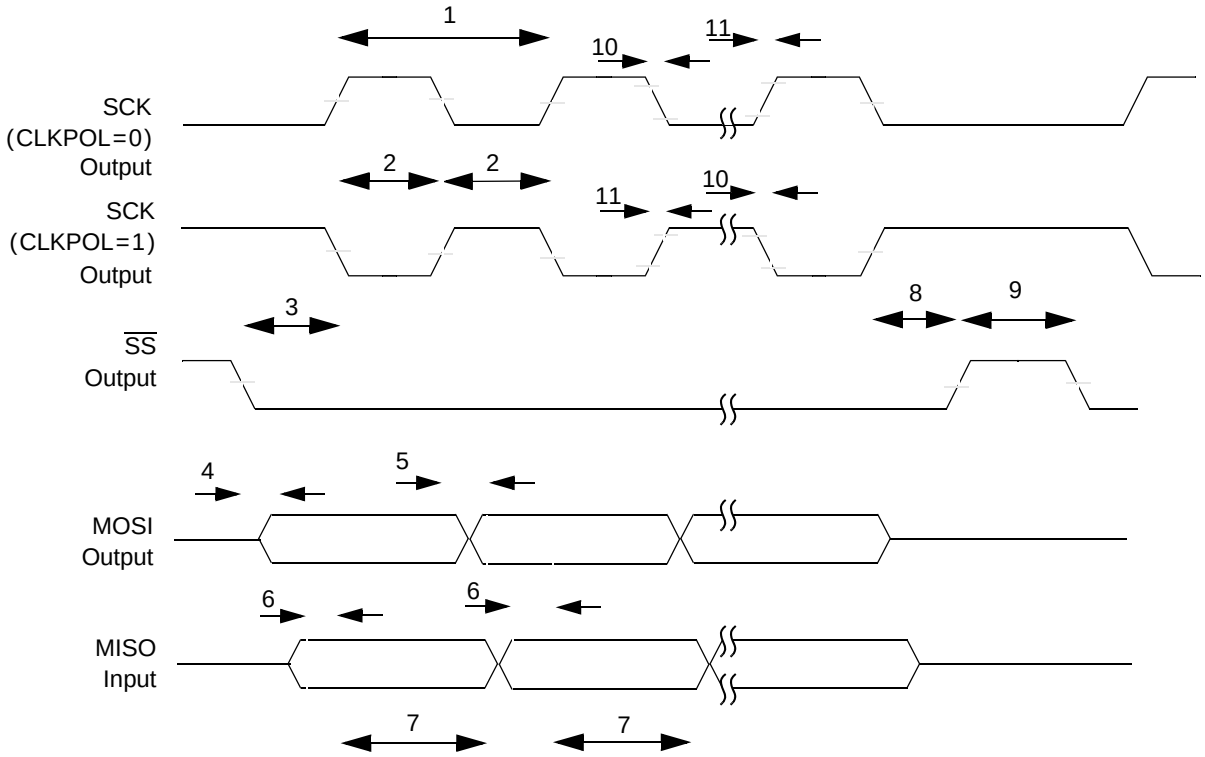


Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A15.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A15.38
3	Slave select clock delay	1.0	—	ns	A15.39
4	Input Data setup time	1.0	—	ns	A15.40
5	Input Data hold time	1.0	—	ns	A15.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A15.42
7	Output data valid after SCK	—	14.0	ns	A15.43
8	Slave disable lag time	0.0	—	ns	A15.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A15.45

NOTE

Output timing is specified at a nominal 50 pF load.

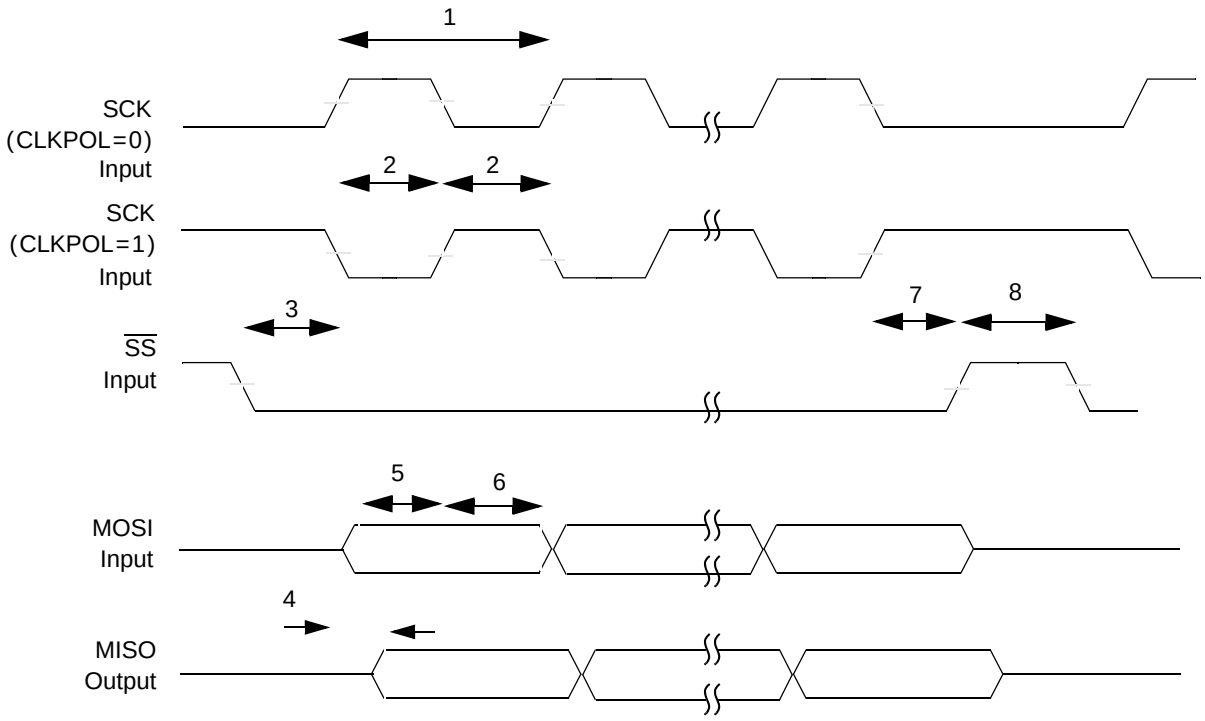


Figure 44. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

1.3.17 GPIOs and Timers

1.3.17.1 General and Asynchronous Signals

The MPC5200B contains several sets if I/Os that do not require special setup, hold, or valid requirements. Most of these are asynchronous to the system clock. The following numbers are provided for test and validation purposes only, and they assume a 133 MHz internal bus frequency.

Figure 45 shows the GPIO Timing Diagram. Table 50 gives the timing specifications.

Table 50. Asynchronous Signals

Sym	Description	Min	Max	Units	SpecID
t_{CK}	Clock Period	7.52	—	ns	A16.1
t_{IS}	Input Setup	12	—	ns	A16.2
t_{IH}	Input Hold	1	—	ns	A16.3
t_{DV}	Output Valid	—	15.33	ns	A16.4
t_{DH}	Output Hold	1	—	ns	A16.5

1.3.18 IEEE 1149.1 (JTAG) AC Specifications

Table 51. JTAG Timing Specification

Sym	Characteristic	Min	Max	Unit	SpecID
—	TCK frequency of operation.	0	25	MHz	A17.1
1	TCK cycle time.	40	—	ns	A17.2
2	TCK clock pulse width measured at 1.5V.	1.08	—	ns	A17.3
3	TCK rise and fall times.	0	3	ns	A17.4
4	$\overline{\text{TRST}}$ setup time to tck falling edge(1).	10	—	ns	A17.5
5	$\overline{\text{TRST}}$ assert time.	5	—	ns	A17.6
6	Input data setup time(2).	5	—	ns	A17.7
7	Input data hold time(2).	15	—	ns	A17.8
8	TCK to output data valid(3).	0	30	ns	A17.9
9	TCK to output high impedance(3).	0	30	ns	A17.10
10	TMS, TDI data setup time.	5	—	ns	A17.11
11	TMS, TDI data hold time.	1	—	ns	A17.12
12	TCK to TDO data valid.	0	15	ns	A17.13
13	TCK to TDO high impedance.	0	15	ns	A17.14

1 $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

2 Non-test, other than TDI and TMS, signal input timing with respect to TCK.

3 Non-test, other than TDO, signal output timing with respect to TCK.

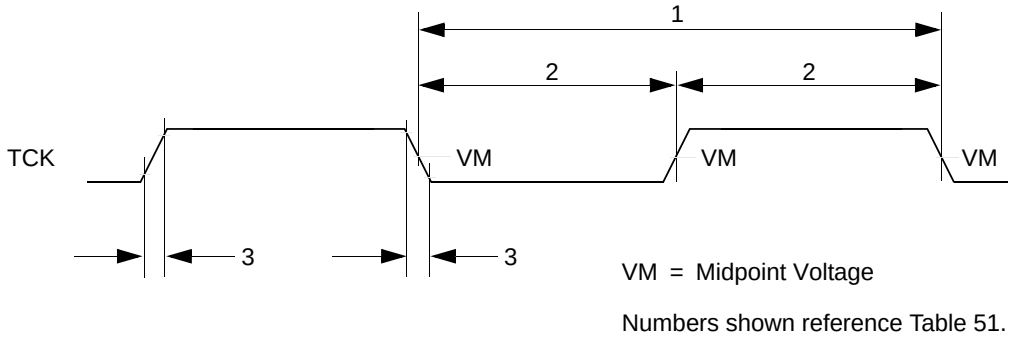


Figure 46. Timing Diagram—JTAG Clock Input

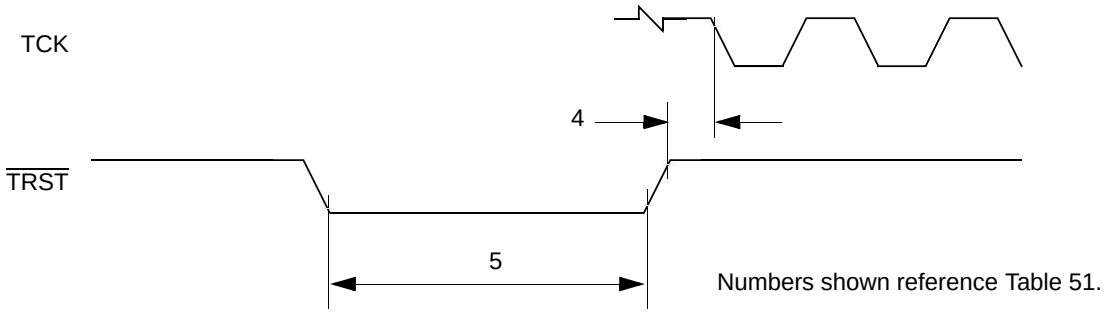


Figure 47. Timing Diagram—JTAG TRST

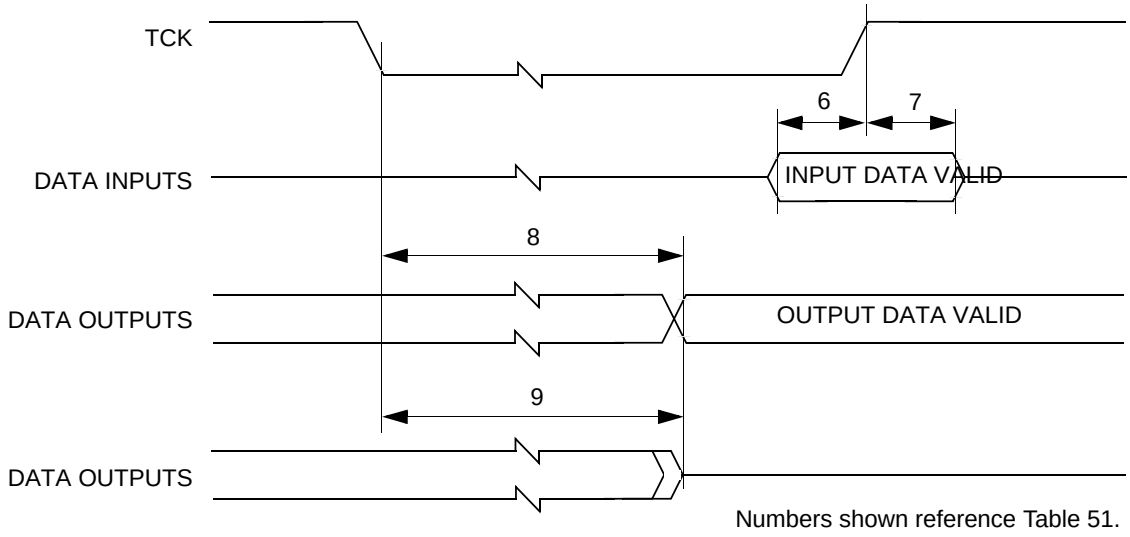


Figure 48. Timing Diagram—JTAG Boundary Scan

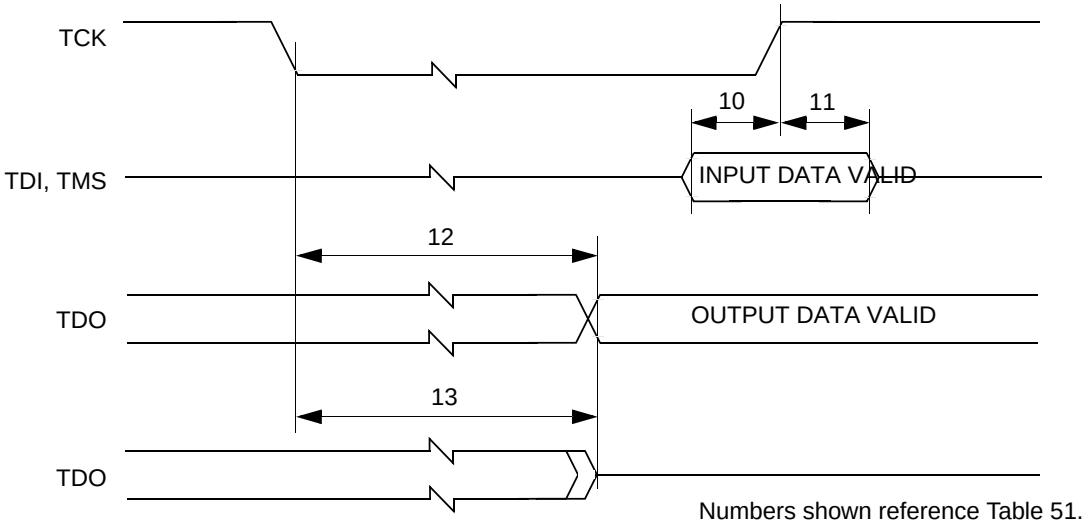


Figure 49. Timing Diagram—Test Access Port

2 Package Description

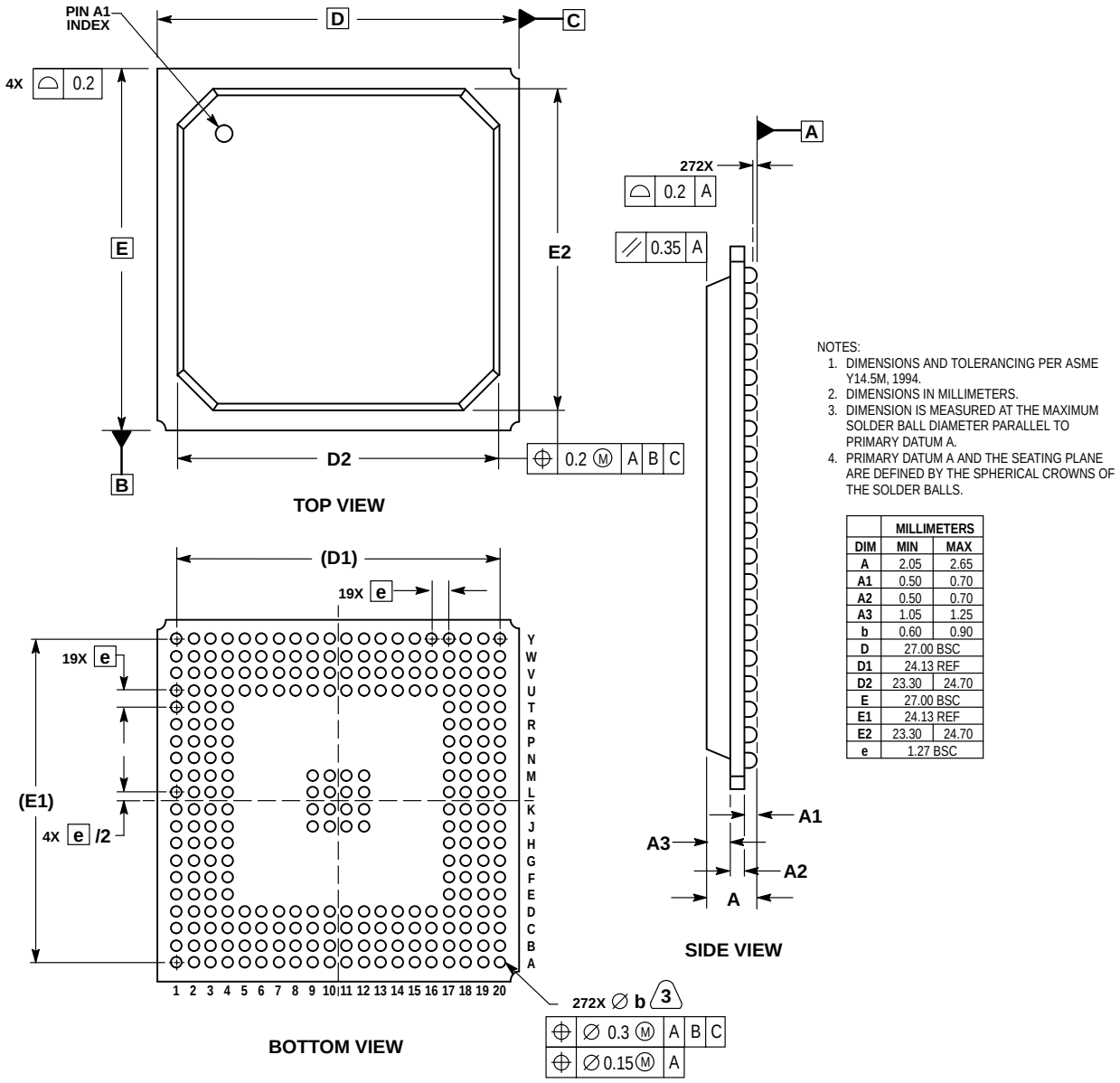
2.1 Package Parameters

The MPC5200B uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline: 27 mm x 27 mm
- Interconnects: 2
- Pitch: 1.27 mm

2.2 Mechanical Dimensions

Figure 50 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC5200B, 272 TE-PBGA package.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

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Figure 50. Mechanical Dimensions and Pinout Assignments for the MPC5200B, 272 TE-PBGA

Table 52. MPC5200B Pinout Listing (continued)

Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
ETH_8	RX_DV	I/O	VDD_IO	DRV4	TTL	
ETH_9	CD, RX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_10	CTS, COL	I/O	VDD_IO	DRV4	TTL	
ETH_11	TX_CLK	I/O	VDD_IO	DRV4	Schmitt	
ETH_12	RXD[0]	I/O	VDD_IO	DRV4	TTL	
ETH_13	USB_RXD, CTS, RXD[1]	I/O	VDD_IO	DRV4	TTL	
ETH_14	USB_RXP, UART_RX, RXD[2]	I/O	VDD_IO	DRV4	TTL	
ETH_15	USB_RXN, RX, RXD[3]	I/O	VDD_IO	DRV4	TTL	
ETH_16	USB_OVRCNT, CTS, RX_ER	I/O	VDD_IO	DRV4	TTL	
ETH_17	CD, CRS	I/O	VDD_IO	DRV4	TTL	
IRDA						
PSC6_0	IRDA_RX, RxD	I/O	VDD_IO	DRV4	TTL	
PSC6_1	Frame, CTS	I/O	VDD_IO	DRV4	TTL	
PSC6_2	IRDA_TX, TxD	I/O	VDD_IO	DRV4	TTL	
PSC6_3	IR_USB_CLK,BitClk, RTS	I/O	VDD_IO	DRV4	Schmitt	
USB						
USB_0	USB_OE	I/O	VDD_IO	DRV4	TTL	
USB_1	USB_TXN	I/O	VDD_IO	DRV4	TTL	
USB_2	USB_TXP	I/O	VDD_IO	DRV4	TTL	
USB_3	USB_RXD	I/O	VDD_IO	DRV4	TTL	
USB_4	USB_RXP	I/O	VDD_IO	DRV4	TTL	
USB_5	USB_RXN	I/O	VDD_IO	DRV4	TTL	
USB_6	USB_PRTPWR	I/O	VDD_IO	DRV4	TTL	
USB_7	USB_SPEED	I/O	VDD_IO	DRV4	TTL	
USB_8	USB_SUPEND	I/O	VDD_IO	DRV4	TTL	
USB_9	USB_OVRCNT	I/O	VDD_IO	DRV4	TTL	
I^2C						
I2C_0	SCL	I/O	VDD_IO	DRV4	Schmitt	
I2C_1	SDA	I/O	VDD_IO	DRV4	Schmitt	
I2C_2	SCL	I/O	VDD_IO	DRV4	Schmitt	

Table 52. MPC5200B Pinout Listing (continued)

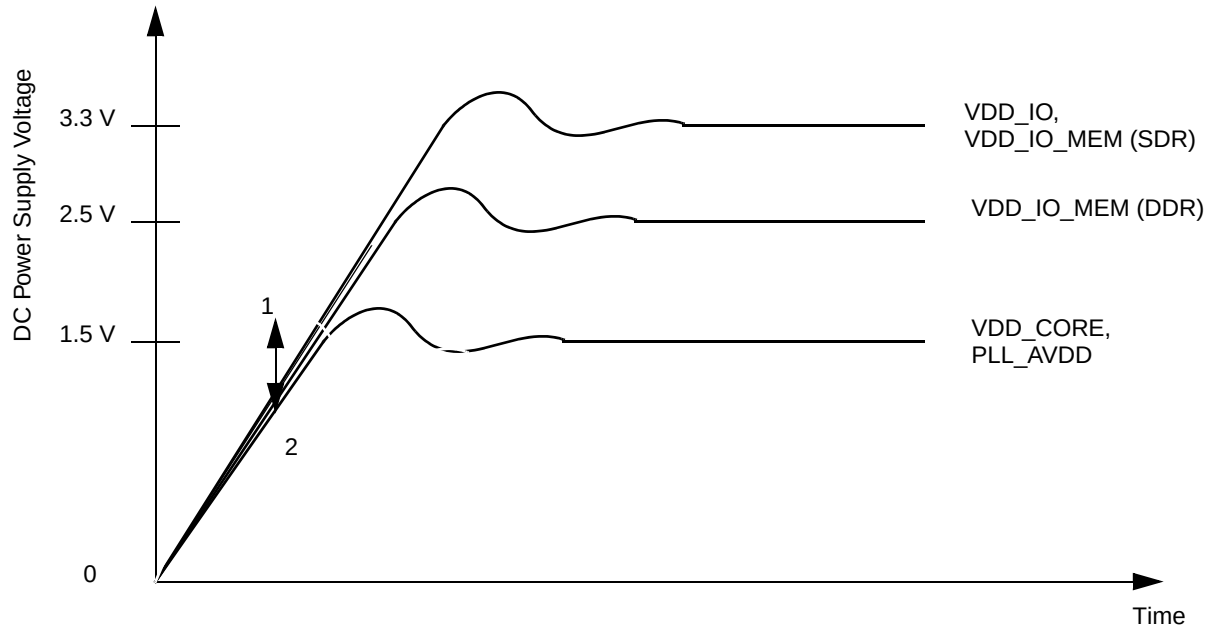
Name	Alias	Type	Power Supply	Output Driver Type	Input Type	Pull-up/ down
VDD_MEM_IO		—				
VDD_CORE		—				
VSS_IO/CORE		—				
SYS_PLL_AVDD		—				
CORE_PLL_AVDD		—				

1 All “open drain” outputs of the MPC5200B are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200B I/O power rail if the external signal is driven above the MPC5200B I/O power rail voltage.

3 System Design Information

3.1 Power Up/Down Sequencing

Figure 51 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).



Note: VDD_CORE should not exceed VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V at any time, including power-up.

Note: It is recommended that VDD_CORE/PLL_AVDD should track VDD_IO/VDD_IO_MEM up to 0.9 V then separate for completion of ramps.

Note: Input voltage must not be greater than the supply voltage (VDD_IO) VDD_IO_MEM, VDD_CORE, or PLL_AVDD) by more than 0.5 V at any time, including during power-up.

Note: Use 1 microsecond or slower rise time for all supplies.

Figure 51. Supply Voltage Sequencing

The relationship between VDD_IO_MEM and VDD_IO is non-critical during power-up and power-down sequences. VDD_IO_MEM (2.5 V or 3.3 V) and VDD_IO are specified relative to VDD_CORE.

3.1.1 Power Up Sequence

If VDD_IO/VDD_IO_MEM are powered up with the VDD_CORE at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the VDD_IO/VDD_IO_MEM to be in a high-impedance state. There is no limit to how long after VDD_IO/VDD_IO_MEM powers up before VDD_CORE must power up. VDD_CORE should not lead the VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

Use one microsecond or slower rise time for all supplies.

VDD_CORE/PLL_AVDD and VDD_IO/VDD_IO_MEM should track up to 0.9 V and then separate for the completion of ramps with VDD_IO/VDD_IO_MEM going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.1.2 Power Down Sequence

If VDD_CORE/PLL_AVDD are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after VDD_CORE and PLL_AVDD power down before VDD_IO or VDD_IO_MEM must power down. VDD_CORE should not lag VDD_IO, VDD_IO_MEM, or PLL_AVDD going low by more than 0.5 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop VDD_CORE/PLL_AVDD to 0 V.
2. Drop VDD_IO/VDD_IO_MEM supplies.

3.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing is a recommendation for the required filter circuit.

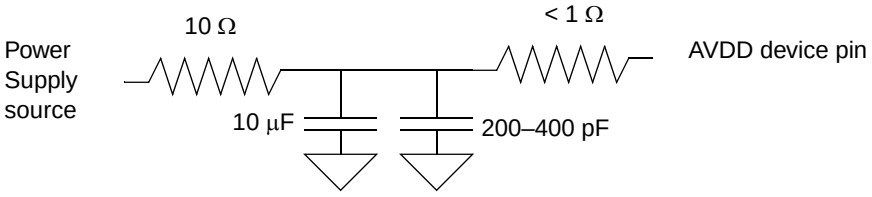


Figure 52. Power Supply Filtering

3.3 Pull-up/Pull-down Resistor Requirements

The MPC5200B requires external pull-up or pull-down resistors on certain pins.

3.3.1 Pull-down Resistor Requirements for TEST pins

The MPC5200B requires pull-down resistors on the test pins TEST_MODE_0, TEST_MODE_1, TEST_SEL_1.

To reset the MPC5200B via the COP connector, the HRESET pin of the COP should be connected to the HRESET pin of the MPC5200B. The circuitry shown in Figure 54 allows the COP to assert HRESET or JTAG_TRST separately, while any other board sources can drive PORRESET.

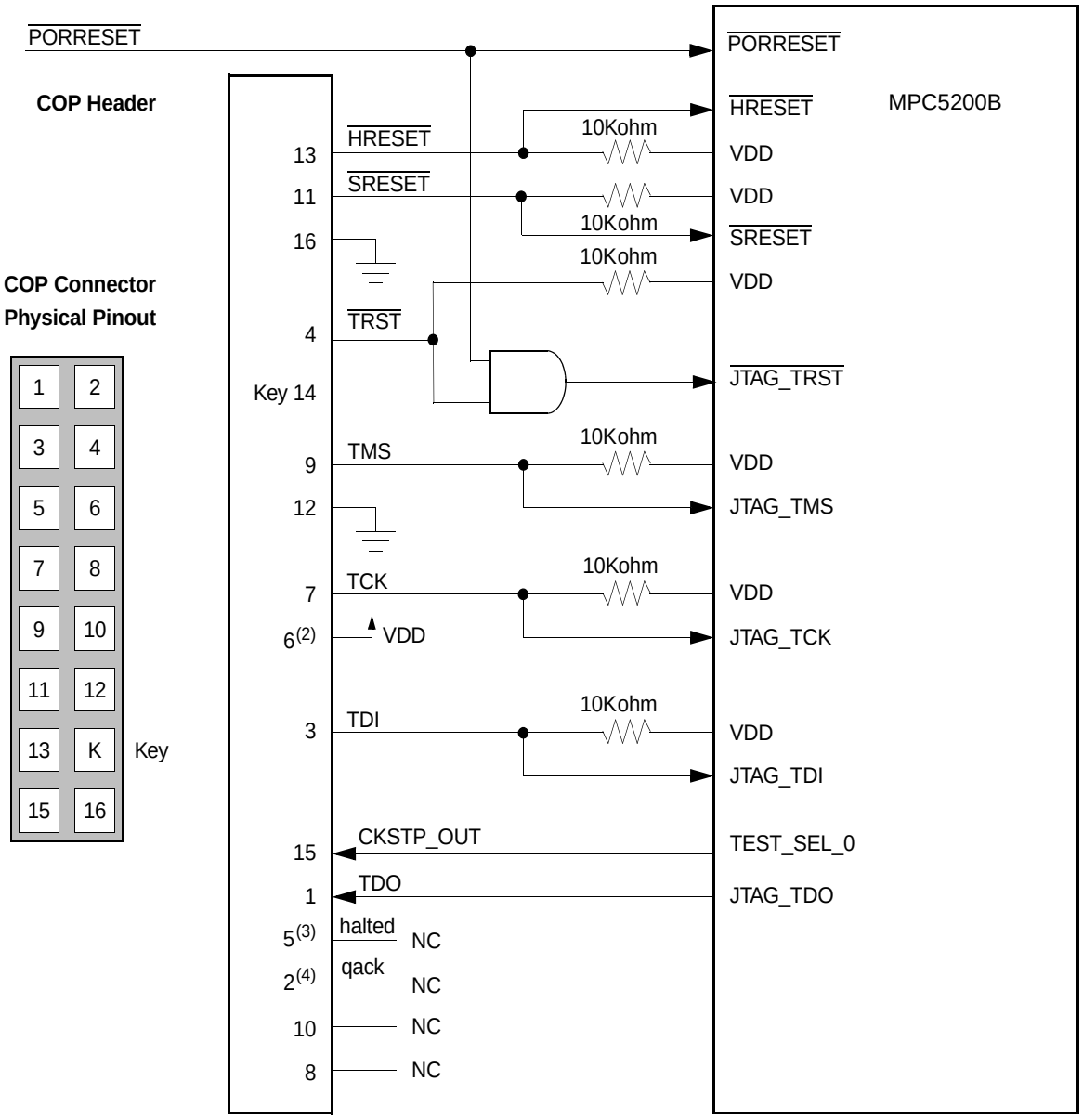


Figure 54. COP Connector Diagram

3.4.2.2 Boards Without COP Connector

If the JTAG interface is not used, JTAG_TRST should be tied to PORRESET, so that it is asserted when the system reset signal (PORRESET) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 55 shows the connection of the JTAG interface without COP connector.