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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l052r8t6

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.13 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.14 Communication interfaces

3.14.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 *can be served by the DMA1 Controller.*

3.14.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.14.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 *can be served by the DMA1 Controller.*

Table 3. Legend/abbreviation for *Table 4*

Type	I= input, O = output, S = power supply	
Level	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. High density value line STM8L05xxx pin description

Pin number	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	NRST/PA1(1)	I/O	-	-	X	-	HS	X	X	**Reset**	PA1
3	PA2/OSC_IN/ *[USART1_TX]*(8)/ *[SPI1_MISO]*(8)	I/O	-	X	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out]*
4	PA3/OSC_OUT/*[USART1_ RX]*(8)/*[SPI1_MOSI]*(8)	I/O	-	X	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
5	PA4/TIM2_BKIN/ *[TIM2_ETR]*(8)/ LCD_COM0/ADC1_IN2	I/O	FT(2)	X	X	X	HS	X	X	**Port A4**	Timer 2 - break input */[Timer 2 - trigger]/* LCD COM 0 / ADC1 input 2
6	PA5/TIM3_BKIN/ *[TIM3_ETR]*(8)/ LCD_COM1/ADC1_IN1	I/O	FT(2)	X	X	X	HS	X	X	**Port A5**	Timer 3 - break input */[Timer 3 - trigger]/* LCD_COM 1 / ADC1 input 1
7	PA6/*[ADC1_TRIG]*/ LCD_COM2/ADC1_IN0	I/O	FT(2)	X	X	X	HS	X	X	**Port A6**	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0
8	PA7/LCD_SEG0(2) /TIM5_CH1	I/O	FT(2)	X	X	X	HS	X	X	**Port A7**	LCD segment 0/ TIM5 channel 1
31	PB0(3)/TIM2_CH1/ LCD_SEG10/ADC1_IN18	I/O	FT(2)	X	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C0	CLK	CLK_CKDIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0xX0
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x
0x00 50D0		CLK_PCKENR3	Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OARH	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0x
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	0xXX
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5311	TIM5	TIM5_CCR1H	TIM5 Capture/Compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 Capture/Compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 Capture/Compare register 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 Capture/Compare register 2 low	0x00
0x00 5315		TIM5_BKR	TIM5 break register	0x00
0x00 5316		TIM5_OISR	TIM5 output idle state register	0x00
0x00 5317 to 0x00 533F	Reserved area			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00
0x00 5352 to 0x00 53BF	Reserved area (110 bytes)			

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
21	TIM3/USART3	TIM3 update/overflow/ trigger/break USART3 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(5)	0x00 805C
22	TIM3/USART3	TIM3 capture/compareUSART3 Receive register data full/overrun/idle line detected/parity error/ interrupt	-	-	Yes	Yes(5)	0x00 8060
23	TIM1	Update /overflow/trigger/ COM	-	-	-	Yes(5)	0x00 8064
24	TIM1	Capture/compare	-	-	-	Yes(5)	0x00 8068
25	TIM4	TIM4 update/overflow/ trigger	-	-	Yes	Yes(5)	0x00 806C
26	SPI1	End of Transfer	Yes	Yes	Yes	Yes(5)	0x00 8070
27	USART1/TIM5	USART1 transmission complete/transmit data register empty/ TIM5 update/overflow/ trigger/break	-	-	Yes	Yes(5)	0x00 8074
28	USART1/TIM5	USART1 received data ready/overrun error/ idle line detected/parity error/TIM5 capture/compare	-	-	Yes	Yes(5)	0x00 8078
29	I^2C1/SPI2	I^2C1 interrupt(4)/SPI2	Yes	Yes	Yes	Yes(5)	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
4. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.
5. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8Lxx Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

Table 10. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
00 4807	PCODESIZE	OPT2	PCODE[7:0]								0x00
00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
00 480C											0x00

Table 11. Option byte description

Option byte no.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area UBC[7:0] Size of the user boot code area 0x00: No UBC 0x01: Page 0 reserved for the UBC and write protected. ... 0xFF: Page 0 to 254 reserved for the UBC and write-protected. Refer to User boot code section in the STM8L reference manual (RM0031).
OPT2	**PCODESIZE[7:0]** Size of the proprietary code area 0x00: No proprietary code area 0x01: Page 0 reserved for the proprietary code and read/write protected. ... 0xFF: Page 0 to 254 reserved for the proprietary code and read/write protected. Refer to Proprietary code area (PCODE) section in the STM8L reference manual (RM0031) for more details.
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent watchdog off in Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles

In the following table, data are based on characterization results, unless otherwise specified.

Table 19. Total current consumption and timing in Low power run mode at V_{DD} = 1.8 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.86	6.38	µA
				T_A = 55 °C	6.52	7.06	
				T_A = 85 °C	7.68	8.7	
			with TIM2 active[2]	T_A = -40 °C to 25 °C	6.2	6.73	
				T_A = 55 °C	6.86	7.41	
				T_A = 85 °C	9.71	10.81	
		LSE [3] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.42	5.94	
				T_A = 55 °C	5.9	6.52	
				T_A = 85 °C	6.14	6.8	
			with TIM2 active [2]	T_A = -40 °C to 25 °C	5.87	6.48	
				T_A = 55 °C	6.44	6.95	
				T_A = 85 °C	6.7	7.65	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*

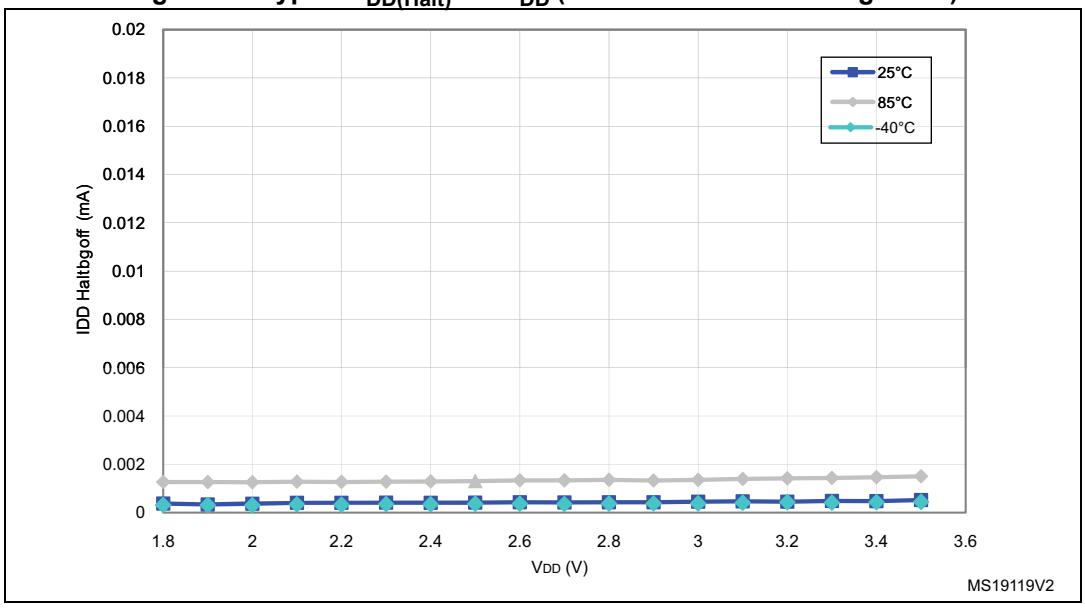
In the following table, data are based on characterization results, unless otherwise specified.

Table 23. Total current consumption and timing in Halt mode at V_{DD} = 1.8 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra low power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	1600(2)	nA
		T_A = 55 °C	810	2400	
		T_A = 85 °C	1600	4500(2)	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7	µs
$t_{WU\_LSI(Halt)}$(3)(4)	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	µs

1. T_A = -40 to 85 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Figure 15. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)



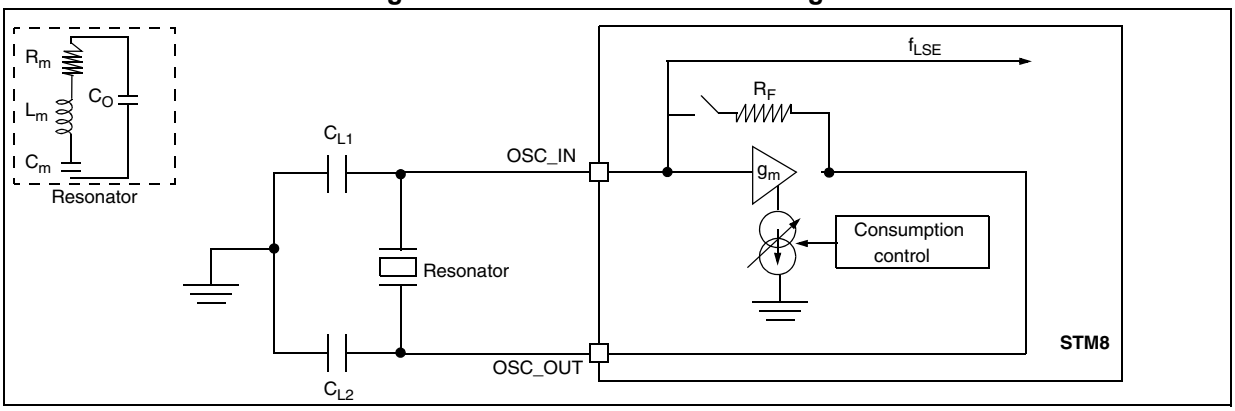
Current consumption of on-chip peripherals

Table 24. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(ALL)}$	Peripherals ON (1)		63	
$I_{DD(TIM1)}$	TIM1 supply current(2)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (2)		7	
$I_{DD(TIM3)}$	TIM3 supply current (2)		7	
$I_{DD(TIM5)}$	TIM5 supply current (2)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (2)		3	
$I_{DD(USART1)}$	USART1 supply current (3)		5	
$I_{DD(USART2)}$	USART2 supply current (3)		5	
$I_{DD(USART3)}$	USART3 supply current (3)		5	
$I_{DD(SPI1)}$	SPI1 supply current (3)		3	
$I_{DD(SPI2)}$	SPI2 supply current (3)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (3)		4	
$I_{DD(DMA1)}$	DMA1 supply current		3	
$I_{DD(WWDG)}$	WWDG supply current		1	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (5)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (5)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
2. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Including supply current of internal reference voltage.

Figure 17. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

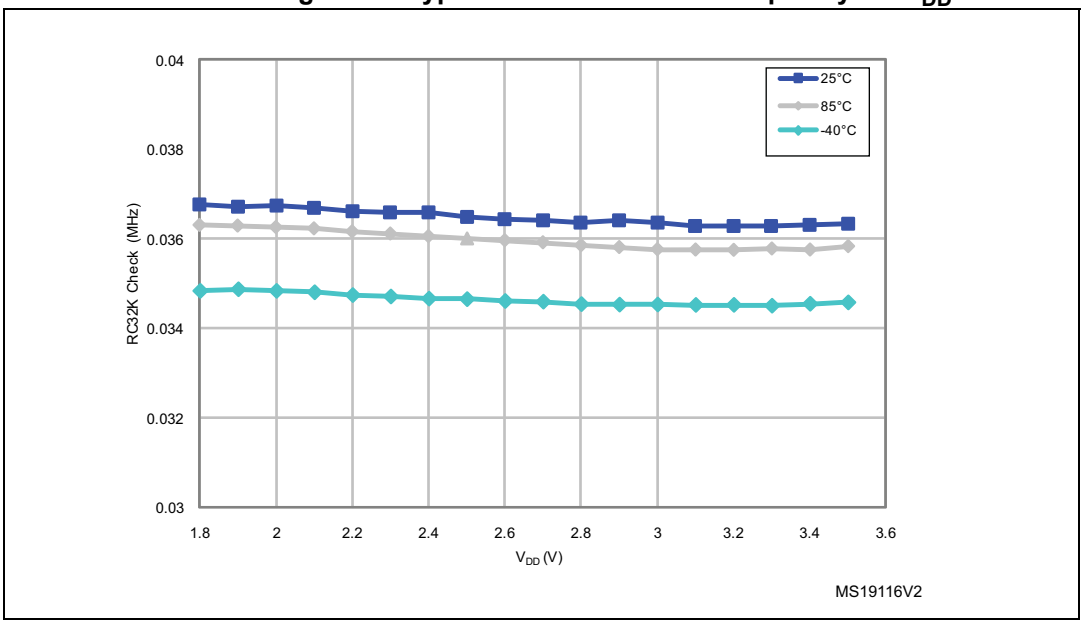
In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)	-	1 (2)	%
		1.8 V ≤V_{DD} ≤ 3.6 V, -40 °C ≤T_A ≤ 85 °C	-5	-	5	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16	-	0.4	0.7	%
		Trimming code = multiple of 16	-		± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6 (4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
4. Guaranteed by design.

Figure 19. Typical LSI clock source frequency vs. V_{DD}



8.3.5 Memory characteristics

T_A = -40 to 85 °C unless otherwise specified.

Table 32. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.8	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

Table 36. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Standard	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 37. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 38. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

8.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 43. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-	-	10	µs
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤85 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation

In the following three tables, data are guaranteed by characterization result, not tested in production.

Table 45. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ.	Max.	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 46. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ.	Max.	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 47. ADC1 accuracy with V_{DDA} = V_{REF+} = 1.8 V to 2.4 V

Symbol	Parameter	Typ.	Max.	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Figure 39. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

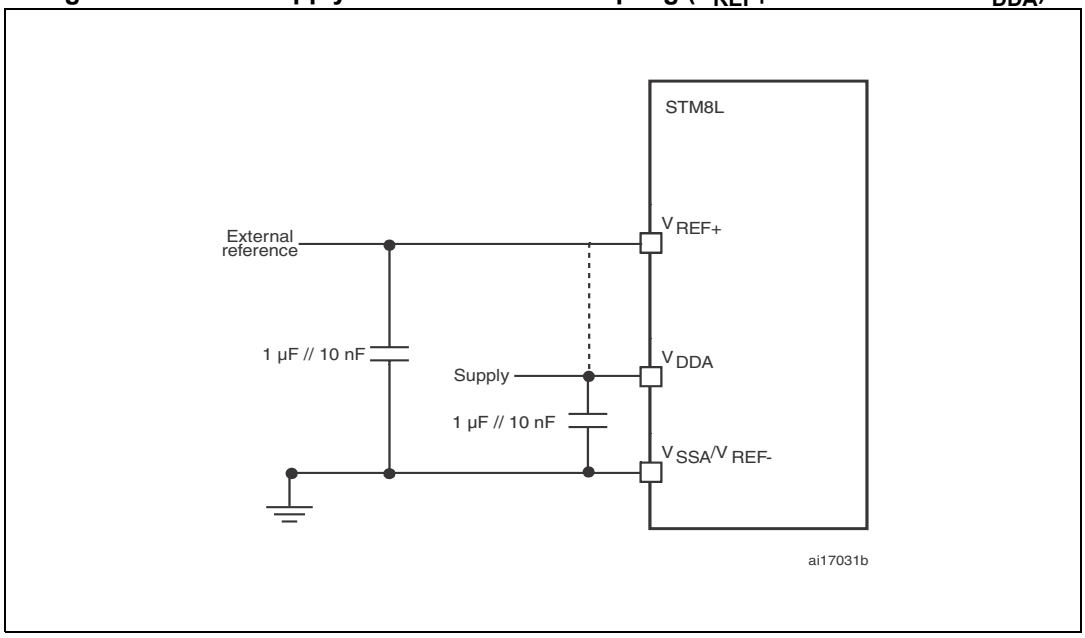
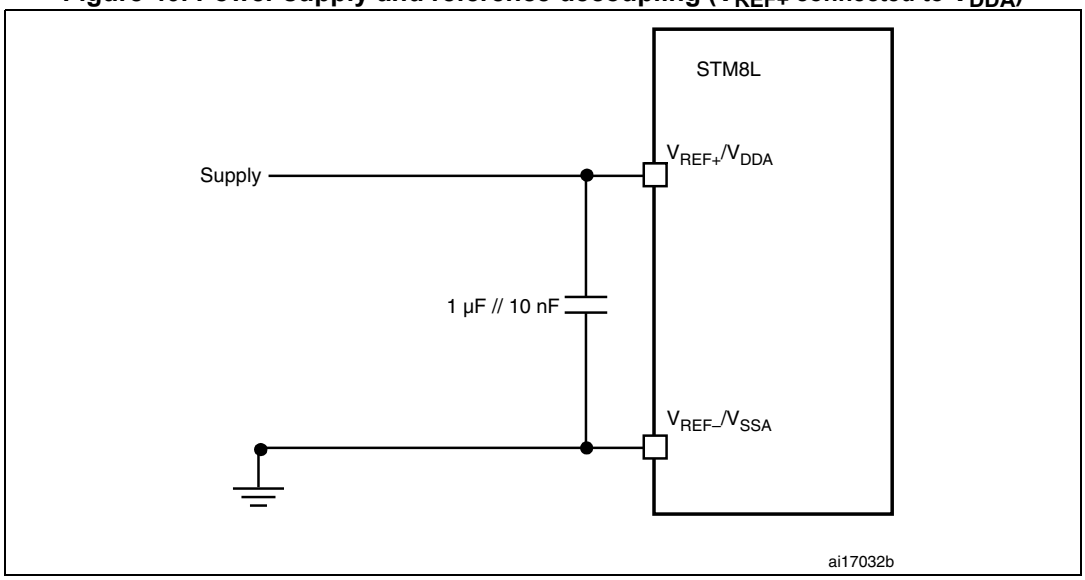


Figure 40. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

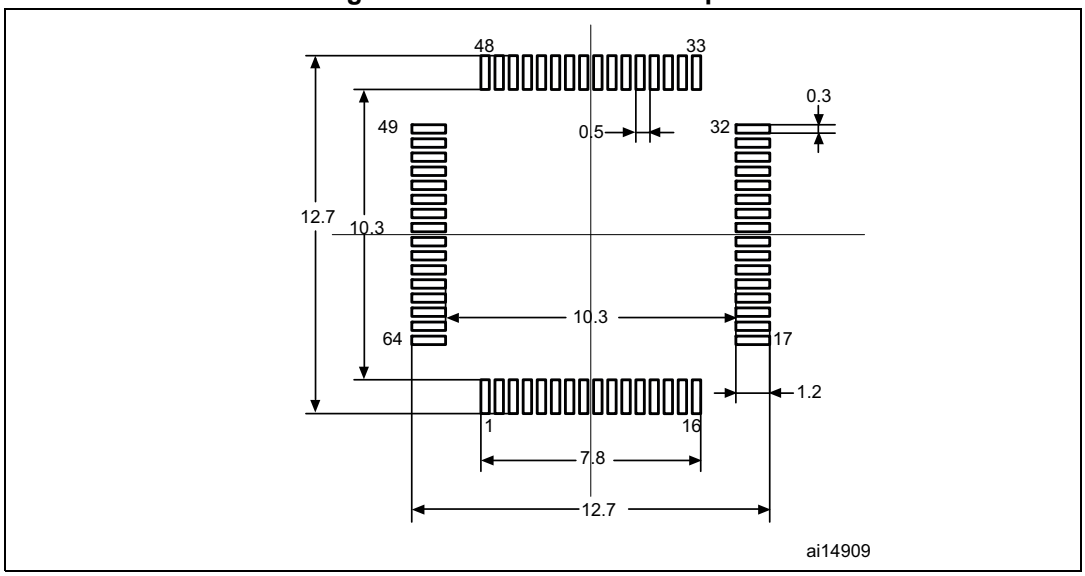


9 Package characteristics

9.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 42. Recommended footprint



1. Dimensions are in millimeters.