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Details

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc878-13ffi-5v-aa

XC87x Data Sheet**Revision History: V1.5 2011-03**

Previous Versions: V1.4

Page	Subjects (major changes since last revision)
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Changes from V1.4 2010-08 to V1.5 2011-03

Page 3	A new variant, SAF-XC874CM-13FVA 5V, has been added in Table 2.
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General Device Information

2.3 Pin Configuration

The pin configuration of the XC878, which is based on the PG-LQFP-64, is shown in **Figure 4**, while that of the XC874, which is based on the PG-VQFN-48 package, is shown in **Figure 5**.

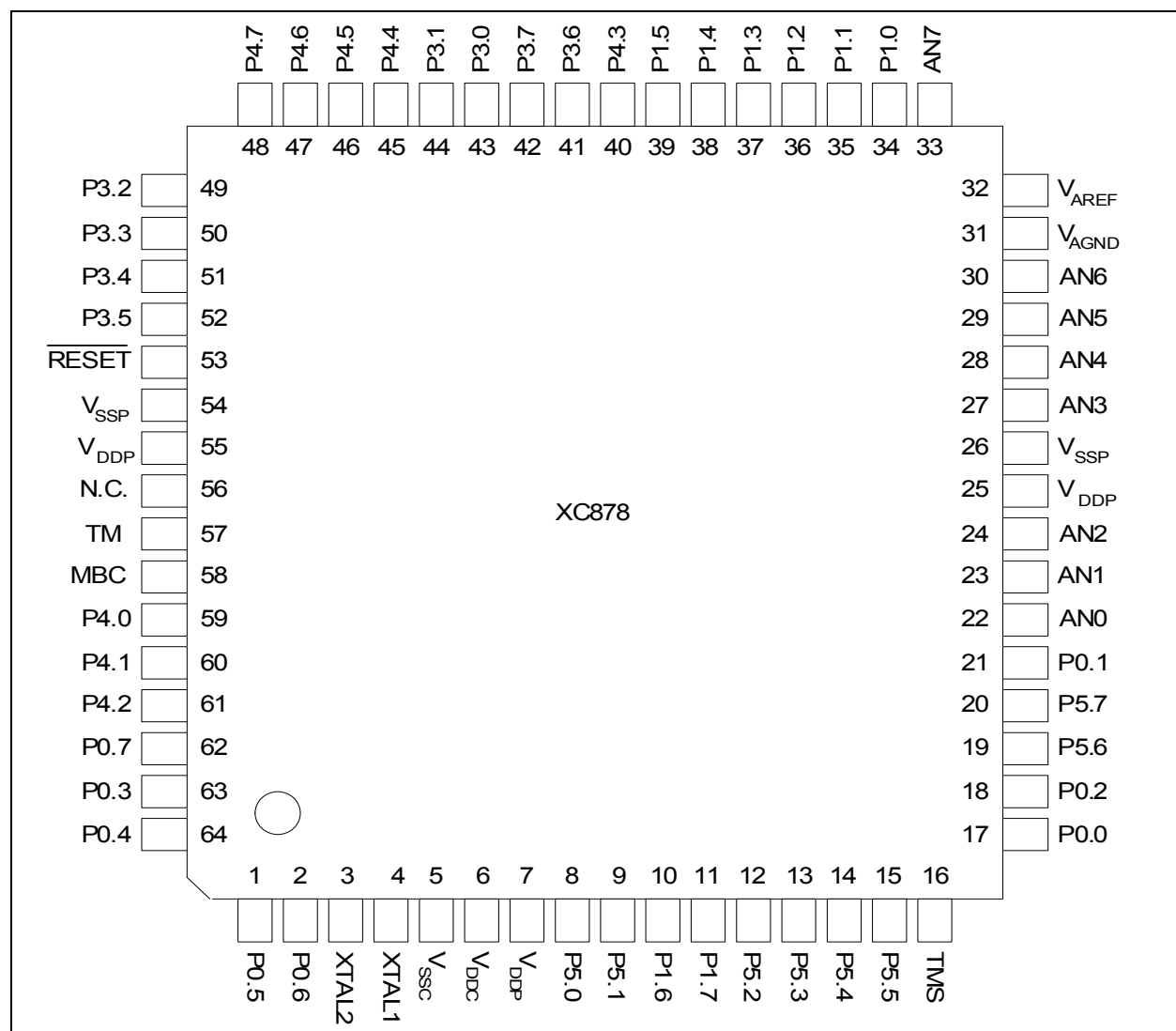


Figure 4 XC878 Pin Configuration, PG-LQFP-64 Package (top view)

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P3		I/O		Port 3 Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, T2CCU, Timer 21, MultiCAN and External Bus Interface. <i>Note: External Bus Interface is not available in XC874.</i>
P3.0	43/33		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output T2CC0_1/ External Interrupt Input 3/T2CCU EXINT3_2 Capture/Compare Channel 0
P3.1	44/34		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	49/35		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1 T2CC1_1/ External Interrupt Input 4/T2CCU EXINT4_2 Capture/Compare Channel 1
P3.3	50/36		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output T2CC2_1/ External Interrupt Input 5/T2CCU EXINT5_2 Capture/Compare Channel 2 A13 Address Line 13 Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P3.4	51/37		Hi-Z	CC62_0 RXDC0_1 T2EX1_0 T2CC3_1/ EXINT6_3 A14	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input External Interrupt Input 6/T2CCU Capture/Compare Channel 3 Address Line 14 Output
P3.5	52/38		Hi-Z	COUT62_0 EXF21_0 TXDC0_1 A15	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output Address Line 15 Output
P3.6	41/32		PU	CTR $\overline{\text{AP}}$ _0	CCU6 Trap Input
P3.7	42/-		Hi-Z	EXINT4_0 COUT63_0 A16	External Interrupt Input 4 Output of Capture/Compare channel 3 Address Line 16 Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P4.5	46/-		Hi-Z	CCPOS1_3 CCU6 Hall Input 1 T1_0 Timer 1 Input COUT61_2 Output of Capture/Compare channel 1 T2CC3_0/ External Interrupt Input 6/T2CCU EXINT6_2 Capture/Compare Channel 3 D5 Data Line 5 Input/Output
P4.6	47/-		Hi-Z	CCPOS2_3 CCU6 Hall Input 2 T2_0 Timer 2 Input CC62_2 Output of Capture/Compare channel 2 T2CC4_0 Compare Output Channel 4 D6 Data Line 6 Input/Output
P4.7	48/-		Hi-Z	CTRAP_3 CCU6 Trap Input COUT62_2 Output of Capture/Compare channel 2 T2CC5_0 Compare Output Channel 5 D7 Data Line 7 Input/Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P5		I/O		Port 5 Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External Interface.
P5.0	8/-		PU	EXINT1_1 External Interrupt Input 1 A0 Address Line 0 Output
P5.1	9/-		PU	EXINT2_1 External Interrupt Input 2 A1 Address Line 1 Output
P5.2	12/-		PU	RXD_2 UART Receive Data Input T2CC2_2/ External Interrupt Input 5/T2CCU EXINT5_3 Capture/Compare Channel 2 A2 Address Line 2 Output
P5.3	13/-		PU	CCPOS0_0 CCU6 Hall Input 0 EXINT1_0 External Interrupt Input 1 T12HR_2 CCU6 Timer 12 Hardware Run Input CC61_3 Input of Capture/Compare channel 1 TXD_2 UART Transmit Data Output/Clock Output T2CC5_2 Compare Output Channel 5 A3 Address Line 3 Output
P5.4	14/-		PU	CCPOS1_0 CCU6 Hall Input 1 EXINT2_0 External Interrupt Input 2 T13HR_2 CCU6 Timer 13 Hardware Run Input CC62_3 Input of Capture/Compare channel 2 RXDO_2 UART Transmit Data Output T2CC4_2 Compare Output Channel 4 A4 Address Line 4 Output

Functional Description

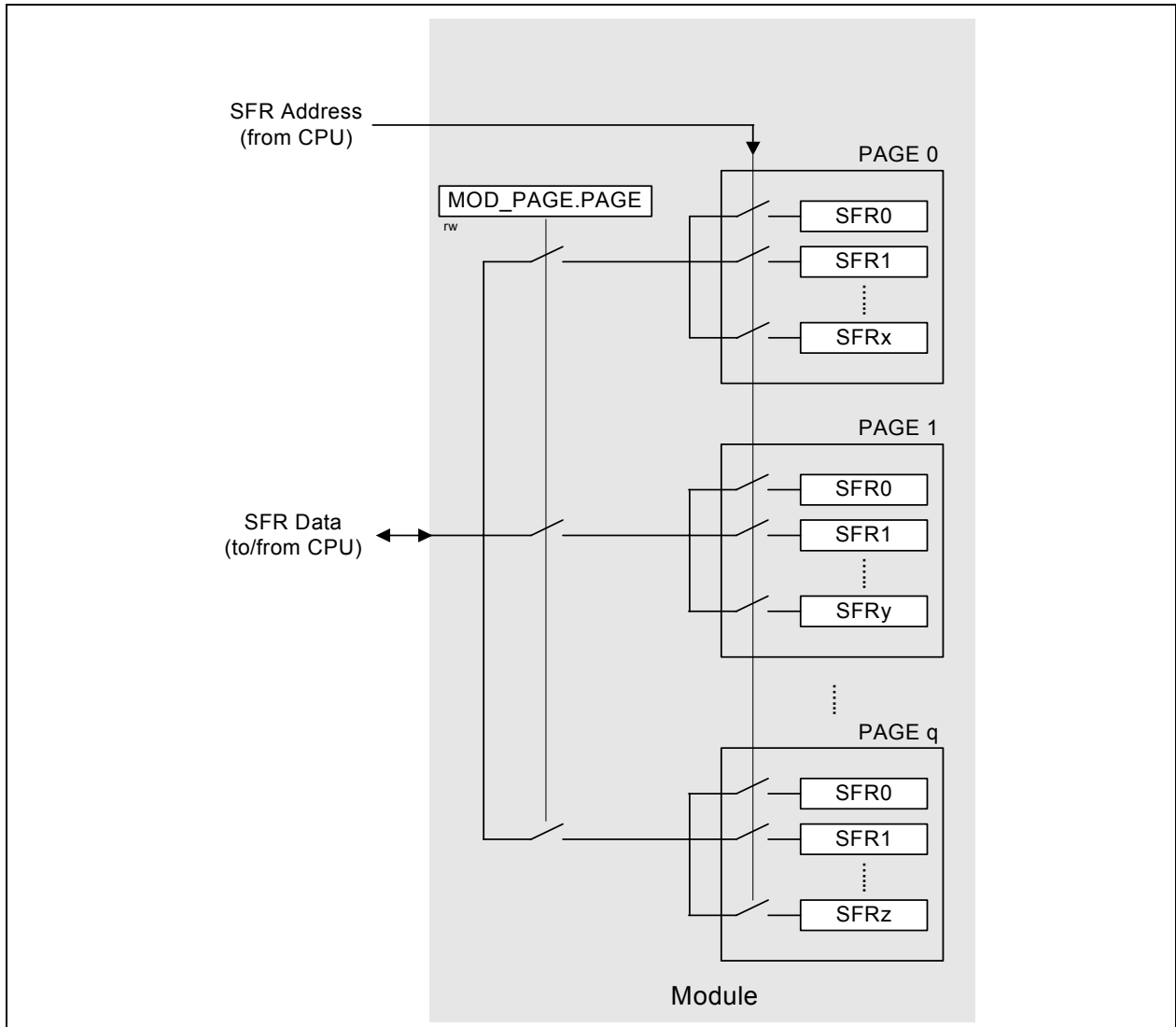


Figure 10 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or

Functional Description
Table 8 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B7 _H	EXICON0 Reset: F0_H External Interrupt Control Register 0	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0	
		Type	rw		rw		rw		rw	
BA _H	EXICON1 Reset: 3F_H External Interrupt Control Register 1	Bit Field	0		EXINT6		EXINT5		EXINT4	
		Type	r		rw		rw		rw	
BB _H	NMICON Reset: 00_H NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	0	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Type	r	rw	rw	r	rw	rw	rw	rw
BC _H	NMISR Reset: 00_H NMI Status Register	Bit Field	0	FNMI ECC	FNMI VDDP	0	FNMI OCDS	FNMI FLASH	FNMI PLL	FNMI WDT
		Type	r	rwh	rwh	r	rwh	rwh	rwh	rwh
BD _H	BCON Reset: 20_H Baud Rate Control Register	Bit Field	BGSEL		NDOV EN	BRDIS	BRPRE			R
		Type	rw		rw	rw	rw			rw
BE _H	BG Reset: 00_H Baud Rate Timer/Reload Register	Bit Field	BR_VALUE							
		Type	rwh							
E9 _H	FDCON Reset: 00_H Fractional Divider Control Register	Bit Field	BGS	SYNE N	ERRS YN	EOFS YN	BRK	NDOV	FDM	FDEN
		Type	rw	rw	rwh	rwh	rwh	rwh	rw	rw
EA _H	FDSTEP Reset: 00_H Fractional Divider Reload Register	Bit Field	STEP							
		Type	rw							
EB _H	FDRES Reset: 00_H Fractional Divider Result Register	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 1										
B3 _H	ID Reset: 49_H Identity Register	Bit Field	PRODID					VERID		
		Type	r					r		
B4 _H	PMCON0 Reset: 80_H Power Mode Control Register 0	Bit Field	VDDP WARN	WDT RST	WKRS	WK SEL	SD	PD	WS	
		Type	rh	rwh	rwh	rw	rw	rwh	rw	
B5 _H	PMCON1 Reset: 00_H Power Mode Control Register 1	Bit Field	0	CDC_ DIS	CAN_ DIS	MDU_ DIS	T2CC U_DIS	CCU_ DIS	SSC_ DIS	ADC_ DIS
		Type	r	rw	rw	rw	rw	rw	rw	rw
B6 _H	OSC_CON Reset: XX_H OSC Control Register	Bit Field	PLLRD RES	PLLBY P	PLLPD	0	XPD	OSC SS	EORD RES	EXTO SCR
		Type	rwh	rwh	rw	r	rw	rwh	rwh	rh
B7 _H	PLL_CON Reset: 18_H PLL Control Register	Bit Field	NDIV						PLLR	PLL_L OCK
		Type	rw						rh	rh
BA _H	CMCON Reset: 10_H Clock Control Register	Bit Field	KDIV		0	FCCF G	CLKREL			
		Type	rw		r	rw	rw			

Functional Description
Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CB _H	ADC_RCR1 Reset: 00_H Result Control Register 1	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CC _H	ADC_RCR2 Reset: 00_H Result Control Register 2	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CD _H	ADC_RCR3 Reset: 00_H Result Control Register 3	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CE _H	ADC_VFCR Reset: 00_H Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA _H	ADC_CHINFR Reset: 00_H Channel Interrupt Flag Register	Bit Field	CHINF 7	CHINF 6	CHINF 5	CHINF 4	CHINF 3	CHINF 2	CHINF 1	CHINF 0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB _H	ADC_CHINCR Reset: 00_H Channel Interrupt Clear Register	Bit Field	CHINC 7	CHINC 6	CHINC 5	CHINC 4	CHINC 3	CHINC 2	CHINC 1	CHINC 0
		Type	w	w	w	w	w	w	w	w
CC _H	ADC_CHINSR Reset: 00_H Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w
CD _H	ADC_CHINPR Reset: 00_H Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE _H	ADC_EVINFR Reset: 00_H Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF _H	ADC_EVINCR Reset: 00_H Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
D2 _H	ADC_EVINSR Reset: 00_H Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
D3 _H	ADC_EVINPR Reset: 00_H Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA _H	ADC_CRCR1 Reset: 00_H Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB _H	ADC_CRPR1 Reset: 00_H Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			

Functional Description
Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
C5 _H	T2CCU_CCTH Reset: 00 _H T2CCU Capture/Compare Timer Register High	Bit Field	CCT							
		Type	rwh							
C6 _H	T2CCU_CCTCON Reset: 00 _H T2CCU CaptureCcompare Timer Control Register	Bit Field	CCTPRE				CCTO VF	CCTO VEN	TIMSY N	CCTS T
		Type	rw				rwh	rw	rw	rw
RMAP = 0, PAGE 2										
C0 _H	T2CCU_COSHDW Reset: 00 _H T2CCU Capture/compare Enable Register	Bit Field	ENSH DW	TXOV	COOU T5	COOU T4	COOU T3	COOU T2	COOU T1	COOU T0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
C1 _H	T2CCU_CC0L Reset: 00 _H T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL							
		Type	rwh							
C2 _H	T2CCU_CC0H Reset: 00 _H T2CCU Capture/compare Register 0 High	Bit Field	CCVALH							
		Type	rwh							
C3 _H	T2CCU_CC1L Reset: 00 _H T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL							
		Type	rwh							
C4 _H	T2CCU_CC1H Reset: 00 _H T2CCU Capture/compare Register 1 High	Bit Field	CCVALH							
		Type	rwh							
C5 _H	T2CCU_CC2L Reset: 00 _H T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL							
		Type	rwh							
C6 _H	T2CCU_CC2H Reset: 00 _H T2CCU Capture/compare Register 2 High	Bit Field	CCVALH							
		Type	rwh							
RMAP = 0, PAGE 3										
C0 _H	T2CCU_COCON Reset: 00 _H T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD	
		Type	rw	rw	rwh	rwh	rw	rw	rw	
C1 _H	T2CCU_CC3L Reset: 00 _H T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL							
		Type	rwh							
C2 _H	T2CCU_CC3H Reset: 00 _H T2CCU Capture/compare Register 3 High	Bit Field	CCVALH							
		Type	rwh							
C3 _H	T2CCU_CC4L Reset: 00 _H T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL							
		Type	rwh							
C4 _H	T2CCU_CC4H Reset: 00 _H T2CCU Capture/compare Register 4 High	Bit Field	CCVALH							
		Type	rwh							
C5 _H	T2CCU_CC5L Reset: 00 _H T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL							
		Type	rwh							
C6 _H	T2CCU_CC5H Reset: 00 _H T2CCU Capture/compare Register 5 High	Bit Field	CCVALH							
		Type	rwh							

Functional Description
3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
A3 _H	CCU6_PAGE Page Register Reset: 00 _H	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
9A _H	CCU6_CC63SRL Capture/Compare Shadow Register for Channel CC63 Low Reset: 00 _H	Bit Field	CC63SL							
		Type	rw							
9B _H	CCU6_CC63SRH Capture/Compare Shadow Register for Channel CC63 High Reset: 00 _H	Bit Field	CC63SH							
		Type	rw							
9C _H	CCU6_TCTR4L Timer Control Register 4 Low Reset: 00 _H	Bit Field	T12 STD	T12 STR	0		DT RES	T12 RES	T12R S	T12R R
		Type	w	w	r		w	w	w	w
9D _H	CCU6_TCTR4H Timer Control Register 4 High Reset: 00 _H	Bit Field	T13 STD	T13 STR	0			T13 RES	T13R S	T13R R
		Type	w	w	r			w	w	w
9E _H	CCU6_MCMOUTSL Multi-Channel Mode Output Shadow Register Low Reset: 00 _H	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
9F _H	CCU6_MCMOUTSH Multi-Channel Mode Output Shadow Register High Reset: 00 _H	Bit Field	STRH P	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
A4 _H	CCU6_ISRL Capture/Compare Interrupt Status Reset Register Low Reset: 00 _H	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
		Type	w	w	w	w	w	w	w	w
A5 _H	CCU6_ISRH Capture/Compare Interrupt Status Reset Register High Reset: 00 _H	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
A6 _H	CCU6_CMPMODIFL Compare State Modification Register Low Reset: 00 _H	Bit Field	0	MCC6 3S	0			MCC6 2S	MCC6 1S	MCC6 0S
		Type	r	w	r			w	w	w
A7 _H	CCU6_CMPMODIFH Compare State Modification Register High Reset: 00 _H	Bit Field	0	MCC6 3R	0			MCC6 2R	MCC6 1R	MCC6 0R
		Type	r	w	r			w	w	w
FA _H	CCU6_CC60SRL Capture/Compare Shadow Register for Channel CC60 Low Reset: 00 _H	Bit Field	CC60SL							
		Type	rwh							
FB _H	CCU6_CC60SRH Capture/Compare Shadow Register for Channel CC60 High Reset: 00 _H	Bit Field	CC60SH							
		Type	rwh							

Functional Description
Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD _H	CCU6_CC61RH Reset: 00_H Capture/Compare Register for Channel CC61 High	Bit Field	CC61VH							
		Type	rh							
FE _H	CCU6_CC62RL Reset: 00_H Capture/Compare Register for Channel CC62 Low	Bit Field	CC62VL							
		Type	rh							
FF _H	CCU6_CC62RH Reset: 00_H Capture/Compare Register for Channel CC62 High	Bit Field	CC62VH							
		Type	rh							
RMAP = 0, PAGE 2										
9A _H	CCU6_T12MSELL Reset: 00_H T12 Capture/Compare Mode Select Register Low	Bit Field	MSEL61				MSEL60			
		Type	rw				rw			
9B _H	CCU6_T12MSELH Reset: 00_H T12 Capture/Compare Mode Select Register High	Bit Field	DBYP	HSYNC			MSEL62			
		Type	rw	rw			rw			
9C _H	CCU6_IENL Reset: 00_H Capture/Compare Interrupt Enable Register Low	Bit Field	ENT1 2 PM	ENT1 2 OM	ENCC 62F	ENCC 62R	ENCC 61F	ENCC 61R	ENCC 60F	ENCC 60R
		Type	rw	rw	rw	rw	rw	rw	rw	rw
9D _H	CCU6_IENH Reset: 00_H Capture/Compare Interrupt Enable Register High	Bit Field	EN STR	EN IDLE	EN WHE	EN CHE	0	EN TRPF	ENT1 3PM	ENT1 3CM
		Type	rw	rw	rw	rw	r	rw	rw	rw
9E _H	CCU6_INPL Reset: 40_H Capture/Compare Interrupt Node Pointer Register Low	Bit Field	INPCHE		INPCC62		INPCC61		INPCC60	
		Type	rw		rw		rw		rw	
9F _H	CCU6_INPH Reset: 39_H Capture/Compare Interrupt Node Pointer Register High	Bit Field	0		INPT13		INPT12		INPERR	
		Type	r		rw		rw		rw	
A4 _H	CCU6_ISSL Reset: 00_H Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12 PM	ST12 OM	SCC6 2F	SCC6 2R	SCC6 1F	SCC6 1R	SCC6 0F	SCC6 0R
		Type	w	w	w	w	w	w	w	w
A5 _H	CCU6_ISSH Reset: 00_H Capture/Compare Interrupt Status Set Register High	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWH C	STRP F	ST13 PM	ST13 CM
		Type	w	w	w	w	w	w	w	w
A6 _H	CCU6_PSLR Reset: 00_H Passive State Level Register	Bit Field	PSL63	0	PSL					
		Type	rwh	r	rwh					
A7 _H	CCU6_MCMCTR Reset: 00_H Multi-Channel Mode Control Register	Bit Field	0		SWSYN		0	SWSEL		
		Type	r		rw		r	rw		
FA _H	CCU6_TCTR2L Reset: 00_H Timer Control Register 2 Low	Bit Field	0	T13TED		T13TEC			T13 SSC	T12 SSC
		Type	r	rw		rw			rw	rw
FB _H	CCU6_TCTR2H Reset: 00_H Timer Control Register 2 High	Bit Field	0				T13RSEL		T12RSEL	
		Type	r				rw		rw	
FC _H	CCU6_MODCTRL Reset: 00_H Modulation Control Register Low	Bit Field	MCM EN	0	T12MODEN					
		Type	rw	r	rw					

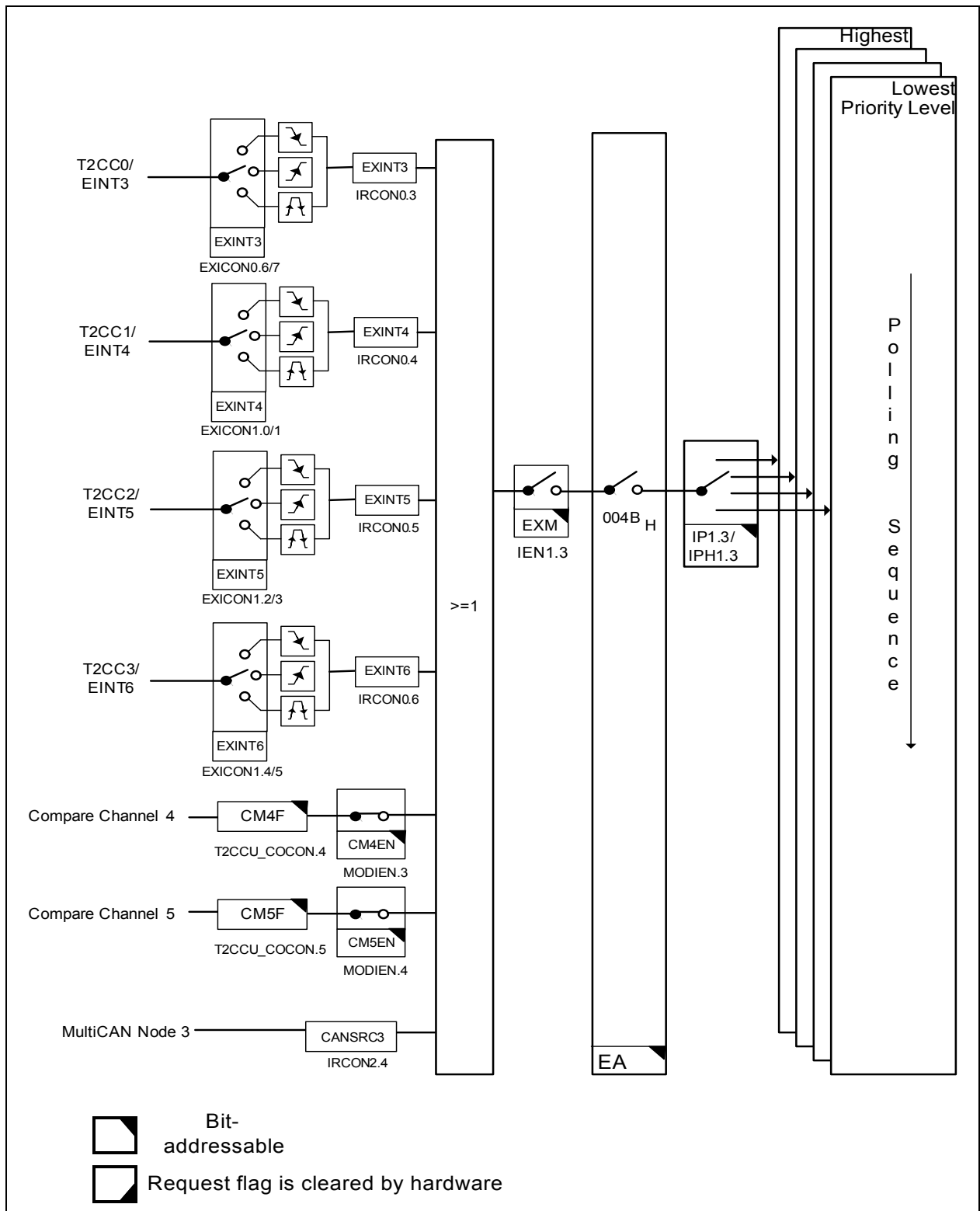


Figure 16 Interrupt Request Sources (Part 4)

3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC87x interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in [Table 22](#).

Table 22 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
NMI	0073 _H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash Timer NMI	NMIFLASH	
		V _{DDP} Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 _H	External Interrupt 0	EX0	IEN0
XINTR1	000B _H	Timer 0	ET0	
XINTR2	0013 _H	External Interrupt 1	EX1	
XINTR3	001B _H	Timer 1	ET1	
XINTR4	0023 _H	UART	ES	
XINTR5	002B _H	T2CCU	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		
		LIN		

Functional Description
Table 22 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
XINTR6	0033 _H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	003B _H	SSC	ESSC	
XINTR8	0043 _H	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	004B _H	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		T2CCU		
		MultiCAN Node 3		
XINTR10	0053 _H	CCU6 INP0	ECCIP0	
		MultiCAN Node 4		
XINTR11	005B _H	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063 _H	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	006B _H	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		

Functional Description

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in [Table 23](#).

Table 23 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
T2CCU, UART Normal Divider Overflow, MultiCAN, LIN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
CCU6 Interrupt Node Pointer 0, MultiCAN interrupt	11
CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt	12
CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt	13
CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt	14

3.5 Parallel Ports

The XC87x has 40 port pins organized into five parallel ports: Port 0 (P0), Port 1 (P1), Port 3 (P3), Port 4 (P4) and Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. These ports are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected.

Bidirectional Port Features

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Functional Description

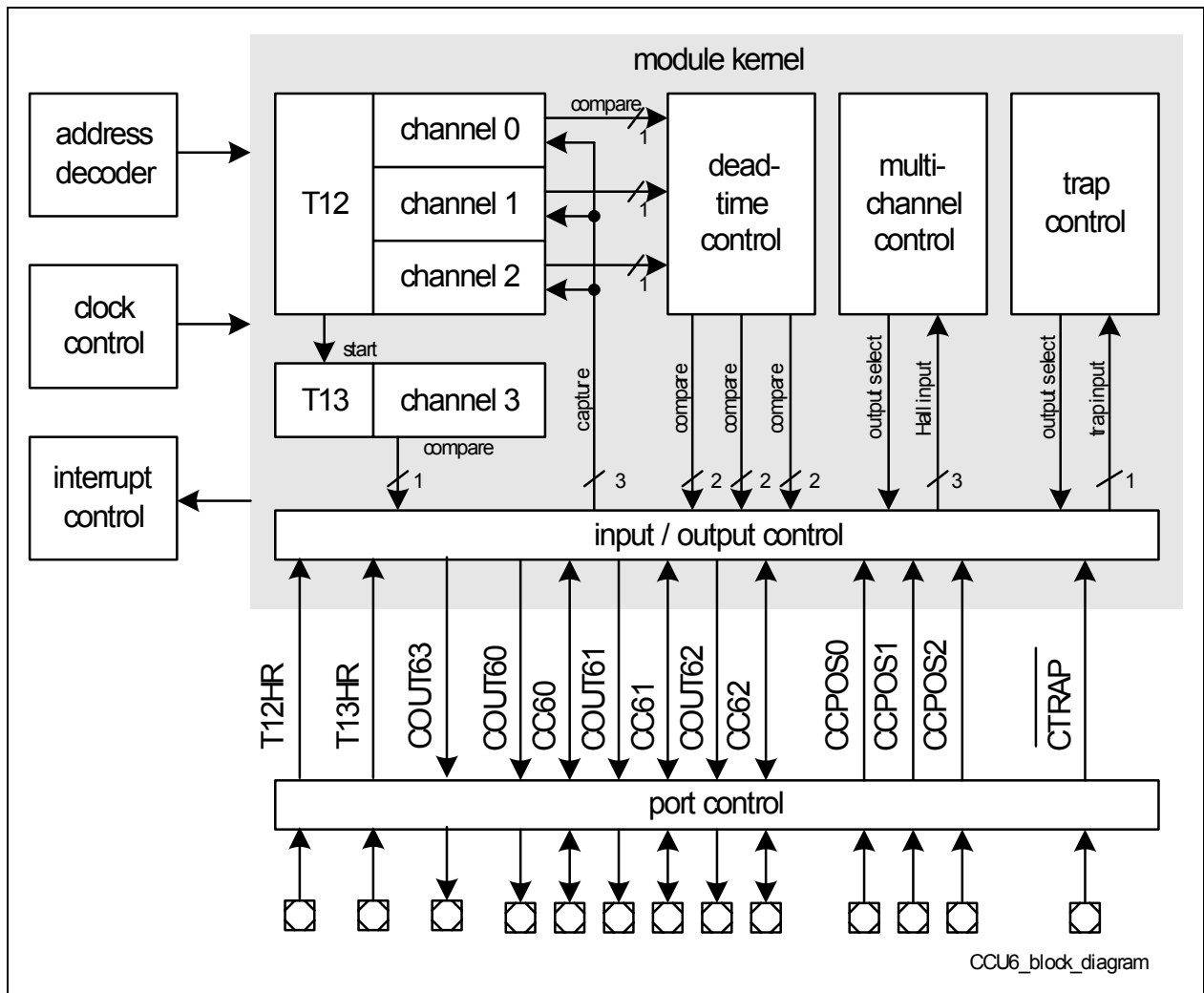


Figure 29 CCU6 Block Diagram

Electrical Parameters
Table 40 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	6)
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR SR	–	8	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma I_M $	SR	–	150	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	200	mA	5)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	200	mA	5)

- 1) DS = 0 refers to the pin having a weak drive strength which is programmable via Px_DS register.
- 2) DS = 1 refers to the pin having a strong drive strength which is programmable via Px_DS register.
- 3) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 4) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{RESET}$ pin have internal pull devices and are not included in the input leakage current characteristic.
- 5) Not subjected to production test, verified by design/characterization.
- 6) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.
- 7) P0.1 has a minimum input hysteresis of 0.25V.

4.3.5 External Data Memory Characteristics

Table 50 shows the timing of the external data memory read cycle.

Table 50 External Data Memory Read Timing¹⁾ (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
$\overline{\text{RD}}$ pulse width	t_1	CC	$2 \cdot f_{\text{CCLK}} - 17$	-	ns	2)
Address valid to $\overline{\text{RD}}$	t_2	CC	$f_{\text{CCLK}} - 12$	-	ns	2)
$\overline{\text{RD}}$ to valid data in	t_3	SR	-	$1.5 \cdot f_{\text{CCLK}} - 27$	ns	2)
Address to valid data in	t_4	SR	-	$3 \cdot f_{\text{CCLK}} - 7$	ns	2)
Data hold after $\overline{\text{RD}}$	t_5	SR	$0.5 \cdot f_{\text{CCLK}} - 17$	-	ns	2)

1) External Bus Interface is not available in XC874.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

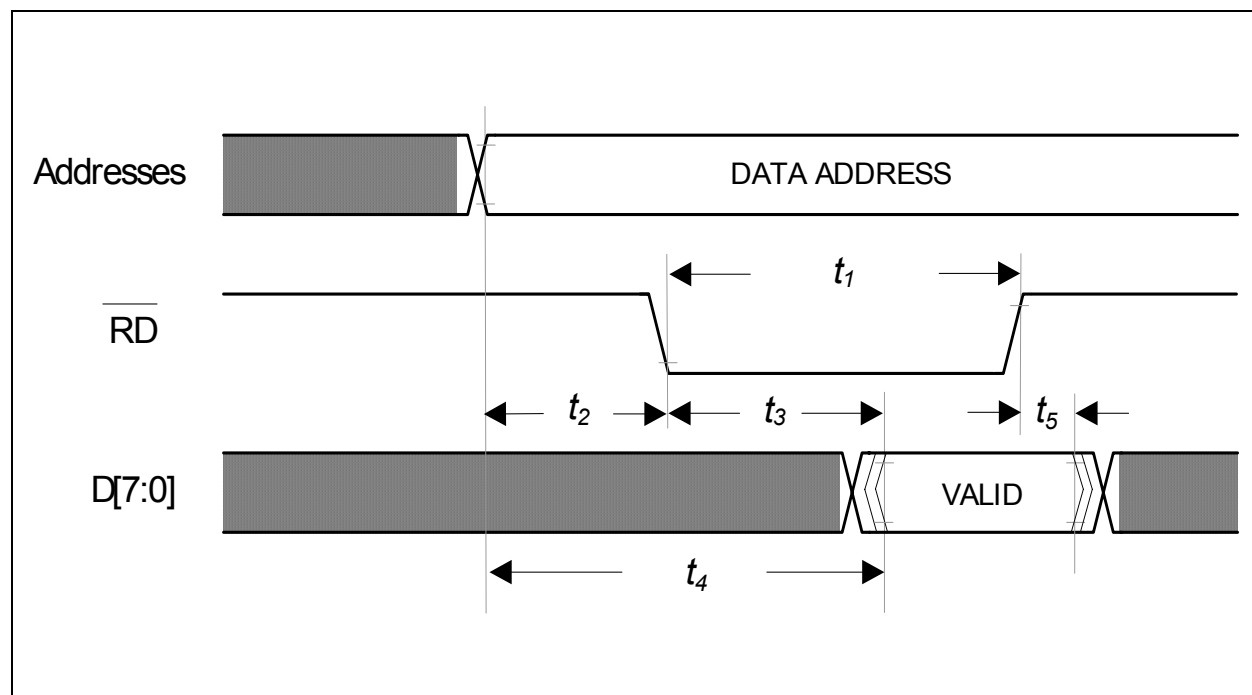


Figure 41 External Data Memory Read Cycle