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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc878-16ffi-5v-aa

Summary of Features

XC87x Variant Devices

The XC87x product family features devices with different configurations, program memory sizes, package options, power supply voltage, temperature and quality profiles (Automotive or Industrial), to offer cost-effective solutions for different application requirements.

The list of XC87x device configurations are summarized in [Table 1](#). 2 types of packages are available :

- PG-LQFP-64, which is denoted by XC878 and;
- PG-VQFN-48, which is denoted by XC874

Table 1 Device Configuration

Device Name	CAN Module	LIN BSL Support	MDU Module
XC87x	No	No	No
XC87xM	No	No	Yes
XC87xCM	Yes	No	Yes
XC87xLM	No	Yes	Yes
XC87xCLM	Yes	Yes	Yes

From these 5 different combinations of configuration, each are further made available in many sales types, which are grouped according to device type, program memory sizes, power supply voltage, temperature and quality profiles (Automotive or Industrial), as shown in [Table 2](#).

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temperature (°C)	Quality Profile
SAF-XC878-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878M-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878CM-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878M-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878CM-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial
SAF-XC878M-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P3.4	51/37		Hi-Z	CC62_0 RXDC0_1 T2EX1_0 T2CC3_1/ EXINT6_3 A14	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input External Interrupt Input 6/T2CCU Capture/Compare Channel 3 Address Line 14 Output
P3.5	52/38		Hi-Z	COUT62_0 EXF21_0 TXDC0_1 A15	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output Address Line 15 Output
P3.6	41/32		PU	CTR $\overline{\text{AP}}$ _0	CCU6 Trap Input
P3.7	42/-		Hi-Z	EXINT4_0 COUT63_0 A16	External Interrupt Input 4 Output of Capture/Compare channel 3 Address Line 16 Output

General Device Information

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
V_{DDP}	7, 25, 55/ 17, 41	—	—	I/O Port Supply (3.3 or 5.0 V) Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	26, 54/ 18, 40	—	—	I/O Ground All pins must be connected.
V_{DDC}	6/8	—	—	Core Supply Monitor (2.5 V)
V_{SSC}	5/7	—	—	Core Supply Ground
V_{AREF}	32/23	—	—	ADC Reference Voltage
V_{AGND}	31/22	—	—	ADC Reference Ground
AN0	22/-	I	Hi-Z	Analog Input 0
AN1	23/15	I	Hi-Z	Analog Input 1
AN2	24/16	I	Hi-Z	Analog Input 2
AN3	27/-	I	Hi-Z	Analog Input 3
AN4	28/19	I	Hi-Z	Analog Input 4
AN5	29/20	I	Hi-Z	Analog Input 5
AN6	30/21	I	Hi-Z	Analog Input 6
AN7	33/24	I	Hi-Z	Analog Input 7
XTAL1	4/6	I	Hi-Z	External Oscillator Input (Feedback resistor required, normally NC)
XTAL2	3/5	O	Hi-Z	External Oscillator Output (Feedback resistor required, normally NC)
TMS	16/11	I	PD	JTAG Test Mode Select
RESET	53/39	I	PU	Reset Input
MBC	58/44	I	PU	Monitor & BootStrap Loader Control
TM	57/43	—	—	Test Mode (External pull down device required)
NC	56/42	—	—	No Connection

Functional Description

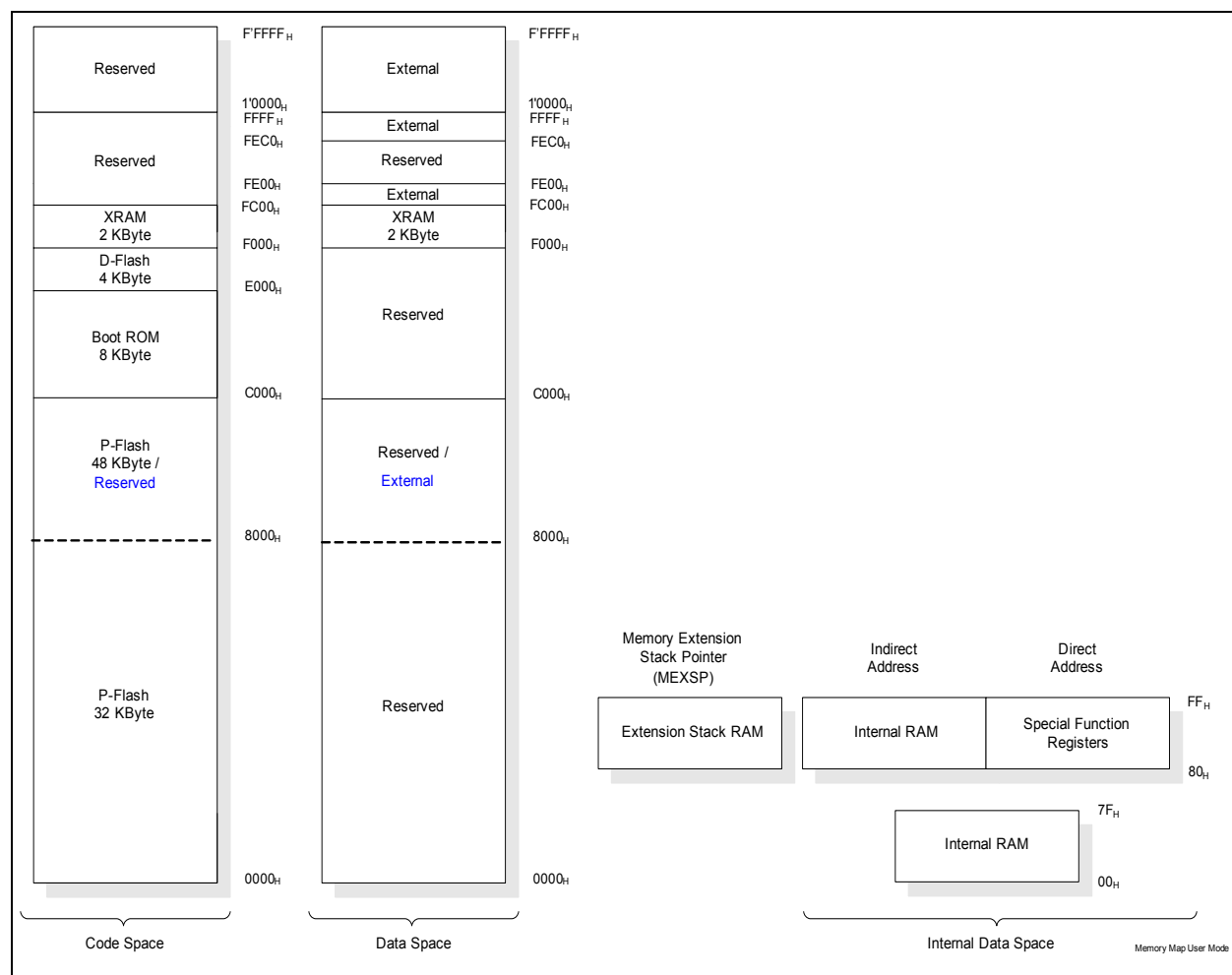


Figure 8 Memory Map of XC87x with 52K Flash Memory in user mode

Functional Description

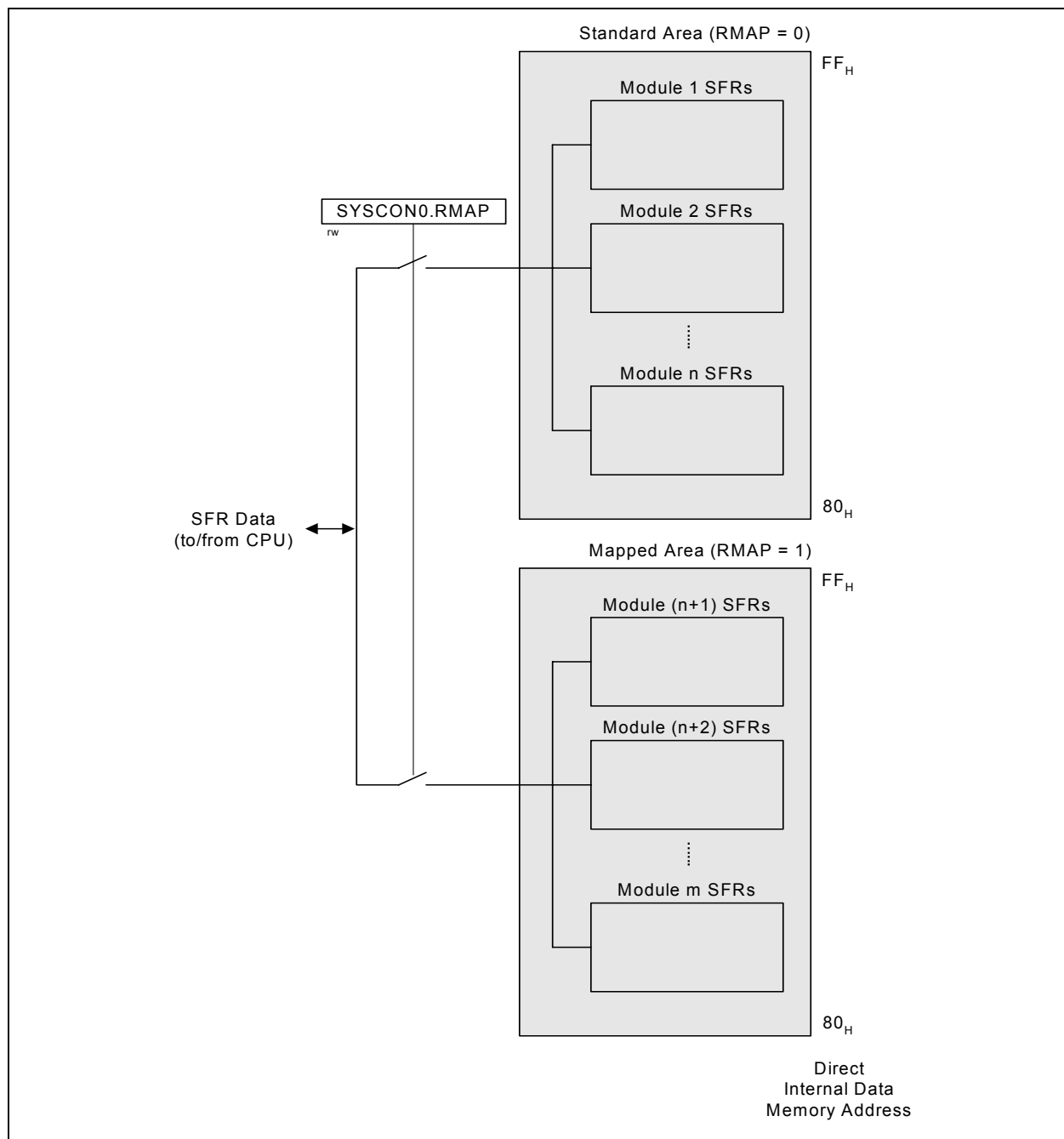


Figure 9 Address Extension by Mapping

Functional Description

3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB _H	WDTCON Reset: 00 _H Watchdog Timer Control Register	Bit Field	0		WINB EN	WDTP R	0	WDTE N	WDTR S	WDTI N
		Type	r		rw	rh	r	rw	rwh	rw
BC _H	WDTREL Reset: 00 _H Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD _H	WDTWINB Reset: 00 _H Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							
BE _H	WDTL Reset: 00 _H Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF _H	WDTH Reset: 00 _H Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
B2 _H	PORT_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
80 _H	P0_DATA Reset: 00_H P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
86 _H	P0_DIR Reset: 00_H P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_DATA Reset: 00_H P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
91 _H	P1_DIR Reset: 00_H P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_DATA Reset: 00_H P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
93 _H	P5_DIR Reset: 00_H P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Functional Description
Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B0 _H	P3_DATA Reset: 00_H P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B1 _H	P3_DIR Reset: 00_H P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_DATA Reset: 00_H P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
C9 _H	P4_DIR Reset: 00_H P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 1										
80 _H	P0_PUDSEL Reset: FF_H P0 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_PUDEN Reset: C4_H P0 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_PUDSEL Reset: FF_H P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91 _H	P1_PUDEN Reset: FF_H P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_PUDSEL Reset: FF_H P5 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93 _H	P5_PUDEN Reset: FF_H P5 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_PUDSEL Reset: BF_H P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_PUDEN Reset: 40_H P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_PUDSEL Reset: FF_H P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_PUDEN Reset: 04_H P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80 _H	P0_ALTSEL0 Reset: 00_H P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_ALTSEL1 Reset: 00_H P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_ALTSEL0 Reset: 00_H P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Functional Description
3.2.4.7 ADC Registers

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 11 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
D1 _H	ADC_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
CA _H	ADC_GLOBCTR Reset: 30_H Global Control Register	Bit Field	ANON	DW	CTC		0			
		Type	rw	rw	rw		r			
CB _H	ADC_GLOBSTR Reset: 00_H Global Status Register	Bit Field	0		CHNR			0	SAMP LE	BUSY
		Type	r		rh			r	rh	rh
CC _H	ADC_PRAR Reset: 00_H Priority and Arbitration Register	Bit Field	ASEN 1	ASEN 0	0	ARBM	CSM1	PRI01	CSM0	PRI00
		Type	rw	rw	r	rw	rw	rw	rw	rw
CD _H	ADC_LCBR Reset: B7_H Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE _H	ADC_INPCR0 Reset: 00_H Input Class 0 Register	Bit Field	STC							
		Type	rw							
CF _H	ADC_ETRCR Reset: 00_H External Trigger Control Register	Bit Field	SYNE N1	SYNE N0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, PAGE 1										
CA _H	ADC_CHCTR0 Reset: 00_H Channel Control Register 0	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CB _H	ADC_CHCTR1 Reset: 00_H Channel Control Register 1	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CC _H	ADC_CHCTR2 Reset: 00_H Channel Control Register 2	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CD _H	ADC_CHCTR3 Reset: 00_H Channel Control Register 3	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CE _H	ADC_CHCTR4 Reset: 00_H Channel Control Register 4	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CF _H	ADC_CHCTR5 Reset: 00_H Channel Control Register 5	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D2 _H	ADC_CHCTR6 Reset: 00_H Channel Control Register 6	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D3 _H	ADC_CHCTR7 Reset: 00_H Channel Control Register 7	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		

Functional Description
Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD _H	CCU6_CC61RH Reset: 00_H Capture/Compare Register for Channel CC61 High	Bit Field	CC61VH							
		Type	rh							
FE _H	CCU6_CC62RL Reset: 00_H Capture/Compare Register for Channel CC62 Low	Bit Field	CC62VL							
		Type	rh							
FF _H	CCU6_CC62RH Reset: 00_H Capture/Compare Register for Channel CC62 High	Bit Field	CC62VH							
		Type	rh							
RMAP = 0, PAGE 2										
9A _H	CCU6_T12MSELL Reset: 00_H T12 Capture/Compare Mode Select Register Low	Bit Field	MSEL61				MSEL60			
		Type	rw				rw			
9B _H	CCU6_T12MSELH Reset: 00_H T12 Capture/Compare Mode Select Register High	Bit Field	DBYP	HSYNC			MSEL62			
		Type	rw	rw			rw			
9C _H	CCU6_IENL Reset: 00_H Capture/Compare Interrupt Enable Register Low	Bit Field	ENT1 2 PM	ENT1 2 OM	ENCC 62F	ENCC 62R	ENCC 61F	ENCC 61R	ENCC 60F	ENCC 60R
		Type	rw	rw	rw	rw	rw	rw	rw	rw
9D _H	CCU6_IENH Reset: 00_H Capture/Compare Interrupt Enable Register High	Bit Field	EN STR	EN IDLE	EN WHE	EN CHE	0	EN TRPF	ENT1 3PM	ENT1 3CM
		Type	rw	rw	rw	rw	r	rw	rw	rw
9E _H	CCU6_INPL Reset: 40_H Capture/Compare Interrupt Node Pointer Register Low	Bit Field	INPCHE		INPCC62		INPCC61		INPCC60	
		Type	rw		rw		rw		rw	
9F _H	CCU6_INPH Reset: 39_H Capture/Compare Interrupt Node Pointer Register High	Bit Field	0		INPT13		INPT12		INPERR	
		Type	r		rw		rw		rw	
A4 _H	CCU6_ISSL Reset: 00_H Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12 PM	ST12 OM	SCC6 2F	SCC6 2R	SCC6 1F	SCC6 1R	SCC6 0F	SCC6 0R
		Type	w	w	w	w	w	w	w	w
A5 _H	CCU6_ISSH Reset: 00_H Capture/Compare Interrupt Status Set Register High	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWH C	STRP F	ST13 PM	ST13 CM
		Type	w	w	w	w	w	w	w	w
A6 _H	CCU6_PSLR Reset: 00_H Passive State Level Register	Bit Field	PSL63	0	PSL					
		Type	rwh	r	rwh					
A7 _H	CCU6_MCMCTR Reset: 00_H Multi-Channel Mode Control Register	Bit Field	0		SWSYN		0	SWSEL		
		Type	r		rw		r	rw		
FA _H	CCU6_TCTR2L Reset: 00_H Timer Control Register 2 Low	Bit Field	0	T13TED		T13TEC			T13 SSC	T12 SSC
		Type	r	rw		rw			rw	rw
FB _H	CCU6_TCTR2H Reset: 00_H Timer Control Register 2 High	Bit Field	0				T13RSEL		T12RSEL	
		Type	r				rw		rw	
FC _H	CCU6_MODCTRL Reset: 00_H Modulation Control Register Low	Bit Field	MCM EN	0	T12MODEN					
		Type	rw	r	rw					

Functional Description

Table 18 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
E9 _H	MMCR2 Reset: 8U_H Monitor Mode Control 2 Register	Bit Field	STMO DE	EXBC	DSUS P	MBCO N	ALTDI	MMEP	MMOD E	JENA
		Type	rw	rw	rw	rwh	rw	rwh	rh	rh
EA _H	MEXTCR Reset: 0U_H Memory Extension Control Register	Bit Field	0				BANKBPx			
		Type	r				rw			
EB _H	MMWR1 Reset: 00_H Monitor Work Register 1	Bit Field	MMWR1							
		Type	rw							
EC _H	MMWR2 Reset: 00_H Monitor Work Register 2	Bit Field	MMWR2							
		Type	rw							
F1 _H	MMCR Reset: 00_H Monitor Mode Control Register	Bit Field	MEXIT _P	MEXIT	0	MSTE P	MRAM S_P	MRAM S	TRF	RRF
		Type	w	rwh	r	rw	w	rwh	rh	rh
F2 _H	MMSR Reset: 00_H Monitor Mode Status Register	Bit Field	MBCA M	MBCIN	EXBF	SWBF	HWB3 F	HWB2 F	HWB1 F	HWB0 F
		Type	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
F3 _H	MMBPCR Reset: 00_H Breakpoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1 C	HWB0C	
		Type	rw	rw		rw		rw	rw	
F4 _H	MMICR Reset: 00_H Monitor Mode Interrupt Control Register	Bit Field	DVEC T	DRET R	COMR ST	MSTS EL	MMUI E_P	MMUI E	RRIE_ P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
F5 _H	MMDR Reset: 00_H Monitor Mode Data Transfer Register Receive	Bit Field	MMRR							
		Type	rh							
F6 _H	HWBPSR Reset: 00_H Hardware Breakpoints Select Register	Bit Field	0			BPSEL _P	BPSEL			
		Type	r			w	rw			
F7 _H	HWBPDR Reset: 00_H Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							

Functional Description
3.2.4.15 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 19 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
D1 _H	FCON Reset: 10_H P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D2 _H	EECON Reset: 10_H D-Flash Control Register	Bit Field	0	EEBS Y	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D3 _H	FCS Reset: 80_H Flash Control and Status Register	Bit Field	1	SBEIE	FTEN	0	EEDE RR	EESE RR	FDER R	FSER R
		Type	r	rw	rwh	r	rwh	rwh	rwh	rwh
D4 _H	FEAL Reset: 00_H Flash Error Address Register, Low Byte	Bit Field	ECCEADDR							
		Type	rh							
D5 _H	FEAH Reset: 00_H Flash Error Address Register, High Byte	Bit Field	ECCEADDR							
		Type	rh							
D6 _H	FTVAL Reset: 78_H Flash Timer Value Register	Bit Field	MODE	OFVAL						
		Type	rw	rw						
DD _H	FCS1 Reset: 00_H Flash Control and Status Register 1	Bit Field	0							EEAB ORT
		Type	r							rwh

3.6 Power Supply System with Embedded Voltage Regulator

The XC87x microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 19 shows the XC87x power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode¹⁾, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

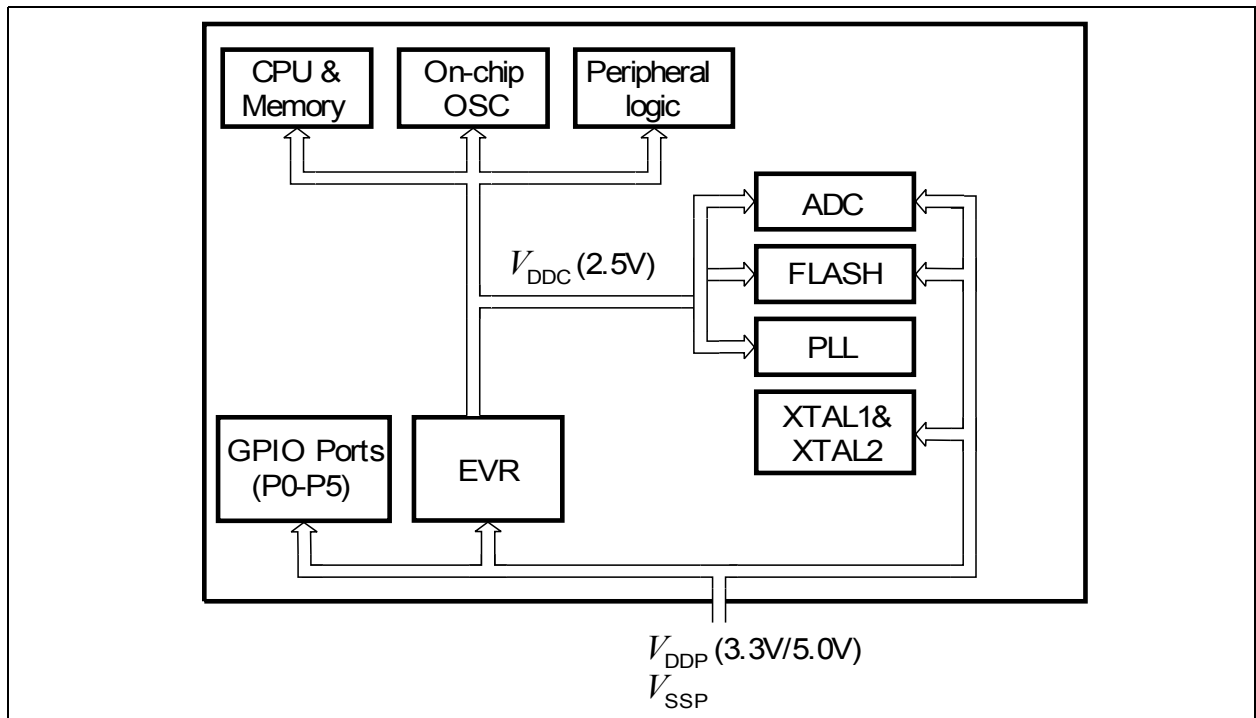


Figure 19 XC87x Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V $\pm$ 7.5%
- Low power voltage regulator provided in power-down mode¹⁾
- V_{DDP} prewarning detection
- V_{DDC} brownout detection

1) SAK product variant does not support power-down mode.

Functional Description

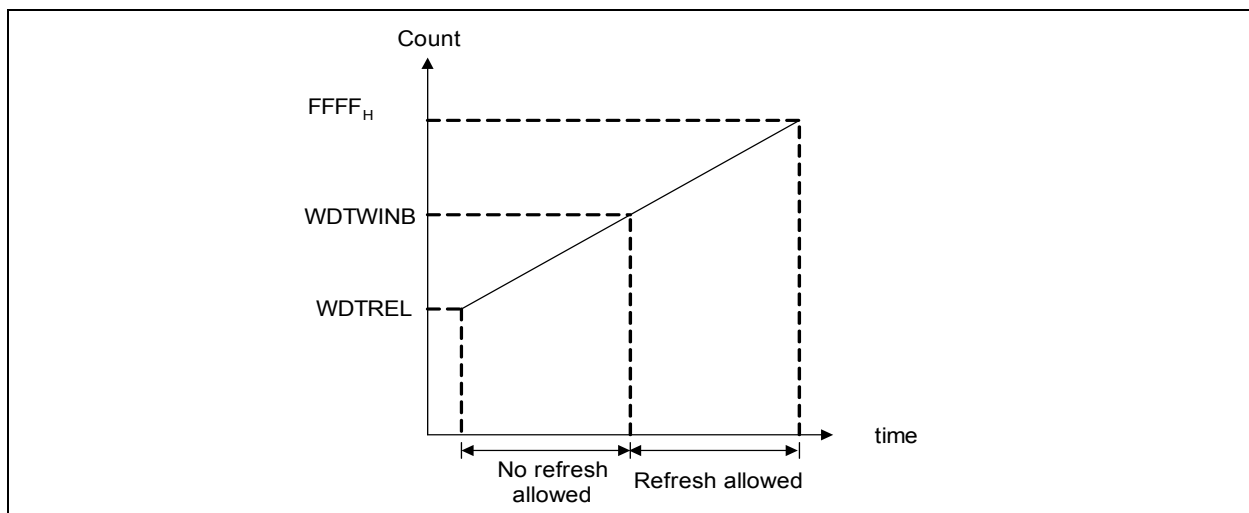


Figure 25 WDT Timing Diagram

Table 28 lists the possible watchdog time ranges that can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 28 Watchdog Time Ranges

Reload value In WDTREL	Prescaler for f_{PCLK}	
	2 (WDTIN = 0)	128 (WDTIN = 1)
	24 MHz	24 MHz
FF _H	21.3 μ s	1.37 ms
7F _H	2.75 ms	176 ms
00 _H	5.46 ms	350 ms

Functional Description

The following formulas calculate the final baud rate without and with the fractional divider respectively:

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \quad \text{where } 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1) > 1$$

(3.4)

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \times \frac{\text{STEP}}{256}$$

(3.5)

The maximum baud rate that can be generated is limited to $f_{\text{PCLK}}/32$. Hence, for a module clock of 24 MHz, the maximum achievable baud rate is 0.75 MBaud.

Standard LIN protocol can support a maximum baud rate of 20 kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20 kHz to 57.6 kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

Table 31 lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 24 MHz is used.

Table 31 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000 _B)	78 (4E _H)	0.17 %
9600 Baud	1 (BRPRE=000 _B)	156 (9C _H)	0.17 %
4800 Baud	2 (BRPRE=001 _B)	156 (9C _H)	0.17 %
2400 Baud	4 (BRPRE=010 _B)	156 (9C _H)	0.17 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 32** lists the resulting deviation errors from generating a baud rate of 57.6 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

Functional Description

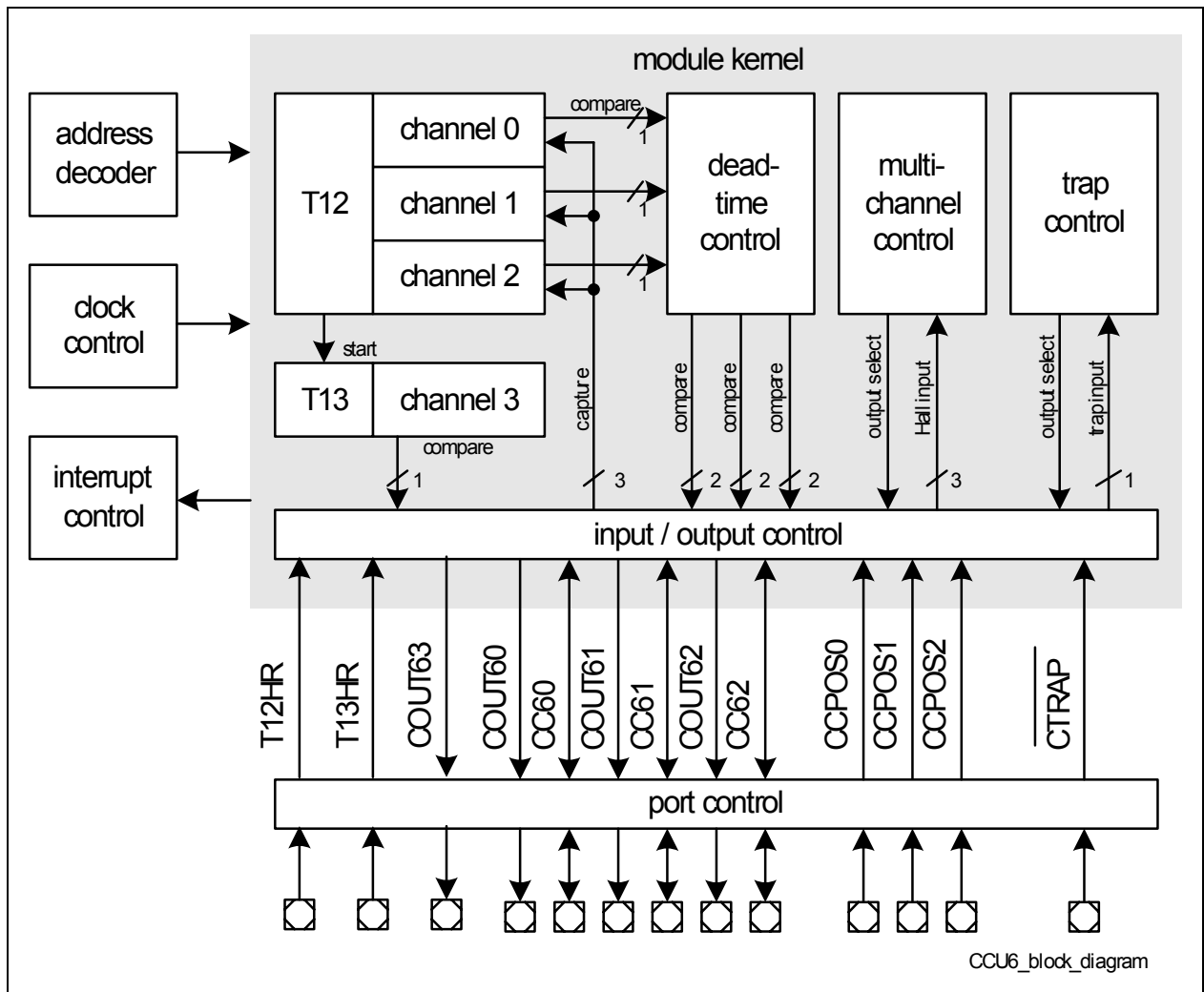


Figure 29 CCU6 Block Diagram

Functional Description

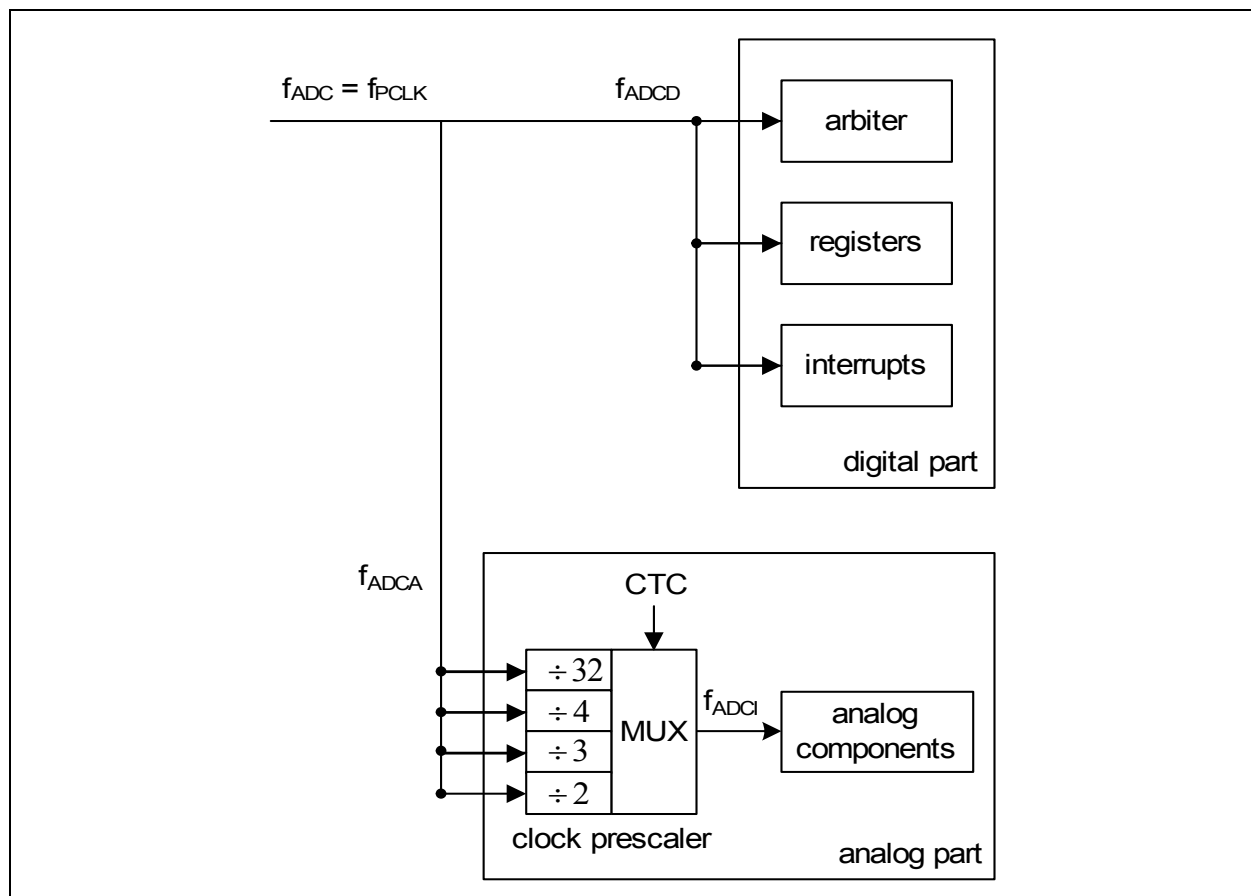


Figure 31 ADC Clocking Scheme

For module clock $f_{\text{ADC}} = 24 \text{ MHz}$, the analog clock f_{ADCl} frequency can be selected as shown in [Table 35](#).

Table 35 f_{ADCl} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCl}
24 MHz	00 _B	÷ 2	12 MHz
	01 _B	÷ 3	8 MHz
	10 _B	÷ 4	6 MHz
	11 _B (default)	÷ 32	750 kHz

During slow-down mode, f_{ADC} may be reduced further, for example, to 12 MHz or 6 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.22.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

Electrical Parameters
4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC87x. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 39 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
CPU Clock Frequency ¹⁾	f_{CCLK}		26.67 ²⁾	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC878/874...
		-40	105	°C	SAX-XC878...
		-40	125	°C	SAK-XC878/874...

1) f_{CCLK} is the input frequency to the XC800 core. Please refer to [Figure 22](#) for detailed description.

2) Default setting of f_{CCLK} upon reset is 24 MHz.

Electrical Parameters

Table 54 JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter	Symbol	Limits		Unit	Test Conditions
		min	max		
TDO high impedance to valid output from TCK	t_4 CC	-	18	ns	5V Device ¹⁾
		-	21	ns	3.3V Device ¹⁾
TDO valid output to high impedance from TCK	t_5 CC	-	21	ns	5V Device ¹⁾
		-	20	ns	3.3V Device ¹⁾

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

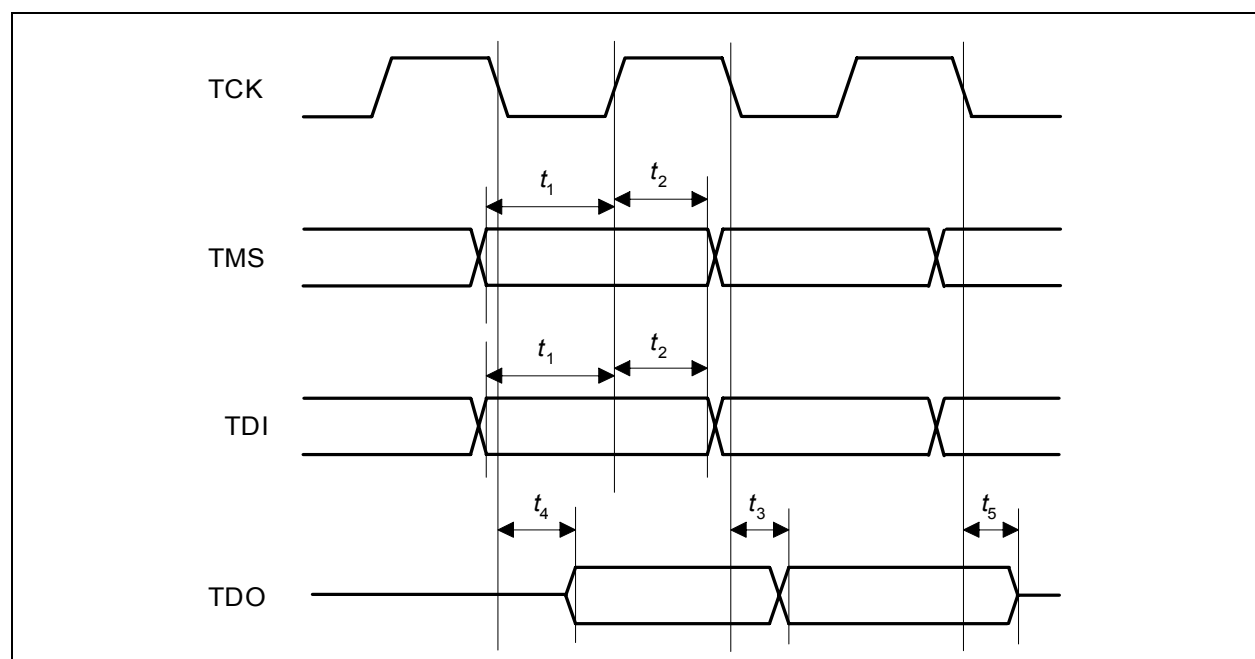


Figure 45 JTAG Timing

4.3.8 SSC Master Mode Timing

Table 55 provides the characteristics of the SSC timing in the XC87x.

Table 55 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
SCLK clock period	t_0	CC	$2 \cdot T_{SSC}$	–	ns	1)2)
MTSR delay from SCLK	t_1	CC	0	5	ns	2)
MRST setup to SCLK	t_2	SR	13	–	ns	2)
MRST hold from SCLK	t_3	SR	0	–	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 83.3$ ns. T_{CPU} is the CPU clock period.

2) 1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

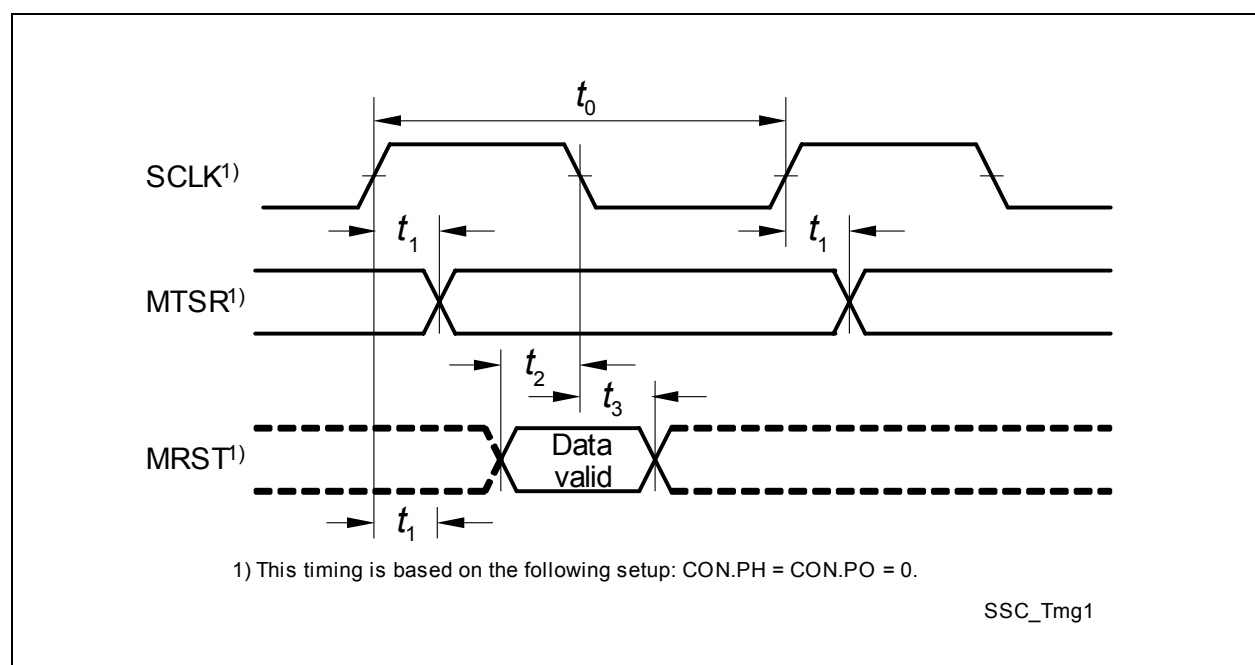


Figure 46 SSC Master Mode Timing

5 Package and Quality Declaration

Chapter 5 provides the information of the XC87x package and reliability section.

5.1 Package Parameters

Table 56 provides the thermal characteristics of the package used in XC878 and XC874.

Table 56 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Notes	
		Min.	Max.			
PG-LQFP-64-4 (XC878)						
Thermal resistance junction case ¹⁾	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead ¹⁾	R_{TJL}	CC	-	34.6	K/W	-
PG-VQFN-48-22 (XC874)						
Thermal resistance junction case ¹⁾	R_{TJC}	CC	-	16.6	K/W	-
Thermal resistance junction lead ¹⁾	R_{TJL}	CC	-	30.7	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by

- simply adding only the two thermal resistances (junction lead and lead ambient), or
- by taking all four resistances into account, depending on the precision needed.