Infineon Technologies - SAF-XC878M-13FFI 5V AA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc878m-13ffi-5v-aa

Table 2 Device Profile (cont'd)

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp-erature (°C)	Quality Profile
SAF-XC878CM-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial
SAF-XC878-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878M-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878CM-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAX-XC878-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAK-XC878-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAF-XC874LM-16FVA 5V	Flash	64	5.0	-40 to 85	Automotive

2.3 Pin Configuration

The pin configuration of the XC878, which is based on the PG-LQFP-64, is shown in **Figure 4**, while that of the XC874, which is based on the PG-VQFN-48 package, is shown in **Figure 5**.

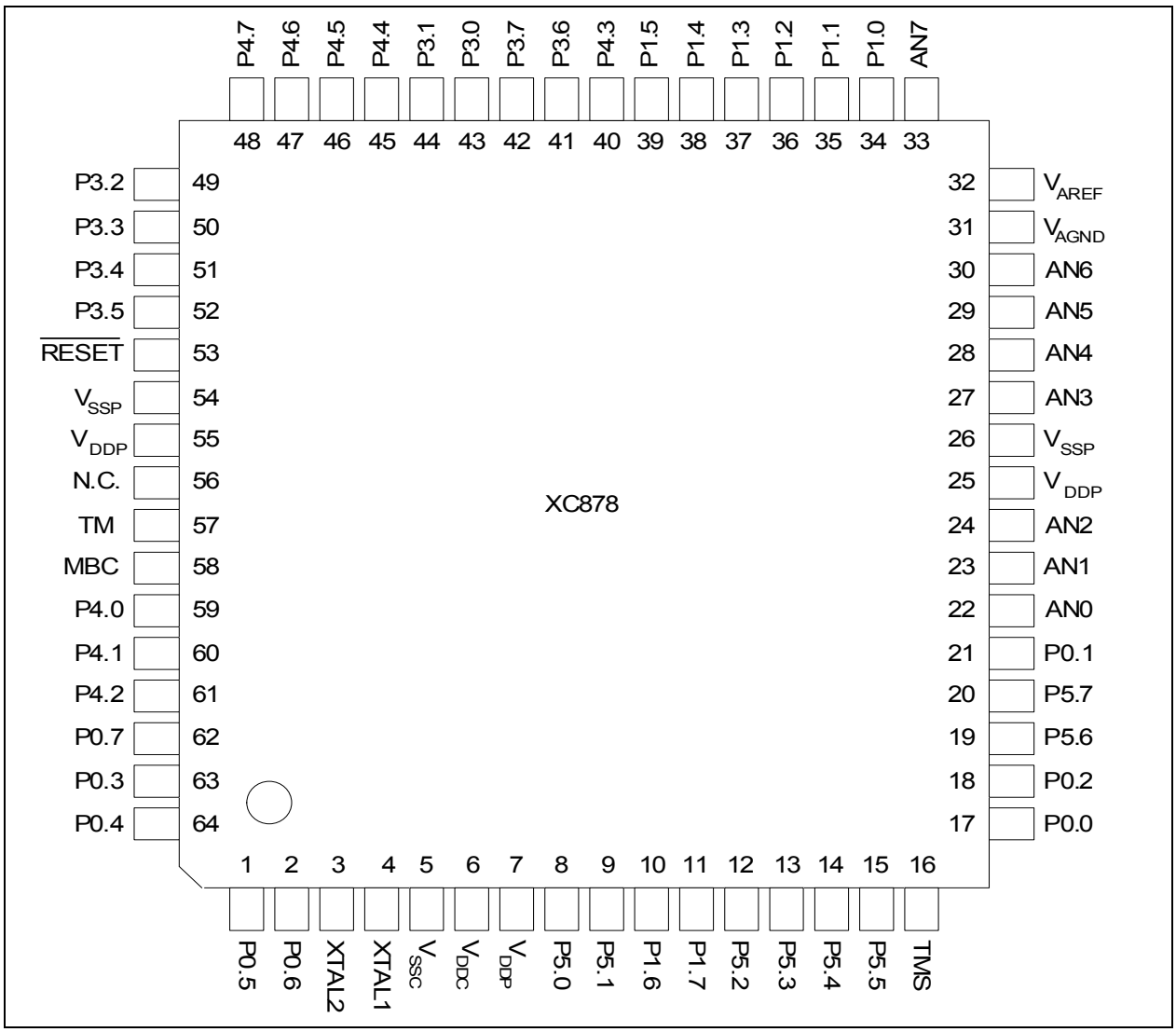

Figure 4 XC878 Pin Configuration, PG-LQFP-64 Package (top view)

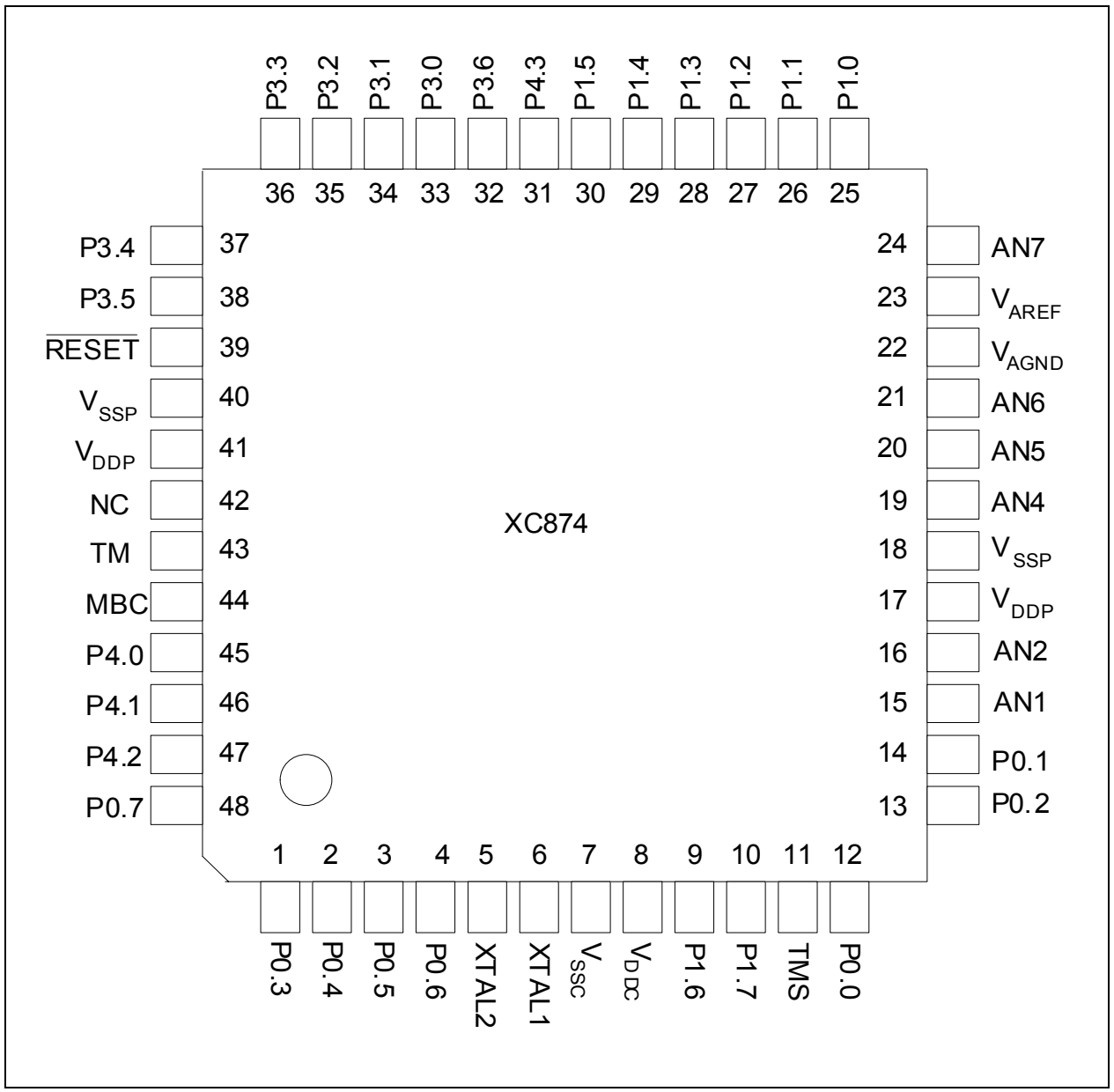

Figure 5 XC874 Pin Configuration, PG-VQFN-48 Package (top view)

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P0.3	63/1		Hi-Z	SCK_1 COUT63_1 RXDO1_0 A17	SSC Clock Input/Output Output of Capture/Compare channel 3 UART1 Transmit Data Output Address Line 17 Output
P0.4	64/2		Hi-Z	MTSR_1 CC62_1 TXD1_0 A18	SSC Master Transmit Output/ Slave Receive Input Input/Output of Capture/Compare channel 2 UART1 Transmit Data Output/Clock Output Address Line 18 Output
P0.5	1/3		Hi-Z	MRST_1 EXINT0_0 T2EX1_1 RXD1_0 COUT62_1 A19	SSC Master Receive Input/Slave Transmit Output External Interrupt Input 0 Timer 21 External Trigger Input UART1 Receive Data Input Output of Capture/Compare channel 2 Address Line 19 Output
P0.6	2/4		PU	$\overline{\text{T2CC4\_1}}$ $\overline{\text{WR}}$	Compare Output Channel 4 External Data Write Control Output
P0.7	62/48		PU	CLKOUT_1 $\overline{\text{T2CC5\_1}}$ $\overline{\text{RD}}$	Clock Output Compare Output Channel 5 External Data Read Control Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface. *Note: External Bus Interface is not available in XC874.*
P1.0	34/25		PU	RXD_0 UART Receive Data Input T2EX_0 Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input A8 Address Line 8 Output
P1.1	35/26		PU	EXINT3_0 External Interrupt Input 3 T0_1 Timer 0 Input TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output A9 Address Line 9 Output
P1.2	36/27		PU	SCK_0 SSC Clock Input/Output A10 Address Line 10 Output
P1.3	37/28		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input SCK_2 SSC Clock Input/Output TXDC1_3 MultiCAN Node 1 Transmitter Output A11 Address Line 11 Output
P1.4	38/29		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input MTSR_2 SSC Master Transmit Output/Slave Receive Input A12 Address Line 12 Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P4		I/O		**Port 4** Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Bus Interface. *Note: External Bus Interface is not available in XC874.*	
P4.0	59/45		Hi-Z	RXDC0_3 CC60_1 T2CC0_0/ EXINT3_1 D0	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0 External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Data Line 0 Input/Output
P4.1	60/46		Hi-Z	TXDC0_3 COUT60_1 T2CC1_0/ EXINT4_1 D1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0 External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Data Line 1 Input/Output
P4.2	61/47		PU	EXINT6_1 T21_0 D2	External Interrupt Input 6 Timer 21 Input Data Line 2 Input/Output
P4.3	40/31		Hi-Z	T2EX_1 EXF21_1 COUT63_2 D3	Timer 2 External Trigger Input Timer 21 External Flag Output Output of Capture/Compare channel 3 Data Line 3 Input/Output
P4.4	45/-		Hi-Z	CCPOS0_3 T0_0 CC61_4 T2CC2_0/ EXINT5_1 D4	CCU6 Hall Input 0 Timer 0 Input Output of Capture/Compare channel 1 External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Data Line 4 Input/Output

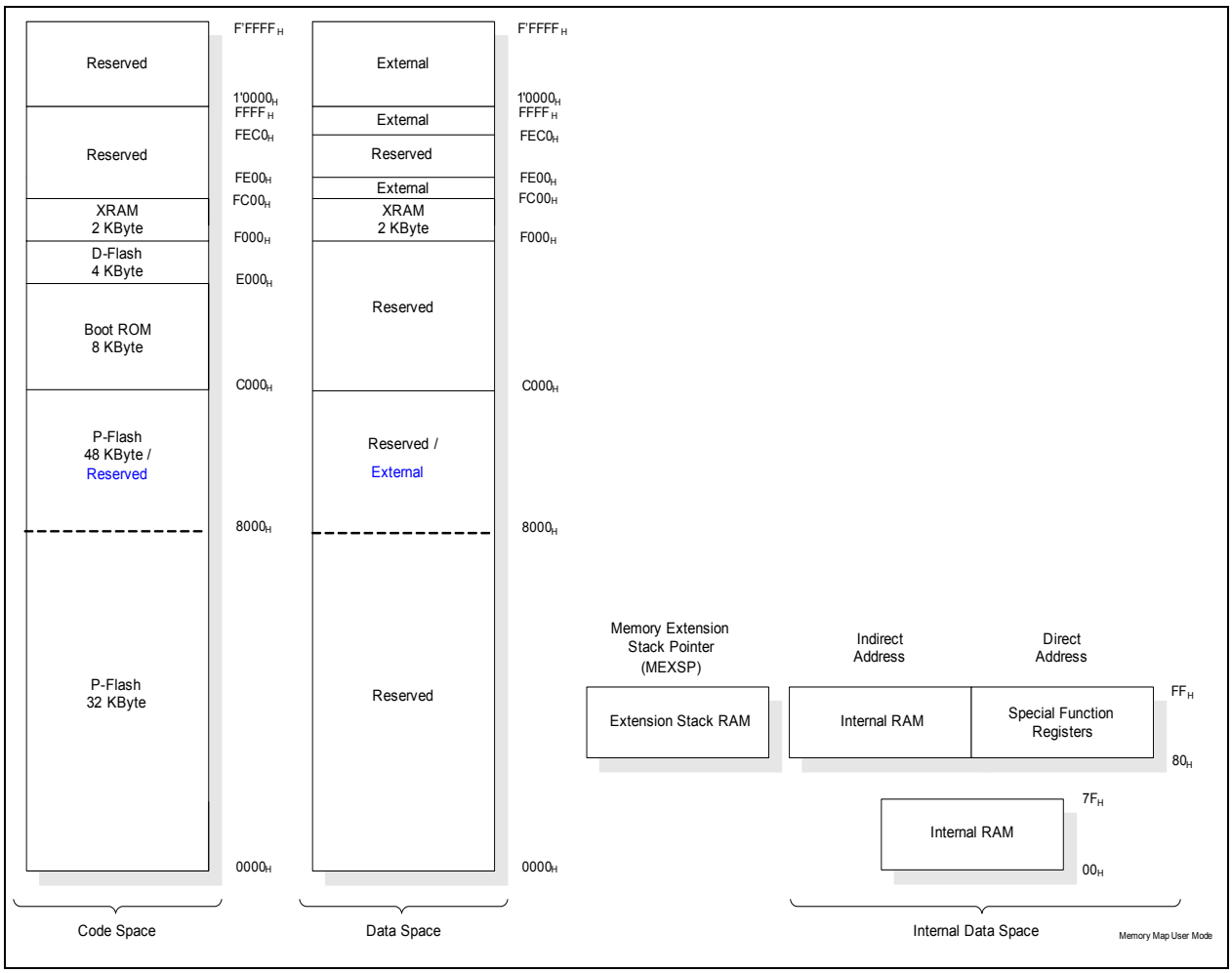

Figure 8 Memory Map of XC87x with 52K Flash Memory in user mode

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 9**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

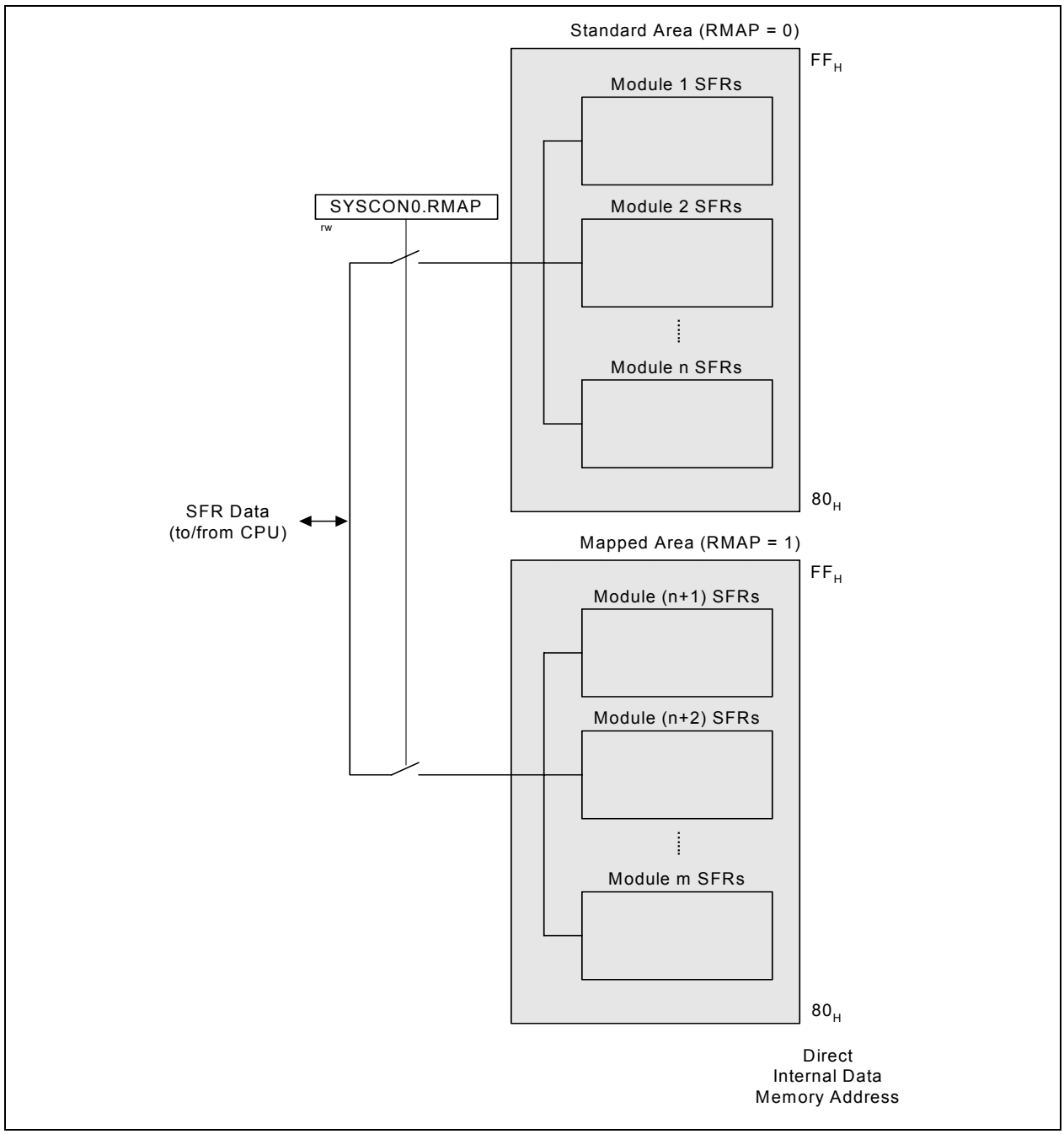

Figure 9 Address Extension by Mapping

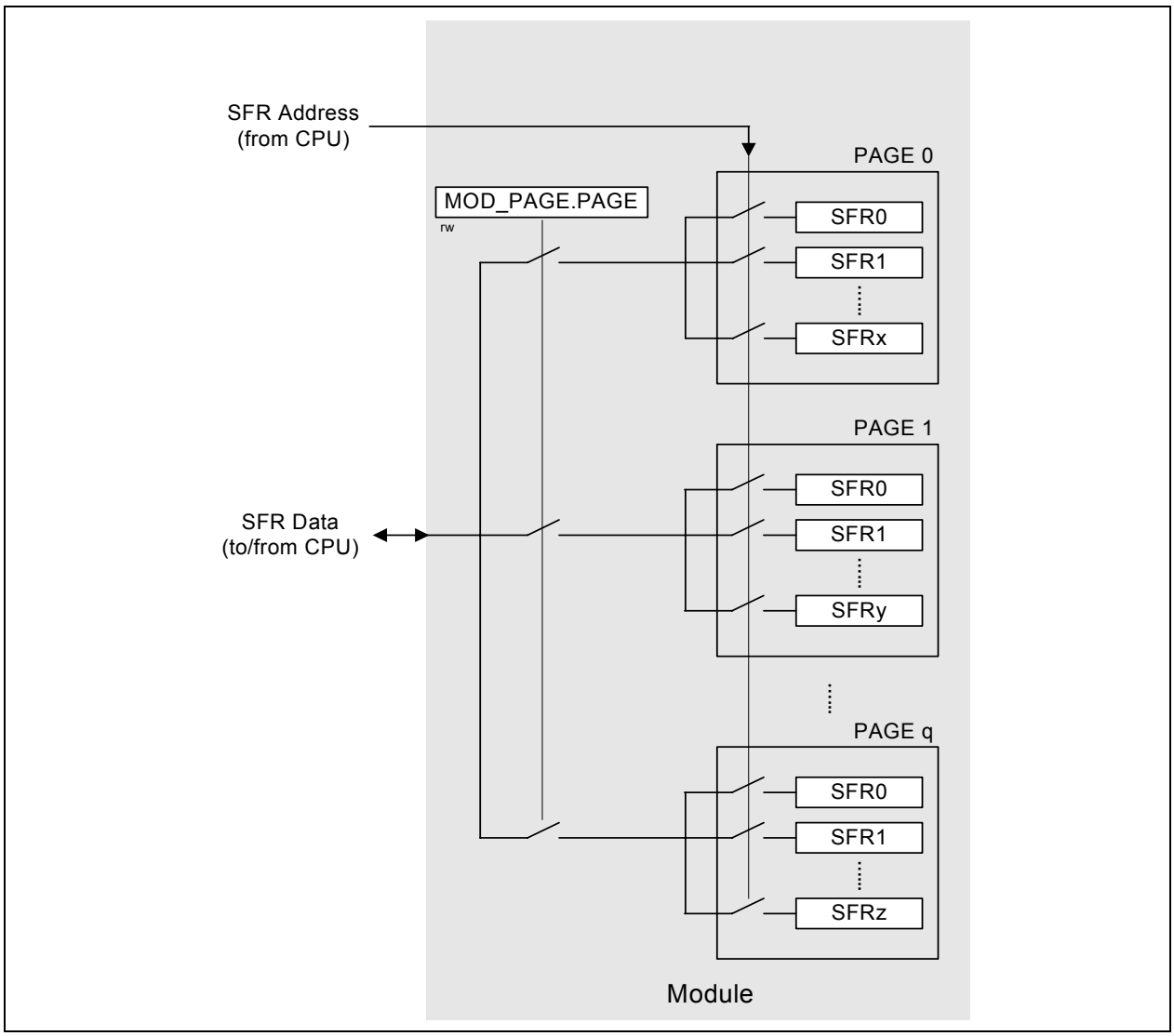

Figure 10 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 2										
CA_H	**ADC_RESR0L Reset: 00_H** Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB_H	**ADC_RESR0H Reset: 00_H** Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC_H	**ADC_RESR1L Reset: 00_H** Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD_H	**ADC_RESR1H Reset: 00_H** Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE_H	**ADC_RESR2L Reset: 00_H** Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF_H	**ADC_RESR2H Reset: 00_H** Result Register 2 High	Bit Field	RESULT							
		Type	rh							
$D2_H$	**ADC_RESR3L Reset: 00_H** Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
$D3_H$	**ADC_RESR3H Reset: 00_H** Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										
CA_H	**ADC_RESRA0L Reset: 00_H** Result Register 0, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB_H	**ADC_RESRA0H Reset: 00_H** Result Register 0, View A High	Bit Field	RESULT							
		Type	rh							
CC_H	**ADC_RESRA1L Reset: 00_H** Result Register 1, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD_H	**ADC_RESRA1H Reset: 00_H** Result Register 1, View A High	Bit Field	RESULT							
		Type	rh							
CE_H	**ADC_RESRA2L Reset: 00_H** Result Register 2, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF_H	**ADC_RESRA2H Reset: 00_H** Result Register 2, View A High	Bit Field	RESULT							
		Type	rh							
$D2_H$	**ADC_RESRA3L Reset: 00_H** Result Register 3, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
$D3_H$	**ADC_RESRA3H Reset: 00_H** Result Register 3, View A High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 4										
CA_H	**ADC_RCR0 Reset: 00_H** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw

3.2.4.8 Timer 2 Compare/Capture Unit Registers

The Timer 2 Compare/Capture Unit SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2CCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$C7_H$	**T2_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
$C0_H$	**T2_T2CON** **Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	$\underline{CP/RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T2_T2MOD** **Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw			rw
$C2_H$	**T2_RC2L** **Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T2_RC2H** **Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T2_T2L** **Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
$C5_H$	**T2_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							
$C6_H$	**T2_T2CON1** **Reset: 03_H** Timer 2 Control Register 1	Bit Field	0						TF2EN	EXF2EN
		Type	r						rw	rw
RMAP = 0, PAGE 1										
$C0_H$	**T2CCU_CCEN** **Reset: 00_H** T2CCU Capture/Compare Enable Register	Bit Field	CCM3		CCM2		CCM1		CCM0	
		Type	rw		rw		rw		rw	
$C1_H$	**T2CCU_CCTBSELReset: 00_H** T2CCU Capture/Compare Time Base Select Register	Bit Field	CASC	CCTTOV	CCTB5	CCTB4	CCTB3	CCTB2	CCTB1	CCTB0
		Type	rw	rwh	rw	rw	rw	rw	rw	rw
$C2_H$	**T2CCU_CCTRELLReset: 00_H** T2CCU Capture/Compare Timer Reload Register Low	Bit Field	CCTREL							
		Type	rw							
$C3_H$	**T2CCU_CCTRELHReset: 00_H** T2CCU Capture/Compare Timer Reload Register High	Bit Field	CCTREL							
		Type	rw							
$C4_H$	**T2CCU_CCTL** **Reset: 00_H** T2CCU Capture/Compare Timer Register Low	Bit Field	CCT							
		Type	rwh							

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 4										
$C2_H$	**T2CCU_CCTDTCLReset: 00_H** T2CCU Capture/Compare Timer Dead-Time Control Register Low	Bit Field	DTM							
		Type	rw							
$C3_H$	**T2CCU_CCTDTCHReset: 00_H** T2CCU Capture/Compare Timer Dead-Time Control Register High	Bit Field	DTRES	DTR2	DTR1	DTR0	DTLEV	DTE2	DTE1	DTE0
		Type	rwh	rh	rh	rh	rw	rw	rw	rw

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C0_H$	**T21_T2CON Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	$\overline{CP/RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T21_T2MOD Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C2_H$	**T21_RC2L Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T21_RC2H Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T21_T2L Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
$C5_H$	**T21_T2H Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							
$C6_H$	**T21_T2CON1 Reset: 03_H** Timer 2 Control Register 1	Bit Field	0						TF2EN	EXF2EN
		Type	r						rw	rw

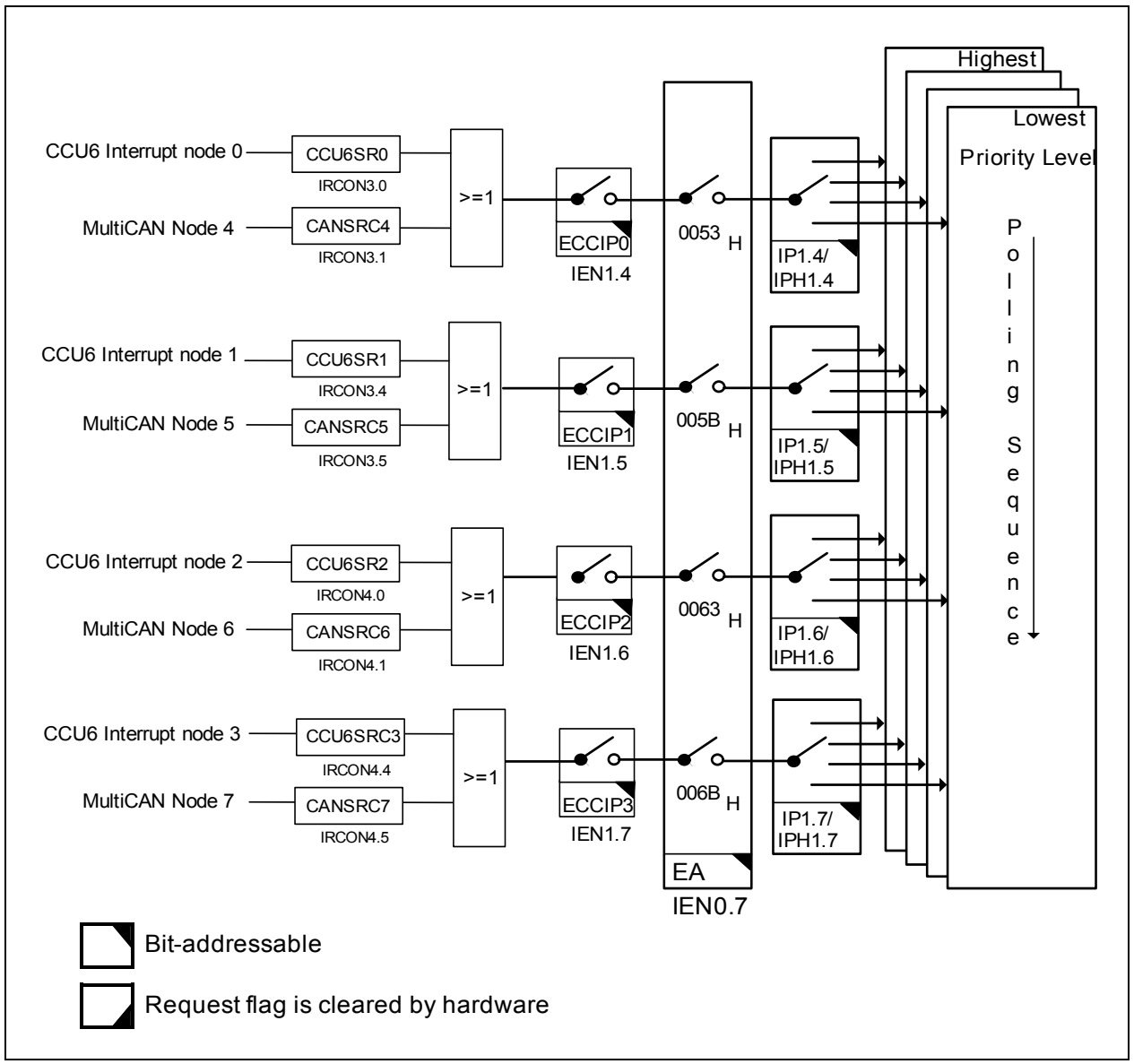

Figure 17 Interrupt Request Sources (Part 5)

Table 22 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
XINTR6	0033_H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	$004B_H$	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		T2CCU		
		MultiCAN Node 3		
XINTR10	0053_H	CCU6 INP0	ECCIP0	
		MultiCAN Node 4		
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063_H	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		

fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 26**.

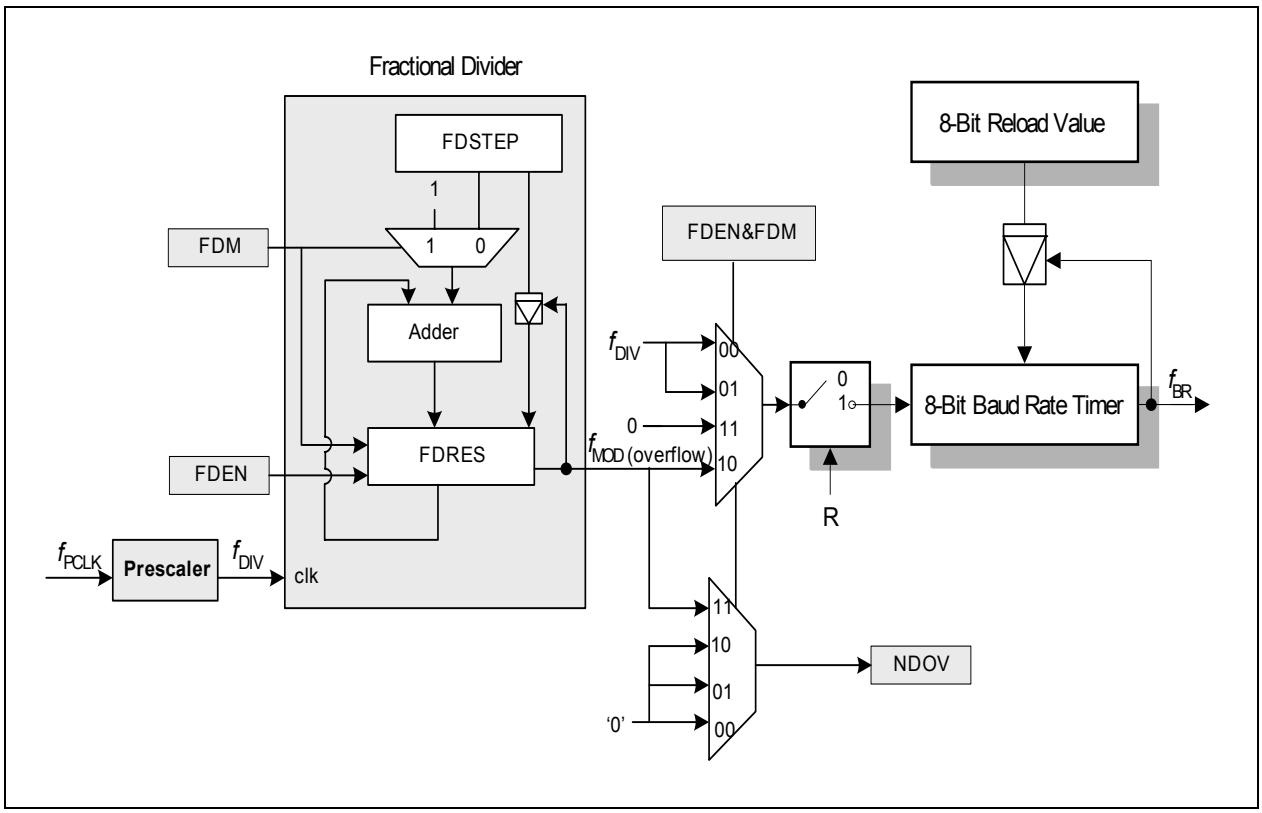

Figure 26 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

Table 37 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number
	AC-step
XC874CM-13FV 5V	$4B590402_H$
XC874LM-13FV 5V	$4B510422_H$
XC874-13FV 5V	$4B590462_H$

4.2.4 Power Supply Current

Table 43, **Table 44**, **Table 45** and **Table 46** provide the characteristics of the power supply current in the XC87x.

Table 43 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	37.5	45	mA	[3] SAF and SAX variants
		40.5	48	mA	[3] SAK variant
Idle Mode	I_{DDP}	29.2	35	mA	[4] SAF and SAX variants
		32.2	38	mA	[4] SAK variant
Active Mode with slow-down enabled	I_{DDP}	10	15	mA	[5] SAF and SAX variants
		13	18	mA	[5] SAK variant
Idle Mode with slow-down enabled	I_{DDP}	9.2	14	mA	[6] SAF and SAX variants
		12.2	17	mA	[6] SAK variant

1) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 105 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

Table 45 Power Supply Current Parameters[1] (Operating Conditions apply; V_{DDP} = 3.3V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[2]	max.[3]		
V_{DDP} = 3.3V Range					
Active Mode	I_{DDP}	35.4	43	mA	[4]
Idle Mode	I_{DDP}	27.6	33	mA	[5]
Active Mode with slow-down enabled	I_{DDP}	8.6	13	mA	[6]
Idle Mode with slow-down enabled	I_{DDP}	8	12	mA	[7]

1) The table is only applicable to SAF and SAX variants.

2) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at T_A = + 25 °C and V_{DDP} = 3.3 V.

3) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 105 °C and V_{DDP} = 3.6 V).

4) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

5) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

6) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

7) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

5 Package and Quality Declaration

Chapter 5 provides the information of the XC87x package and reliability section.

5.1 Package Parameters

Table 56 provides the thermal characteristics of the package used in XC878 and XC874.

Table 56 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
PG-LQFP-64-4 (XC878)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	34.6	K/W	-
PG-VQFN-48-22 (XC874)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	16.6	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	30.7	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.