Infineon Technologies - SAX-XC878-13FFA 5V AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sax-xc878-13ffa-5v-ac

Never stop thinking

8-Bit

XC87xCLM

8-Bit Single-Chip Microcontroller

Data Sheet

V1.5 2011-03

Microcontrollers

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - Loss-of-Clock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINT0[1)]
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Five ports
  - Up to 40 pins as digital I/O
  - 8 dedicated analog inputs used as A/D converter input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Two Capture/compare units
  - Capture/compare unit 6 for PWM signal generation (CCU6)
  - Timer 2 Capture/compare unit for vaious digital signal generation (T2CCU)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Packages:
  - PG-LQFP-64
  - PG-VQFN-48
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAX (-40 to 105 °C)
  - SAK (-40 to 125 °C)

1) SAK product variant does not support power-down mode.

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface. *Note: External Bus Interface is not available in XC874.*
P1.0	34/25		PU	RXD_0 UART Receive Data Input T2EX_0 Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input A8 Address Line 8 Output
P1.1	35/26		PU	EXINT3_0 External Interrupt Input 3 T0_1 Timer 0 Input TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output A9 Address Line 9 Output
P1.2	36/27		PU	SCK_0 SSC Clock Input/Output A10 Address Line 10 Output
P1.3	37/28		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input SCK_2 SSC Clock Input/Output TXDC1_3 MultiCAN Node 1 Transmitter Output A11 Address Line 11 Output
P1.4	38/29		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input MTSR_2 SSC Master Transmit Output/Slave Receive Input A12 Address Line 12 Output

Table 4 Flash Protection Modes (cont'd)

Flash Protection	Without hardware protection	With hardware protection	
P-Flash program and erase	Possible	Possible only on the condition that MSB - 1 of password is set to 1	Possible only on the condition that MSB - 1 of password is set to 1
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
External access to D-Flash	Not possible	Not possible	Not possible
D-Flash program	Possible	Possible	Possible, on the condition that MSB - 1 of password is set to 1
D-Flash erase	Possible	Possible, on these conditions: • MISC_CON.DFLASHEN bit is set to 1 prior to each erase operation; or • the MSB - 1 of password is set to 1	Possible, on the condition that MSB - 1 of password is set to 1

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. To disable the flash protection, a password match is required. A password match triggers an automatic erase of the protected P-Flash and D-Flash contents, including the programmed password. With a valid password, the Flash hardware protection is then enabled or disabled upon next reset. For the other protection strategies, no reset is necessary.

Although no protection scheme can be considered infallible, the XC87x memory protection strategy provides a very high level of protection for a general purpose microcontroller.

Note: If ROM read-out protection is enabled, only read instructions in the ROM memory can target the ROM contents.

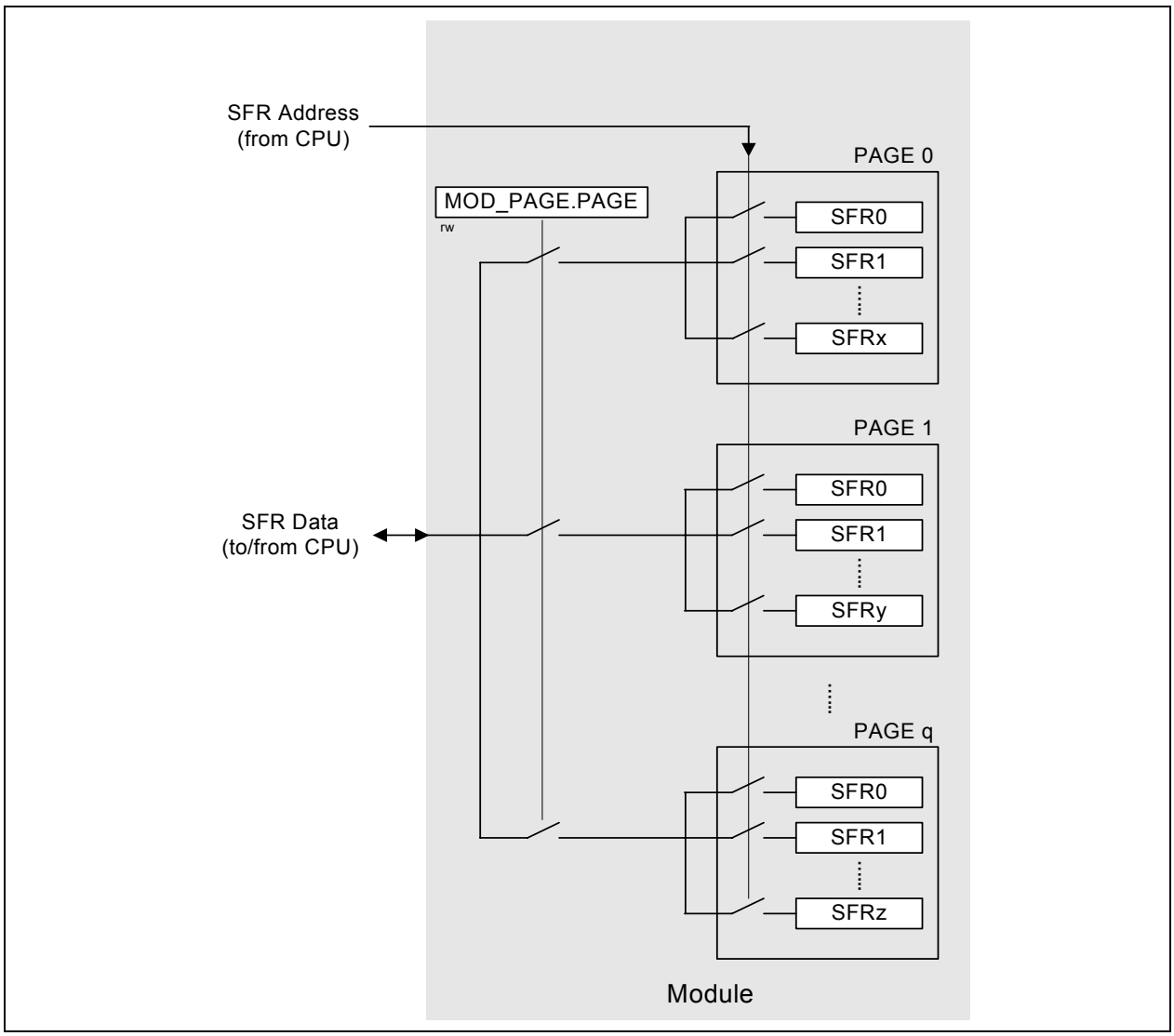


Figure 10 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or

Table 6 MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B1_H$	**MDUCON** **Reset: 00_H** MDU Control Register	Bit Field	IE	IR	RSEL	START	OPCODE			
		Type	rw	rw	rw	rwh	rw			
$B2_H$	**MD0** **Reset: 00_H** MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
$B2_H$	**MR0** **Reset: 00_H** MDU Result Register 0	Bit Field	DATA							
		Type	rh							
$B3_H$	**MD1** **Reset: 00_H** MDU Operand Register 1	Bit Field	DATA							
		Type	rw							
$B3_H$	**MR1** **Reset: 00_H** MDU Result Register 1	Bit Field	DATA							
		Type	rh							
$B4_H$	**MD2** **Reset: 00_H** MDU Operand Register 2	Bit Field	DATA							
		Type	rw							
$B4_H$	**MR2** **Reset: 00_H** MDU Result Register 2	Bit Field	DATA							
		Type	rh							
$B5_H$	**MD3** **Reset: 00_H** MDU Operand Register 3	Bit Field	DATA							
		Type	rw							
$B5_H$	**MR3** **Reset: 00_H** MDU Result Register 3	Bit Field	DATA							
		Type	rh							
$B6_H$	**MD4** **Reset: 00_H** MDU Operand Register 4	Bit Field	DATA							
		Type	rw							
$B6_H$	**MR4** **Reset: 00_H** MDU Result Register 4	Bit Field	DATA							
		Type	rh							
$B7_H$	**MD5** **Reset: 00_H** MDU Operand Register 5	Bit Field	DATA							
		Type	rw							
$B7_H$	**MR5** **Reset: 00_H** MDU Result Register 5	Bit Field	DATA							
		Type	rh							

3.2.4.3 CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7 CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$9A_H$	**CD_CORDXL** **Reset: 00_H** CORDIC X Data Low Byte	Bit Field	DATAL							
		Type	rw							
$9B_H$	**CD_CORDXH** **Reset: 00_H** CORDIC X Data High Byte	Bit Field	DATAH							
		Type	rw							

Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_DATA** **Reset: 00_H** P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$C9_H$	**P4_DIR** **Reset: 00_H** P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 1										
80_H	**P0_PUDSEL** **Reset: FF_H** P0 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_PUDEN** **Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_PUDSEL** **Reset: FF_H** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_PUDEN** **Reset: FF_H** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_PUDSEL** **Reset: FF_H** P5 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_PUDEN** **Reset: FF_H** P5 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_PUDSEL** **Reset: BF_H** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_PUDEN** **Reset: 40_H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_PUDSEL** **Reset: FF_H** P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_PUDEN** **Reset: 04_H** P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80_H	**P0_ALTSEL0** **Reset: 00_H** P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_ALTSEL1** **Reset: 00_H** P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_ALTSEL0** **Reset: 00_H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T2CCU_CCTH Reset: 00_H** T2CCU Capture/Compare Timer Register High	Bit Field	CCT							
		Type	rwh							
$C6_H$	**T2CCU_CCTCON Reset: 00_H** T2CCU CaptureCcompare Timer Control Register	Bit Field	CCTPRE				CCTOVF	CCTOVEN	TIMSYN	CCTST
		Type	rw				rwh	rw	rw	rw
RMAP = 0, PAGE 2										
$C0_H$	**T2CCU_COSHDWReset: 00_H** T2CCU Capture/compare Enable Register	Bit Field	ENSHDW	TXOV	COOUT5	COOUT4	COOUT3	COOUT2	COOUT1	COOUT0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$C1_H$	**T2CCU_CC0L Reset: 00_H** T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC0H Reset: 00_H** T2CCU Capture/compare Register 0 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC1L Reset: 00_H** T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC1H Reset: 00_H** T2CCU Capture/compare Register 1 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC2L Reset: 00_H** T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC2H Reset: 00_H** T2CCU Capture/compare Register 2 High	Bit Field	CCVALH							
		Type	rwh							
RMAP = 0, PAGE 3										
$C0_H$	**T2CCU_COCON Reset: 00_H** T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD	
		Type	rw	rw	rwh	rwh	rw	rw	rw	
$C1_H$	**T2CCU_CC3L Reset: 00_H** T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC3H Reset: 00_H** T2CCU Capture/compare Register 3 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC4L Reset: 00_H** T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC4H Reset: 00_H** T2CCU Capture/compare Register 4 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC5L Reset: 00_H** T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC5H Reset: 00_H** T2CCU Capture/compare Register 5 High	Bit Field	CCVALH							
		Type	rwh							

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD_H	**CCU6_CC61RH Reset: 00_H** Capture/Compare Register for Channel CC61 High	Bit Field	CC61VH							
		Type	rh							
FE_H	**CCU6_CC62RL Reset: 00_H** Capture/Compare Register for Channel CC62 Low	Bit Field	CC62VL							
		Type	rh							
FF_H	**CCU6_CC62RH Reset: 00_H** Capture/Compare Register for Channel CC62 High	Bit Field	CC62VH							
		Type	rh							
RMAP = 0, PAGE 2										
$9A_H$	**CCU6_T12MSELL Reset: 00_H** T12 Capture/Compare Mode Select Register Low	Bit Field	MSEL61				MSEL60			
		Type	rw				rw			
$9B_H$	**CCU6_T12MSELH Reset: 00_H** T12 Capture/Compare Mode Select Register High	Bit Field	DBYP	HSYNC			MSEL62			
		Type	rw	rw			rw			
$9C_H$	**CCU6_IENL Reset: 00_H** Capture/Compare Interrupt Enable Register Low	Bit Field	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$9D_H$	**CCU6_IENH Reset: 00_H** Capture/Compare Interrupt Enable Register High	Bit Field	ENSTR	ENIDLE	ENWHE	ENCHE	0	ENTRPF	ENT13PM	ENT13CM
		Type	rw	rw	rw	rw	r	rw	rw	rw
$9E_H$	**CCU6_INPL Reset: 40_H** Capture/Compare Interrupt Node Pointer Register Low	Bit Field	INPCHE		INPCC62		INPCC61		INPCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_INPH Reset: 39_H** Capture/Compare Interrupt Node Pointer Register High	Bit Field	0		INPT13		INPT12		INPERR	
		Type	r		rw		rw		rw	
$A4_H$	**CCU6_ISSL Reset: 00_H** Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12PM	ST12OM	SCC62F	SCC62R	SCC61F	SCC61R	SCC60F	SCC60R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISSH Reset: 00_H** Capture/Compare Interrupt Status Set Register High	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWHC	STRPF	ST13PM	ST13CM
		Type	w	w	w	w	w	w	w	w
$A6_H$	**CCU6_PSLR Reset: 00_H** Passive State Level Register	Bit Field	PSL63	0	PSL					
		Type	rwh	r	rwh					
$A7_H$	**CCU6_MCMCTR Reset: 00_H** Multi-Channel Mode Control Register	Bit Field	0		SWSYN		0	SWSEL		
		Type	r		rw		r	rw		
FA_H	**CCU6_TCTR2L Reset: 00_H** Timer Control Register 2 Low	Bit Field	0	T13TED		T13TEC			T13SSC	T12SSC
		Type	r	rw		rw			rw	rw
FB_H	**CCU6_TCTR2H Reset: 00_H** Timer Control Register 2 High	Bit Field	0				T13RSEL		T12RSEL	
		Type	r				rw		rw	
FC_H	**CCU6_MODCTRL Reset: 00_H** Modulation Control Register Low	Bit Field	MCMEN	0	T12MODEN					
		Type	rw	r	rw					

Table 22 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
XINTR6	0033_H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	$004B_H$	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		T2CCU		
		MultiCAN Node 3		
XINTR10	0053_H	CCU6 INP0	ECCIP0	
		MultiCAN Node 4		
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063_H	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		

3.6 Power Supply System with Embedded Voltage Regulator

The XC87x microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 19 shows the XC87x power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode[1)], the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

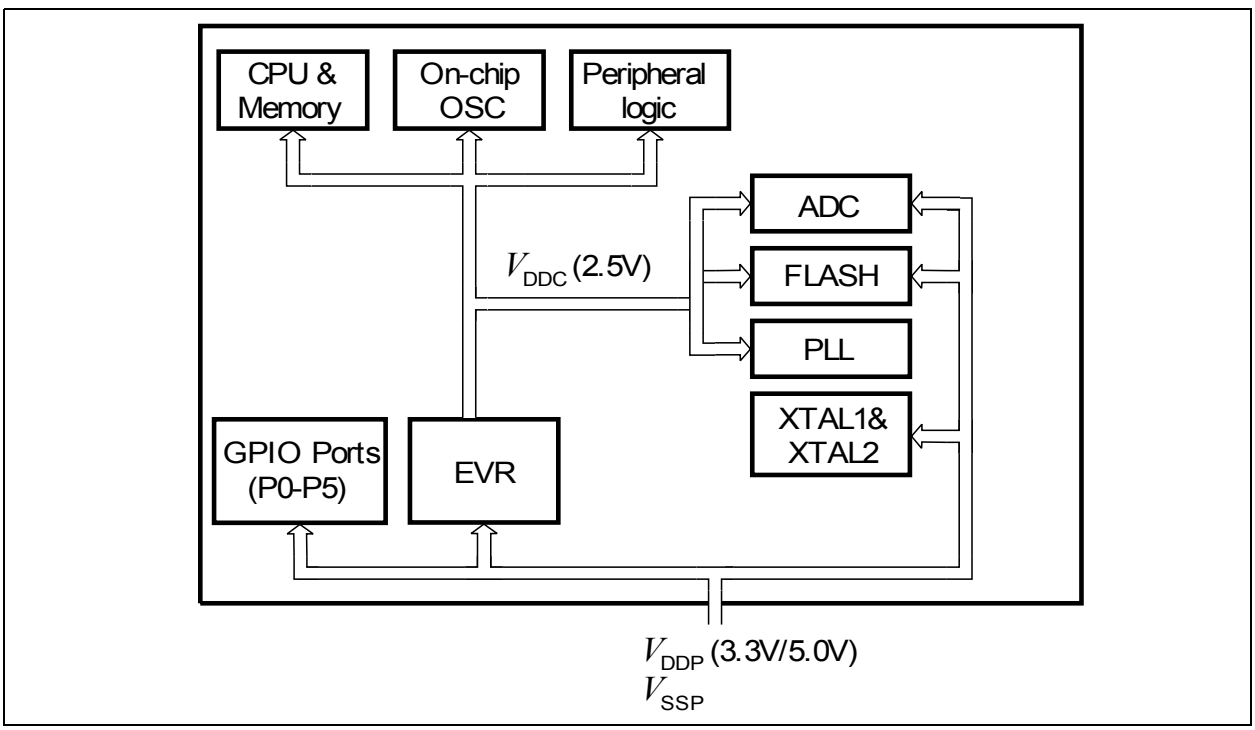


Figure 19 XC87x Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode[1)]
- V_{DDP} prewarning detection
- V_{DDC} brownout detection

1) SAK product variant does not support power-down mode.

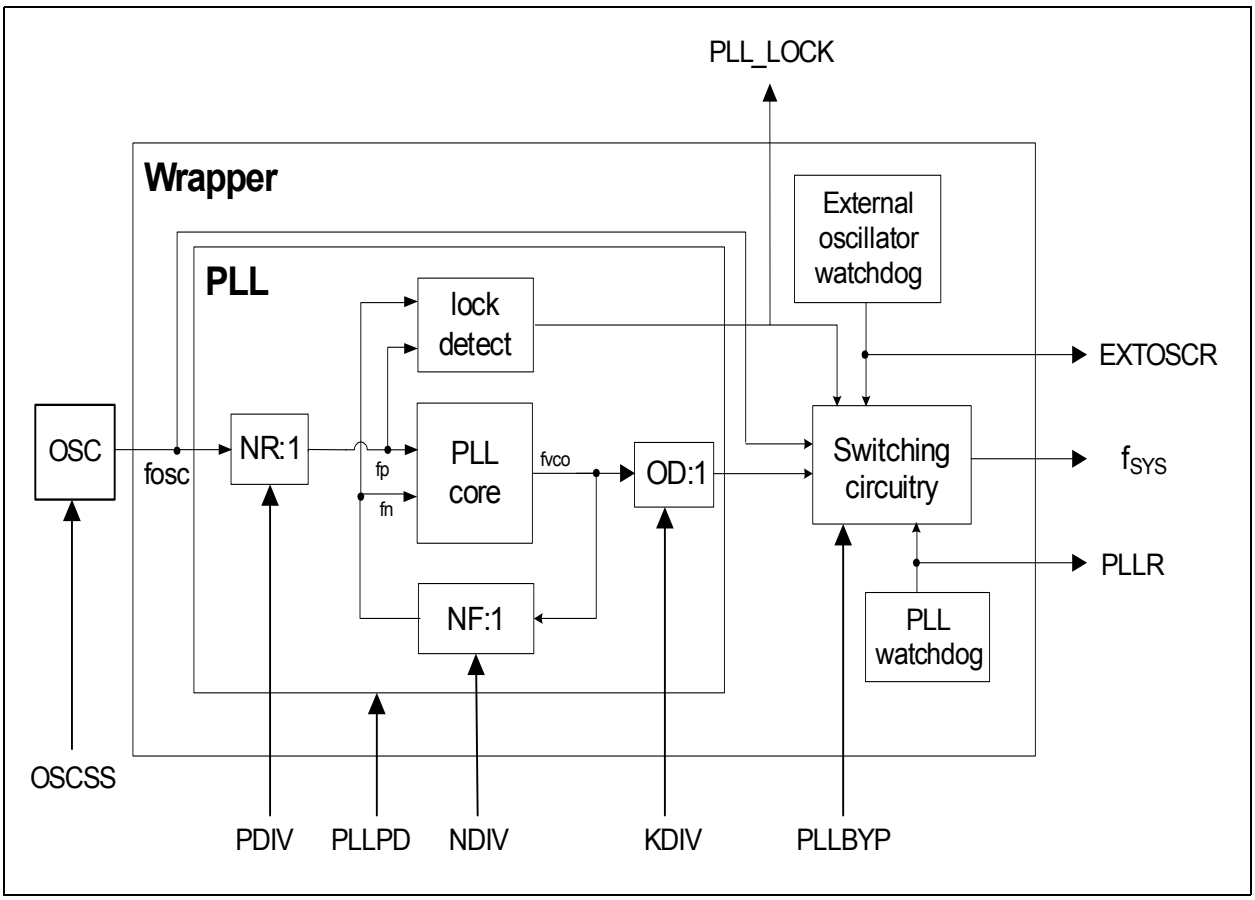


Figure 20 CGU Block Diagram

Direct Drive (PLL Bypass Operation)

During PLL bypass operation, the system clock has the same frequency as the external clock source.

(3.1)

$$f_{SYS} = f_{OSC}$$

PLL Mode

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must

Table 32 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
24 MHz	1	6 (6_H)	59 ($3B_H$)	+0.03 %
12 MHz	1	3 (3_H)	59 ($3B_H$)	+0.03 %
8 MHz	1	2 (2_H)	59 ($3B_H$)	+0.03 %
6 MHz	1	6 (6_H)	236 (EC_H)	+0.03 %

3.13.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)} \tag{3.6}$$

3.14 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 26**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV}, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP} \tag{3.7}$$

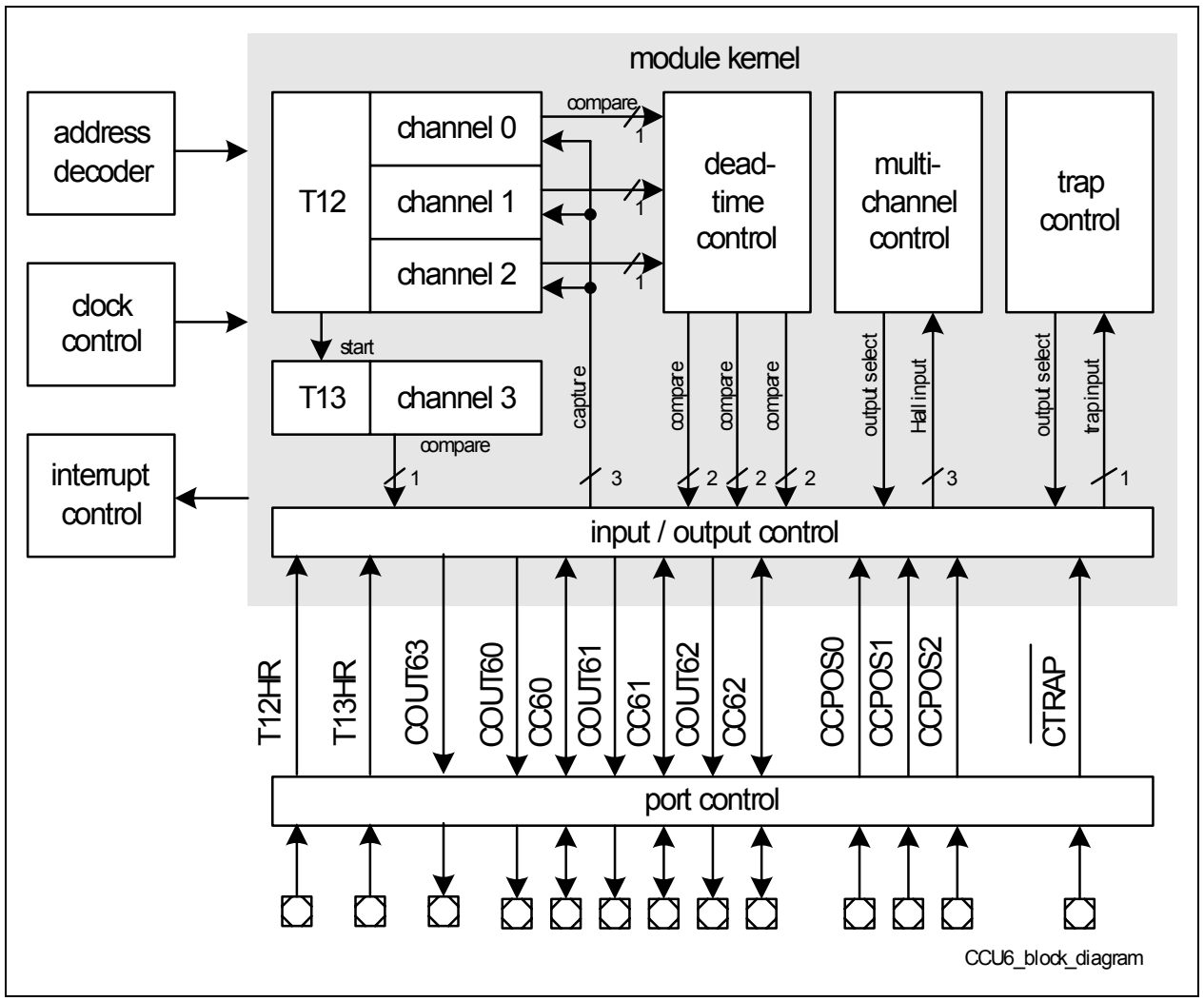


Figure 29 CCU6 Block Diagram

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

3.23 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

Features

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in **Figure 33**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG[1)], which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC87x has been started in OCDS mode.

1) The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).
User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

4.3.4 On-Chip Oscillator Characteristics

Table 49 provides the characteristics of the on-chip oscillator in the XC87x.

Table 49 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM}	CC	3.88	4	4.12	MHz	under nominal conditions[1] after IFX-backend trimming
Long term frequency deviation	Δf_{LT}	CC	-5	–	5	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to 105°C), for one given device after trimming
Short term frequency deviation	Δf_{ST}	CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

4.3.5 External Data Memory Characteristics

Table 50 shows the timing of the external data memory read cycle.

Table 50 External Data Memory Read Timing[1] (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
$\overline{RD}$ pulse width	t_1	CC	$2*f_{CCLK}$ - 17	-	ns	2)
Address valid to $\overline{RD}$	t_2	CC	f_{CCLK} - 12	-	ns	2)
$\overline{RD}$ to valid data in	t_3	SR	-	$1.5*f_{CCLK}$ - 27	ns	2)
Address to valid data in	t_4	SR	-	$3*f_{CCLK}$ - 7	ns	2)
Data hold after $\overline{RD}$	t_5	SR	$0.5*f_{CCLK}$ -17	-	ns	2)

1) External Bus Interface is not available in XC874.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

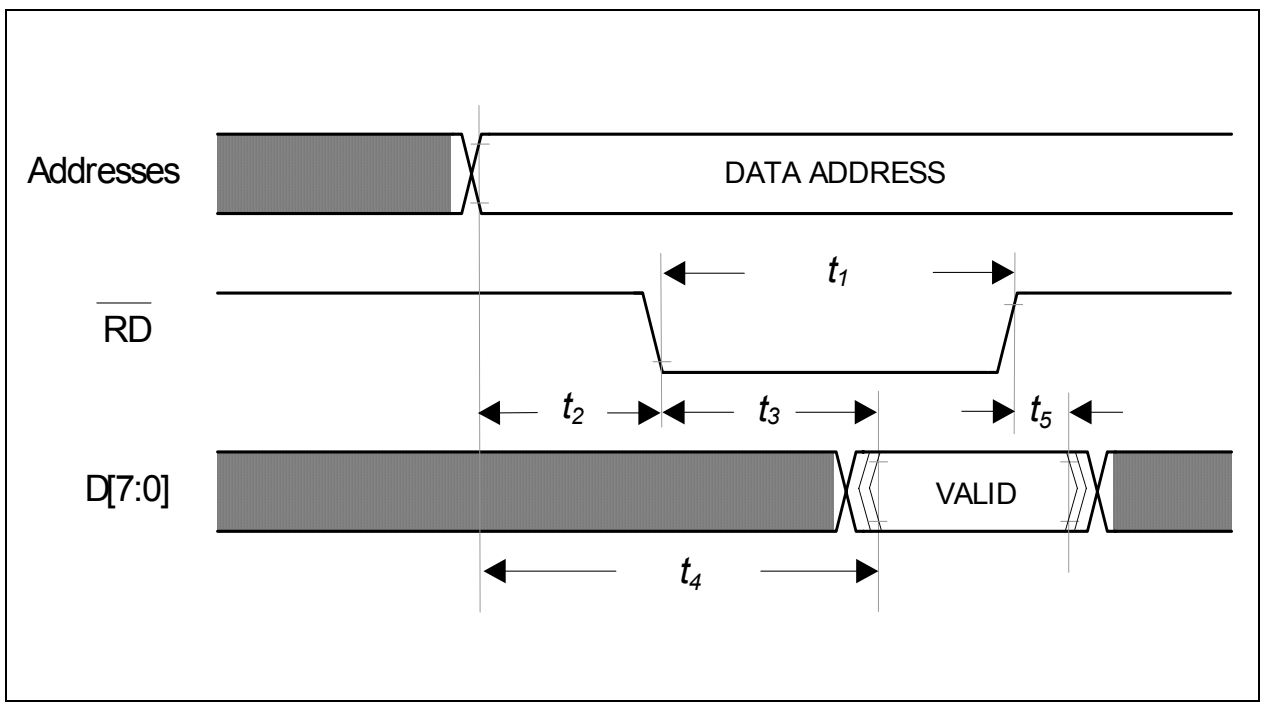
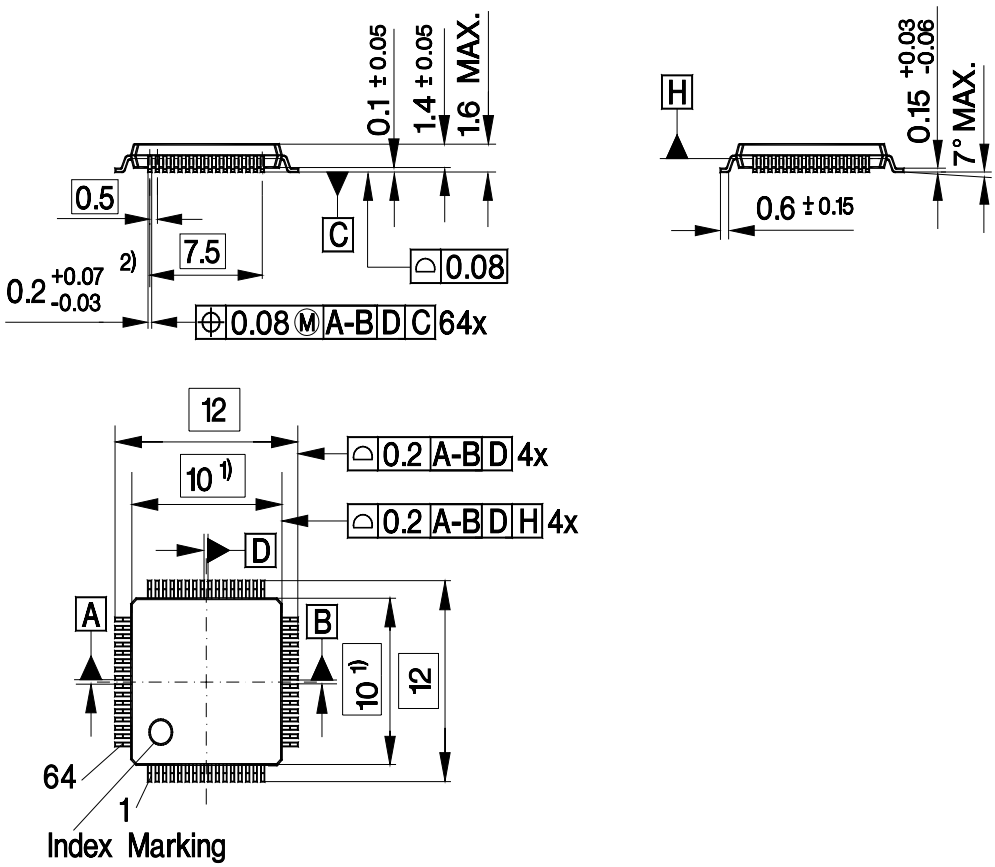


Figure 41 External Data Memory Read Cycle

5.2 Package Outline

Figure 47 shows the package outlines of the XC878.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Figure 47 PG-LQFP-64-4 Package Outline

5.3 Quality Declaration

Table 57 shows the characteristics of the quality parameters in the XC87x.

Table 57 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the two stated T_J 1)	t_{OP1}	-	15000	hours	T_J = 110°C
		-	2000	hours	T_J = -40°C
Operation Lifetime when the device is used at the five stated T_J 1)	t_{OP2}	-	120	hours	T_J = 140°C
		-	960	hours	T_J = 135°C
		-	7800	hours	T_J = 91°C
		-	2400	hours	T_J = 38°C
		-	720	hours	T_J = -25°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	750	V	Conforming to JESD22-C101-C

1) This lifetime refers only to the time when device is powered-on.