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Details

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sax-xc878-16ffa-5v-ac

XC87x Data Sheet**Revision History: V1.5 2011-03**

Previous Versions: V1.4

Page	Subjects (major changes since last revision)
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Changes from V1.4 2010-08 to V1.5 2011-03

Page 3	A new variant, SAF-XC874CM-13FVA 5V, has been added in Table 2.
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Any information within this document that you feel is wrong, unclear or missing at all?
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2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC87x.

2.1 Block Diagram

The block diagram of the XC87x is shown in **Figure 2**.

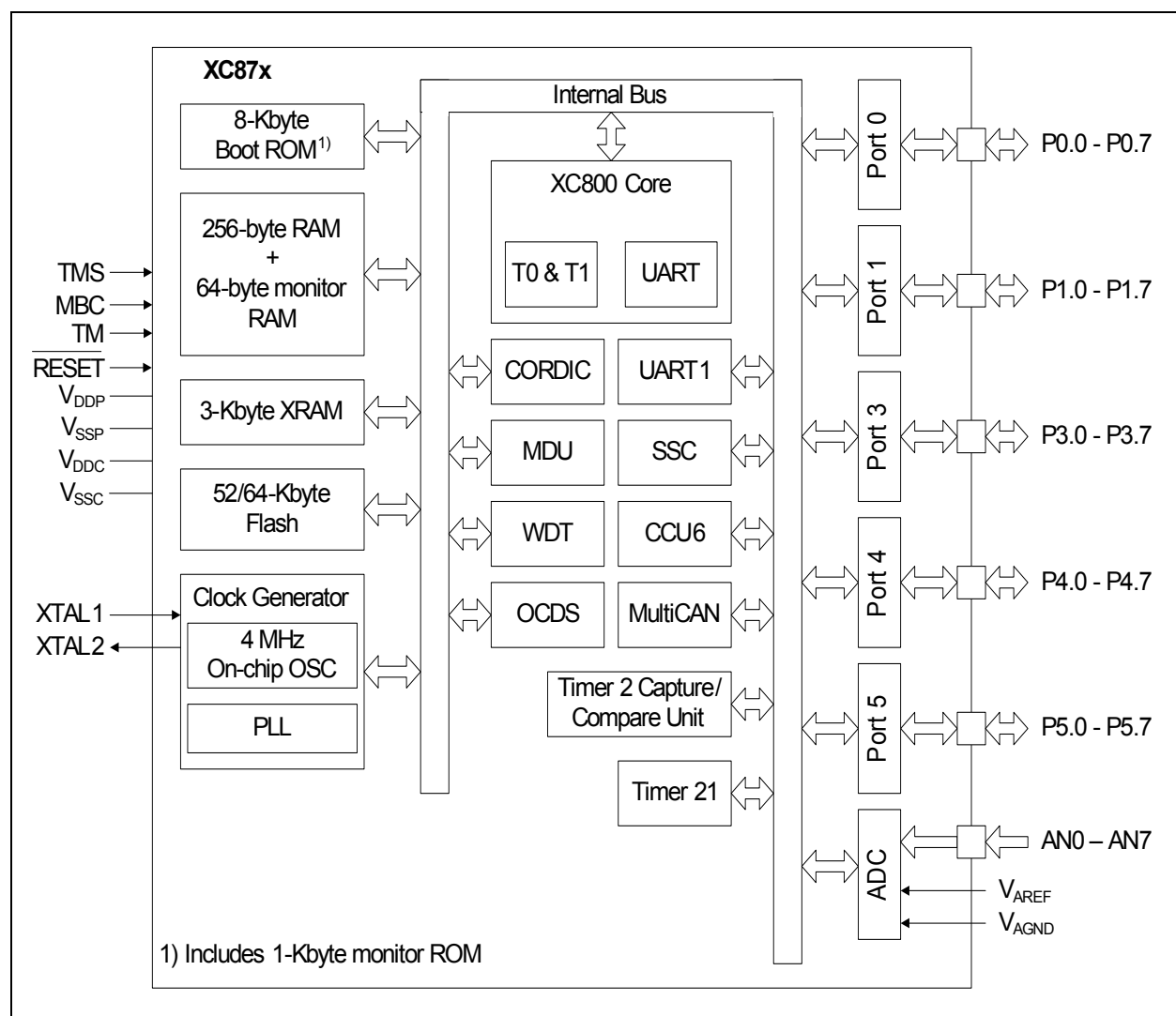


Figure 2 XC87x Block Diagram

General Device Information

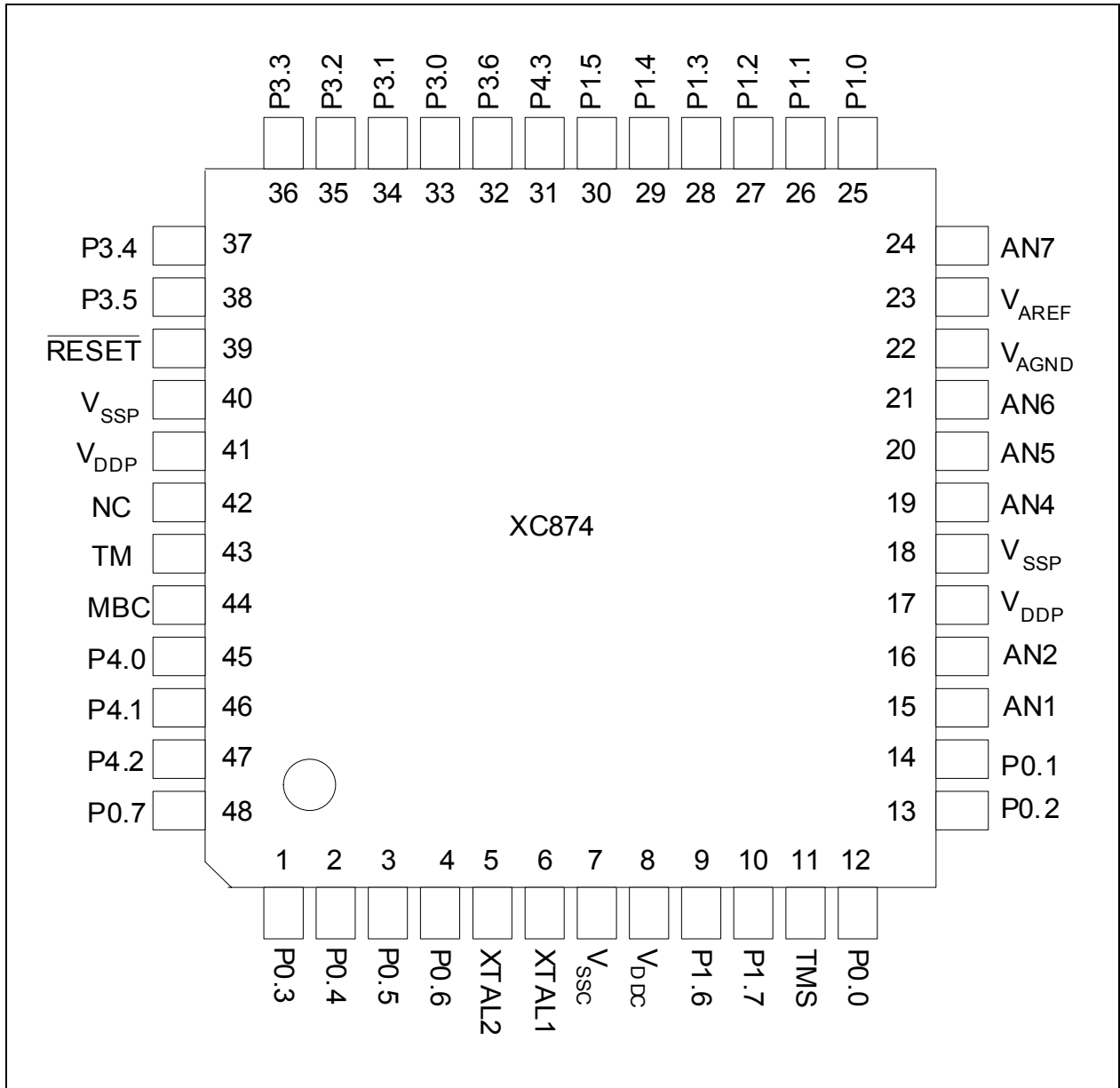


Figure 5 XC874 Pin Configuration, PG-VQFN-48 Package (top view)

Functional Description

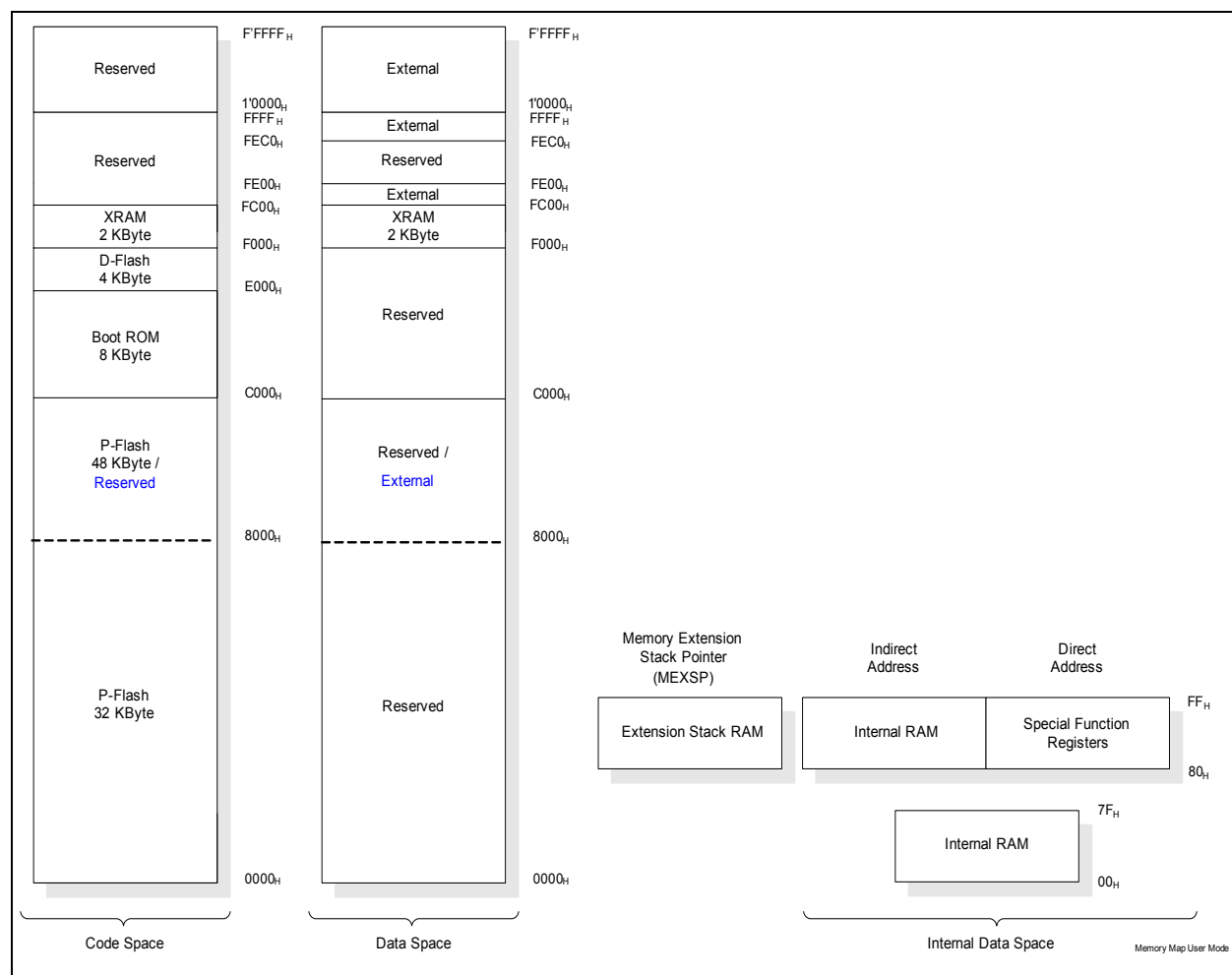


Figure 8 Memory Map of XC87x with 52K Flash Memory in user mode

Functional Description

SYSCON0

System Control Register 0

Reset Value: 04_H

7	6	5	4	3	2	1	0
0			IMODE	0	1	0	RMAP
r			rw	r	r	r	rw

Field	Bits	Type	Description
RMAP	0	rw	Interrupt Node XINTR0 Enable 0 The access to the standard SFR area is enabled 1 The access to the mapped SFR area is enabled
1	2	r	Reserved Returns 1 if read; should be written with 1.
0	[7:5], 3,1	r	Reserved Returns 0 if read; should be written with 0.

Note: The RMAP bit should be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC87x has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in [Figure 10](#).

Functional Description

Table 6 MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B1 _H	MDUCON Reset: 00_H MDU Control Register	Bit Field	IE	IR	RSEL	STAR T	OPCODE			
		Type	rw	rw	rw	rwh	rw			
B2 _H	MD0 Reset: 00_H MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
B2 _H	MR0 Reset: 00_H MDU Result Register 0	Bit Field	DATA							
		Type	rh							
B3 _H	MD1 Reset: 00_H MDU Operand Register 1	Bit Field	DATA							
		Type	rw							
B3 _H	MR1 Reset: 00_H MDU Result Register 1	Bit Field	DATA							
		Type	rh							
B4 _H	MD2 Reset: 00_H MDU Operand Register 2	Bit Field	DATA							
		Type	rw							
B4 _H	MR2 Reset: 00_H MDU Result Register 2	Bit Field	DATA							
		Type	rh							
B5 _H	MD3 Reset: 00_H MDU Operand Register 3	Bit Field	DATA							
		Type	rw							
B5 _H	MR3 Reset: 00_H MDU Result Register 3	Bit Field	DATA							
		Type	rh							
B6 _H	MD4 Reset: 00_H MDU Operand Register 4	Bit Field	DATA							
		Type	rw							
B6 _H	MR4 Reset: 00_H MDU Result Register 4	Bit Field	DATA							
		Type	rh							
B7 _H	MD5 Reset: 00_H MDU Operand Register 5	Bit Field	DATA							
		Type	rw							
B7 _H	MR5 Reset: 00_H MDU Result Register 5	Bit Field	DATA							
		Type	rh							

3.2.4.3 CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7 CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
9A _H	CD_CORDXL Reset: 00 _H CORDIC X Data Low Byte	Bit Field	DATAL							
		Type	rw							
9B _H	CD_CORDXH Reset: 00 _H CORDIC X Data High Byte	Bit Field	DATAH							
		Type	rw							

Functional Description
Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CB _H	ADC_RCR1 Reset: 00_H Result Control Register 1	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CC _H	ADC_RCR2 Reset: 00_H Result Control Register 2	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CD _H	ADC_RCR3 Reset: 00_H Result Control Register 3	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CE _H	ADC_VFCR Reset: 00_H Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA _H	ADC_CHINFR Reset: 00_H Channel Interrupt Flag Register	Bit Field	CHINF 7	CHINF 6	CHINF 5	CHINF 4	CHINF 3	CHINF 2	CHINF 1	CHINF 0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB _H	ADC_CHINCR Reset: 00_H Channel Interrupt Clear Register	Bit Field	CHINC 7	CHINC 6	CHINC 5	CHINC 4	CHINC 3	CHINC 2	CHINC 1	CHINC 0
		Type	w	w	w	w	w	w	w	w
CC _H	ADC_CHINSR Reset: 00_H Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w
CD _H	ADC_CHINPR Reset: 00_H Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE _H	ADC_EVINFR Reset: 00_H Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF _H	ADC_EVINCR Reset: 00_H Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
D2 _H	ADC_EVINSR Reset: 00_H Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
D3 _H	ADC_EVINPR Reset: 00_H Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA _H	ADC_CRCR1 Reset: 00_H Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB _H	ADC_CRPR1 Reset: 00_H Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			

Functional Description
Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CC _H	ADC_CRMR1 Reset: 00_H Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD _H	ADC_QMR0 Reset: 00_H Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE _H	ADC_QSR0 Reset: 20_H Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF _H	ADC_Q0R0 Reset: 00_H Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QBUR0 Reset: 00_H Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QINR0 Reset: 00_H Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Functional Description
Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FC _H	CCU6_CC61SRL Reset: 00_H Capture/Compare Shadow Register for Channel CC61 Low	Bit Field	CC61SL							
		Type	rwh							
FD _H	CCU6_CC61SRH Reset: 00_H Capture/Compare Shadow Register for Channel CC61 High	Bit Field	CC61SH							
		Type	rwh							
FE _H	CCU6_CC62SRL Reset: 00_H Capture/Compare Shadow Register for Channel CC62 Low	Bit Field	CC62SL							
		Type	rwh							
FF _H	CCU6_CC62SRH Reset: 00_H Capture/Compare Shadow Register for Channel CC62 High	Bit Field	CC62SH							
		Type	rwh							
RMAP = 0, PAGE 1										
9A _H	CCU6_CC63RL Reset: 00_H Capture/Compare Register for Channel CC63 Low	Bit Field	CC63VL							
		Type	rh							
9B _H	CCU6_CC63RH Reset: 00_H Capture/Compare Register for Channel CC63 High	Bit Field	CC63VH							
		Type	rh							
9C _H	CCU6_T12PRL Reset: 00_H Timer T12 Period Register Low	Bit Field	T12PVL							
		Type	rwh							
9D _H	CCU6_T12PRH Reset: 00_H Timer T12 Period Register High	Bit Field	T12PVH							
		Type	rwh							
9E _H	CCU6_T13PRL Reset: 00_H Timer T13 Period Register Low	Bit Field	T13PVL							
		Type	rwh							
9F _H	CCU6_T13PRH Reset: 00_H Timer T13 Period Register High	Bit Field	T13PVH							
		Type	rwh							
A4 _H	CCU6_T12DTCL Reset: 00_H Dead-Time Control Register for Timer T12 Low	Bit Field	DTM							
		Type	rw							
A5 _H	CCU6_T12DTCH Reset: 00_H Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0
		Type	r	rh	rh	rh	r	rw	rw	rw
A6 _H	CCU6_TCTR0L Reset: 00_H Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE1 2	T12R	T12 PRE	T12CLK		
		Type	rw	rh	rh	rh	rw	rw		
A7 _H	CCU6_TCTR0H Reset: 00_H Timer Control Register 0 High	Bit Field	0		STE1 3	T13R	T13 PRE	T13CLK		
		Type	r		rh	rh	rw	rw		
FA _H	CCU6_CC60RL Reset: 00_H Capture/Compare Register for Channel CC60 Low	Bit Field	CC60VL							
		Type	rh							
FB _H	CCU6_CC60RH Reset: 00_H Capture/Compare Register for Channel CC60 High	Bit Field	CC60VH							
		Type	rh							
FC _H	CCU6_CC61RL Reset: 00_H Capture/Compare Register for Channel CC61 Low	Bit Field	CC61VL							
		Type	rh							

Functional Description

3.2.4.15 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 19 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
D1 _H	FCON Reset: 10_H P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D2 _H	EECON Reset: 10_H D-Flash Control Register	Bit Field	0	EEBS Y	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D3 _H	FCS Reset: 80_H Flash Control and Status Register	Bit Field	1	SBEIE	FTEN	0	EEDE RR	EESE RR	FDER R	FSER R
		Type	r	rw	rwh	r	rwh	rwh	rwh	rwh
D4 _H	FEAL Reset: 00_H Flash Error Address Register, Low Byte	Bit Field	ECCEADDR							
		Type	rh							
D5 _H	FEAH Reset: 00_H Flash Error Address Register, High Byte	Bit Field	ECCEADDR							
		Type	rh							
D6 _H	FTVAL Reset: 78_H Flash Timer Value Register	Bit Field	MODE	OFVAL						
		Type	rw	rw						
DD _H	FCS1 Reset: 00_H Flash Control and Status Register 1	Bit Field	0							EEAB ORT
		Type	r							rwh

Functional Description

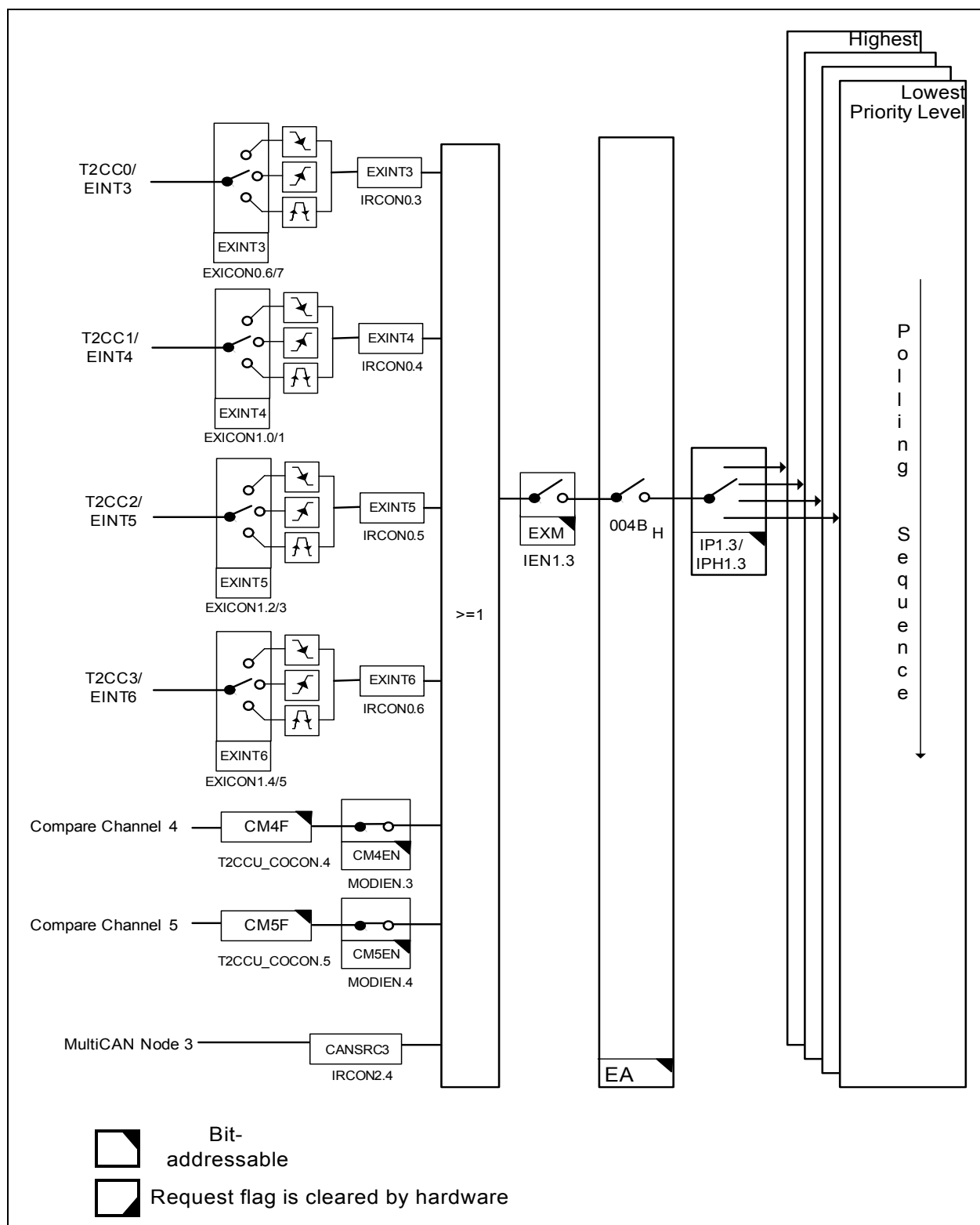


Figure 16 Interrupt Request Sources (Part 4)

Functional Description

3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC87x interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in [Table 22](#).

Table 22 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
NMI	0073 _H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash Timer NMI	NMIFLASH	
		V _{DDP} Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 _H	External Interrupt 0	EX0	IEN0
XINTR1	000B _H	Timer 0	ET0	
XINTR2	0013 _H	External Interrupt 1	EX1	
XINTR3	001B _H	Timer 1	ET1	
XINTR4	0023 _H	UART	ES	
XINTR5	002B _H	T2CCU	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		
		LIN		

Functional Description

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2⁸). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT} , between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}} \quad (3.3)$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see [Figure 25](#). This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.

3.12 CORDIC Coprocessor

The CORDIC Coprocessor provides CPU with hardware support for the solving of circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions.

Features

- Modes of operation
 - Supports all CORDIC operating modes for solving circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions
 - Integrated look-up tables (LUTs) for all operating modes
- Circular vectoring mode: Extended support for values of initial X and Y data up to full range of $[-2^{15}, (2^{15}-1)]$ for solving angle and magnitude
- Circular rotation mode: Extended support for values of initial Z data up to full range of $[-2^{15}, (2^{15}-1)]$, representing angles in the range $[-\pi, ((2^{15}-1)/2^{15})\pi]$ for solving trigonometry
- Implementation-dependent operational frequency of up to 80 MHz
- Gated clock input to support disabling of module
- 16-bit accessible data width
 - 24-bit kernel data width plus 2 overflow bits for X and Y each
 - 20-bit kernel data width plus 1 overflow bit for Z
 - With KEEP bit to retain the last value in the kernel register for a new calculation
- 16 iterations per calculation: Approximately 41 clock-cycles or less, from set of start (ST) bit to set of end-of-calculation flag, excluding time taken for write and read access of data bytes.
- Twos complement data processing
 - Only exception: X result data with user selectable option for unsigned result
- X and Y data generally accepted as integer or rational number; X and Y must be of the same data form
- Entries of LUTs are 20-bit signed integers
 - Entries of atan and atanh LUTs are integer representations (S19) of angles with the scaling such that $[-2^{15}, (2^{15}-1)]$ represents the range $[-\pi, ((2^{15}-1)/2^{15})\pi]$
 - Accessible Z result data for circular and hyperbolic functions is integer in data form of S15
- Emulated LUT for linear function
 - Data form is 1 integer bit and 15-bit fractional part (1.15)
 - Accessible Z result data for linear function is rational number with fixed data form of S4.11 (signed 4Q16)
- Truncation Error
 - The result of a CORDIC calculation may return an approximation due to truncation of LSBs
 - Good accuracy of the CORDIC calculated result data, especially in circular mode
- Interrupt
 - On completion of a calculation

3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits. The clock frequency of T2CCU, f_{T2CCU} , could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be 'reset' immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
 - Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
 - Active level can be defined by register bit for channel groups A and B.
 - Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

Electrical Parameters
4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC87x. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 39 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
CPU Clock Frequency ¹⁾	f_{CCLK}		26.67 ²⁾	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC878/874...
		-40	105	°C	SAX-XC878...
		-40	125	°C	SAK-XC878/874...

1) f_{CCLK} is the input frequency to the XC800 core. Please refer to [Figure 22](#) for detailed description.

2) Default setting of f_{CCLK} upon reset is 24 MHz.

Electrical Parameters
4.2.4 Power Supply Current

Table 43, **Table 44**, **Table 45** and **Table 46** provide the characteristics of the power supply current in the XC87x.

**Table 43 Power Supply Current Parameters (Operating Conditions apply;
 $V_{DDP} = 5V$ range)**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. ¹⁾	max. ²⁾		
$V_{DDP} = 5V$ Range					
Active Mode	I_{DDP}	37.5	45	mA	³⁾ SAF and SAX variants
		40.5	48	mA	³⁾ SAK variant
Idle Mode	I_{DDP}	29.2	35	mA	⁴⁾ SAF and SAX variants
		32.2	38	mA	⁴⁾ SAK variant
Active Mode with slow-down enabled	I_{DDP}	10	15	mA	⁵⁾ SAF and SAX variants
		13	18	mA	⁵⁾ SAK variant
Idle Mode with slow-down enabled	I_{DDP}	9.2	14	mA	⁶⁾ SAF and SAX variants
		12.2	17	mA	⁶⁾ SAK variant

- 1) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at $T_A = +25\text{ °C}$ and $V_{DDP} = 5.0\text{ V}$.
- 2) The maximum I_{DDP} values are measured under worst case conditions ($T_A = +105\text{ °C}$ and $V_{DDP} = 5.5\text{ V}$).
- 3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.
- 4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.
- 5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.
- 6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.

Electrical Parameters

Table 46 Power Down Current¹⁾(Operating Conditions apply; $V_{DDP} = 3.3V$ range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. ²⁾	max. ³⁾		
V_{DDP} = 3.3V Range					
Power-Down Mode	I_{PDP}	20	80	μA	T_A = + 25 °C ⁴⁾⁵⁾
		-	250	μA	T_A = + 85 °C ⁵⁾⁶⁾

1) The table is only applicable to SAF and SAX variants.

2) The typical I_{PDP} values are based on preliminary measurements and are to be used as reference only. These values are measured at $V_{DDP} = 3.3\text{ V}$.

3) The maximum I_{PDP} values are measured at $V_{DDP} = 3.6\text{ V}$.

4) I_{PDP} has a maximum value of $450\text{ }\mu A$ at $T_A = + 105\text{ }^{\circ}C$.

5) I_{PDP} is measured with: $\overline{RESET} = V_{DDP}$, $V_{AGND} = V_{SS}$, $RXD/INT0 = V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

6) Not subjected to production test, verified by design/characterization.