Infineon Technologies - SAX-XC878CM-13FFA 5V AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	CANbus, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sax-xc878cm-13ffa-5v-ac

Never stop thinking

8-Bit

XC87xCLM

8-Bit Single-Chip Microcontroller

Data Sheet

V1.5 2011-03

Microcontrollers

2.3 Pin Configuration

The pin configuration of the XC878, which is based on the PG-LQFP-64, is shown in **Figure 4**, while that of the XC874, which is based on the PG-VQFN-48 package, is shown in **Figure 5**.

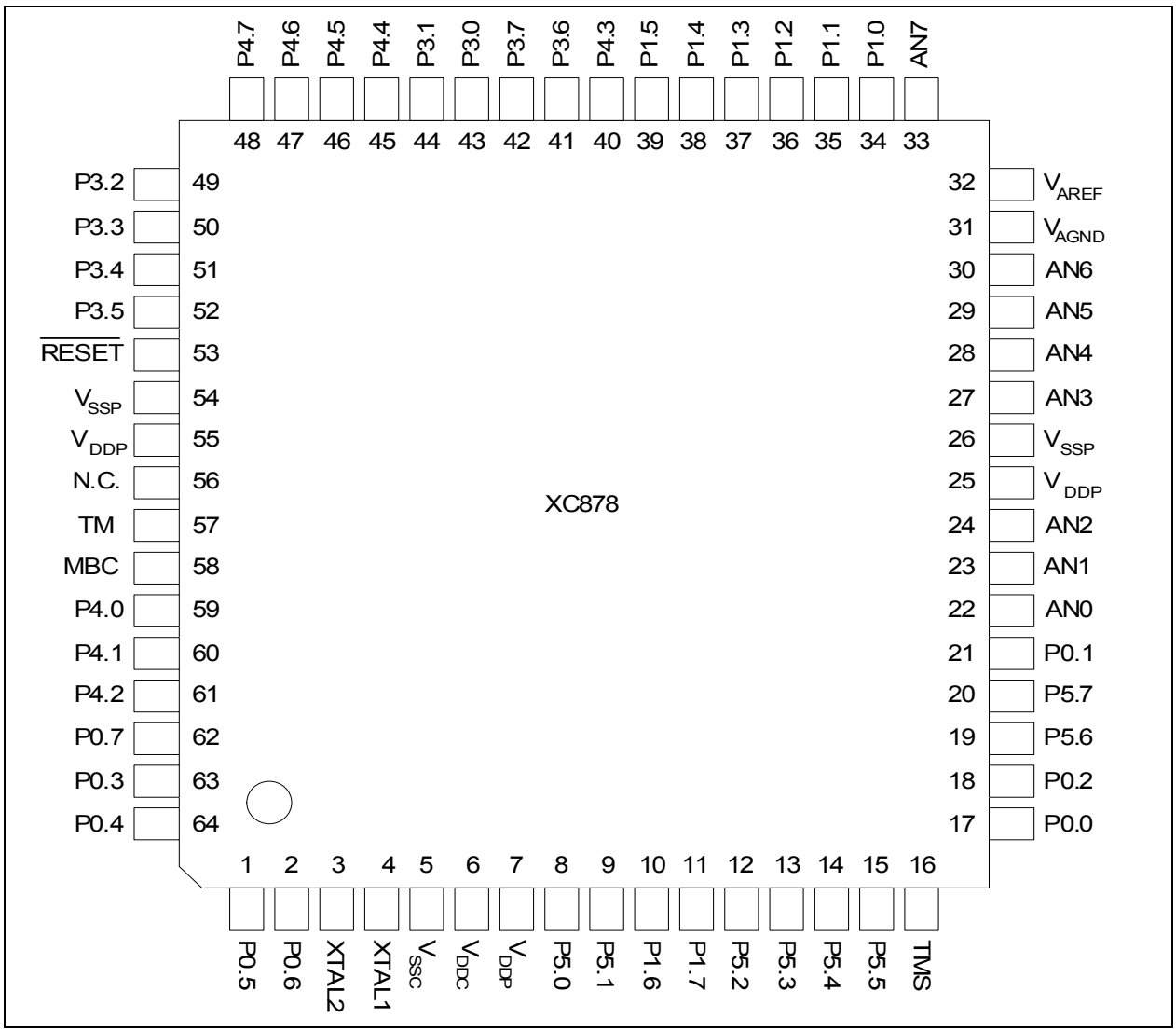


Figure 4 XC878 Pin Configuration, PG-LQFP-64 Package (top view)

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P4		I/O		**Port 4** Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Bus Interface. *Note: External Bus Interface is not available in XC874.*	
P4.0	59/45		Hi-Z	RXDC0_3 CC60_1 T2CC0_0/ EXINT3_1 D0	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0 External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Data Line 0 Input/Output
P4.1	60/46		Hi-Z	TXDC0_3 COUT60_1 T2CC1_0/ EXINT4_1 D1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0 External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Data Line 1 Input/Output
P4.2	61/47		PU	EXINT6_1 T21_0 D2	External Interrupt Input 6 Timer 21 Input Data Line 2 Input/Output
P4.3	40/31		Hi-Z	T2EX_1 EXF21_1 COUT63_2 D3	Timer 2 External Trigger Input Timer 21 External Flag Output Output of Capture/Compare channel 3 Data Line 3 Input/Output
P4.4	45/-		Hi-Z	CCPOS0_3 T0_0 CC61_4 T2CC2_0/ EXINT5_1 D4	CCU6 Hall Input 0 Timer 0 Input Output of Capture/Compare channel 1 External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Data Line 4 Input/Output

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

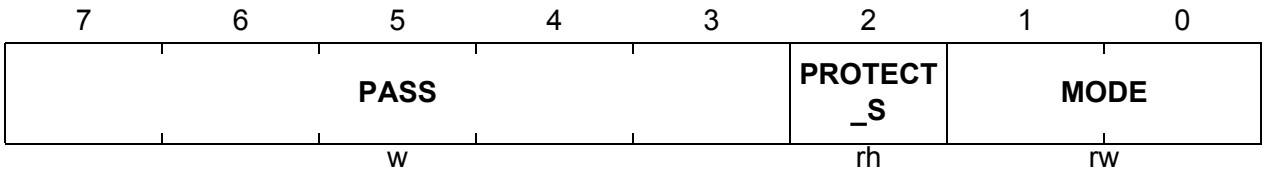
3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 9**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

3.2.3.1 Password Register

PASSWD
Password Register **Reset Value: 07_H**



Field	Bits	Type	Description
MODE	[1:0]	rw	**Bit Protection Scheme Control Bits** 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others:Scheme Enabled. These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	**Bit Protection Signal Status Bit** This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits.
PASS	[7:3]	w	**Password Bits** The Bit Protection Scheme only recognizes three patterns. 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits

3.2.4.8 Timer 2 Compare/Capture Unit Registers

The Timer 2 Compare/Capture Unit SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2CCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$C7_H$	**T2_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
$C0_H$	**T2_T2CON** **Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	$\underline{CP/RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T2_T2MOD** **Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw			rw
$C2_H$	**T2_RC2L** **Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T2_RC2H** **Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T2_T2L** **Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
$C5_H$	**T2_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							
$C6_H$	**T2_T2CON1** **Reset: 03_H** Timer 2 Control Register 1	Bit Field	0						TF2EN	EXF2EN
		Type	r						rw	rw
RMAP = 0, PAGE 1										
$C0_H$	**T2CCU_CCEN** **Reset: 00_H** T2CCU Capture/Compare Enable Register	Bit Field	CCM3		CCM2		CCM1		CCM0	
		Type	rw		rw		rw		rw	
$C1_H$	**T2CCU_CCTBSELReset: 00_H** T2CCU Capture/Compare Time Base Select Register	Bit Field	CASC	CCTTOV	CCTB5	CCTB4	CCTB3	CCTB2	CCTB1	CCTB0
		Type	rw	rwh	rw	rw	rw	rw	rw	rw
$C2_H$	**T2CCU_CCTRELLReset: 00_H** T2CCU Capture/Compare Timer Reload Register Low	Bit Field	CCTREL							
		Type	rw							
$C3_H$	**T2CCU_CCTRELHReset: 00_H** T2CCU Capture/Compare Timer Reload Register High	Bit Field	CCTREL							
		Type	rw							
$C4_H$	**T2CCU_CCTL** **Reset: 00_H** T2CCU Capture/Compare Timer Register Low	Bit Field	CCT							
		Type	rwh							

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T2CCU_CCTH Reset: 00_H** T2CCU Capture/Compare Timer Register High	Bit Field	CCT							
		Type	rwh							
$C6_H$	**T2CCU_CCTCON Reset: 00_H** T2CCU CaptureCcompare Timer Control Register	Bit Field	CCTPRE				CCTOVF	CCTOVEN	TIMSYN	CCTST
		Type	rw				rwh	rw	rw	rw
RMAP = 0, PAGE 2										
$C0_H$	**T2CCU_COSHDWReset: 00_H** T2CCU Capture/compare Enable Register	Bit Field	ENSHDW	TXOV	COOUT5	COOUT4	COOUT3	COOUT2	COOUT1	COOUT0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$C1_H$	**T2CCU_CC0L Reset: 00_H** T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC0H Reset: 00_H** T2CCU Capture/compare Register 0 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC1L Reset: 00_H** T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC1H Reset: 00_H** T2CCU Capture/compare Register 1 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC2L Reset: 00_H** T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC2H Reset: 00_H** T2CCU Capture/compare Register 2 High	Bit Field	CCVALH							
		Type	rwh							
RMAP = 0, PAGE 3										
$C0_H$	**T2CCU_COCON Reset: 00_H** T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD	
		Type	rw	rw	rwh	rwh	rw	rw	rw	
$C1_H$	**T2CCU_CC3L Reset: 00_H** T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC3H Reset: 00_H** T2CCU Capture/compare Register 3 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC4L Reset: 00_H** T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC4H Reset: 00_H** T2CCU Capture/compare Register 4 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC5L Reset: 00_H** T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC5H Reset: 00_H** T2CCU Capture/compare Register 5 High	Bit Field	CCVALH							
		Type	rwh							

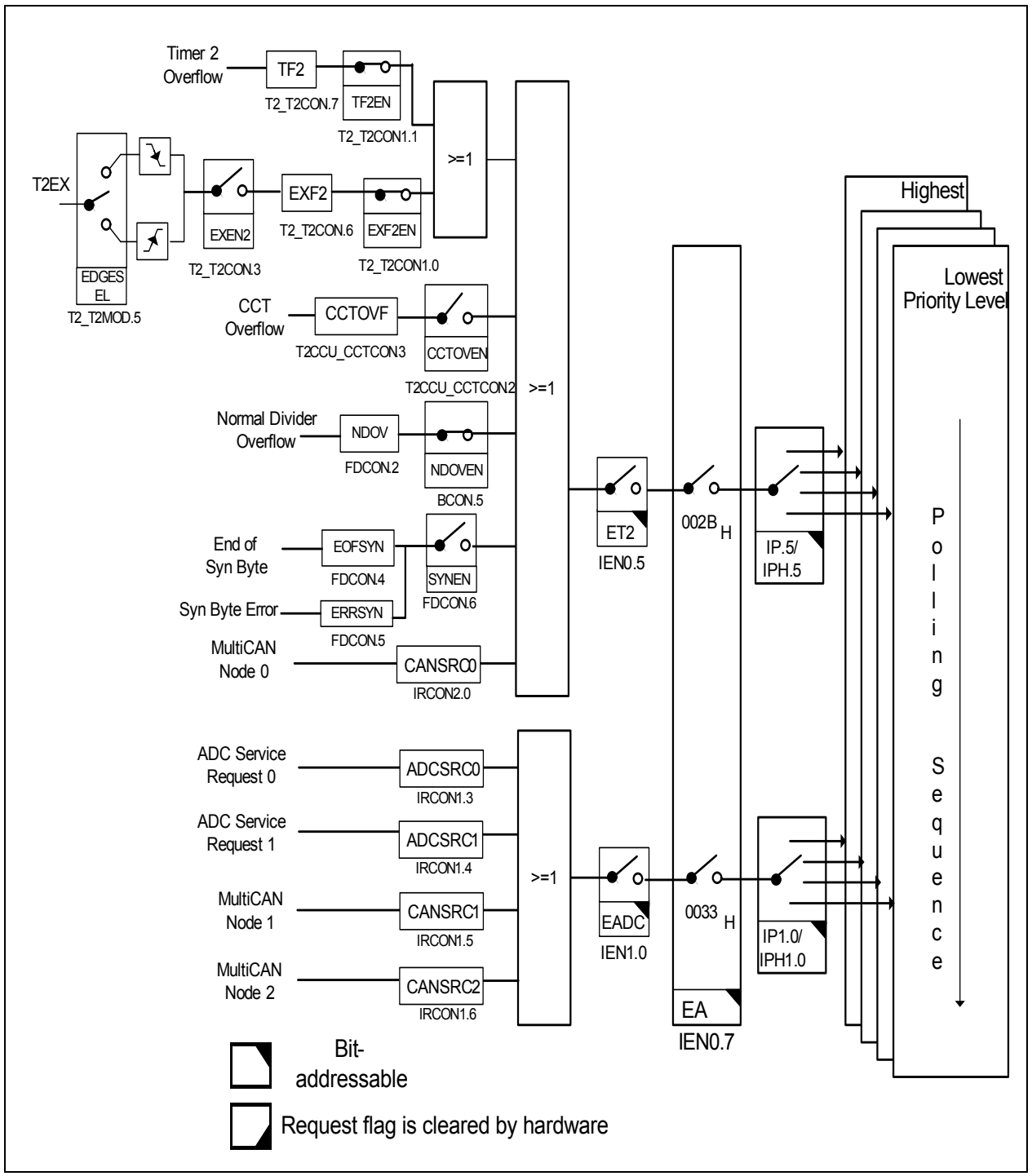


Figure 14 Interrupt Request Sources (Part 2)

3.6 Power Supply System with Embedded Voltage Regulator

The XC87x microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 19 shows the XC87x power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode[1)], the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

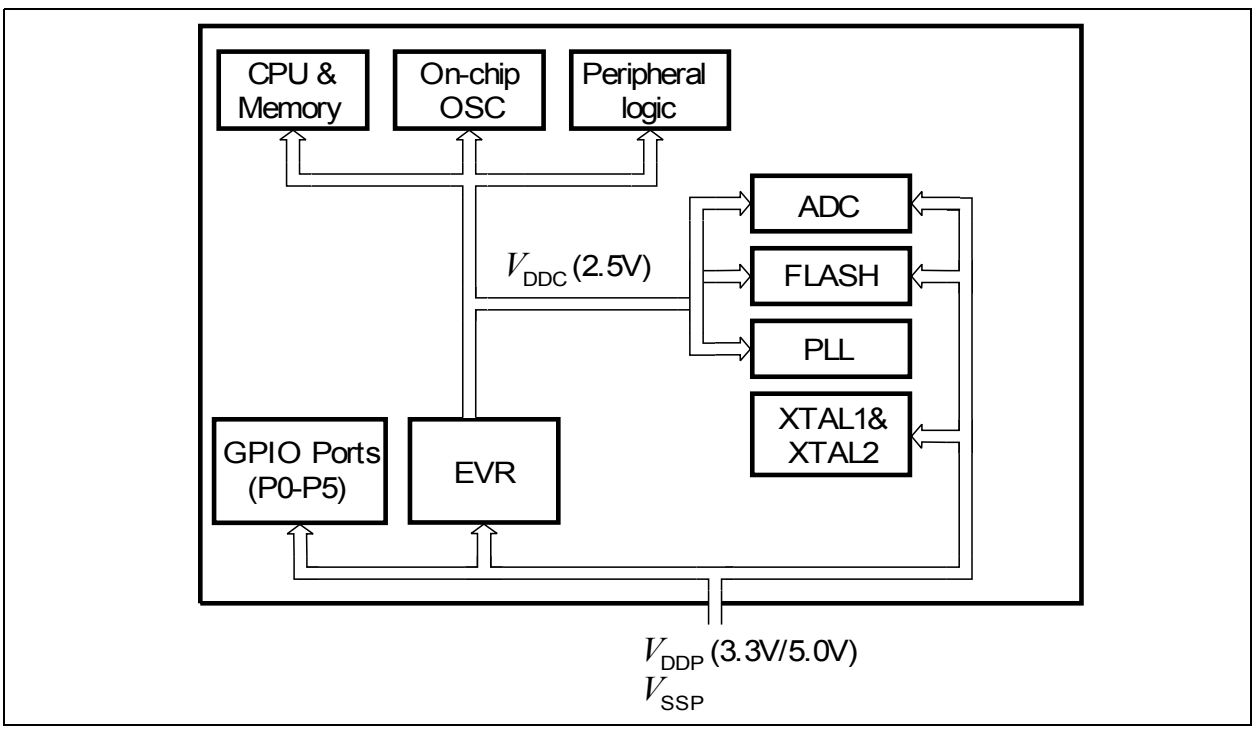


Figure 19 XC87x Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode[1)]
- V_{DDP} prewarning detection
- V_{DDC} brownout detection

1) SAK product variant does not support power-down mode.

not be bypassed for this PLL mode. The PLL mode is used during normal system operation.

(3.2)

$$f_{SYS} = f_{OSC} \times \frac{NF}{NR \times OD}$$

System Frequency Selection

For the XC87x, the value of NF, NR and OD can be selected by bits NDIV, PDIV and KDIV respectively for different oscillator inputs inorder to obtain the required fsys. But the combination of these factors must fulfill the following condition:

- 100 MHz < f_{VCO} < 175 MHz
- 800 KHz < f_{OSC} / (2 * NR) < 8 MHz

Table 26 provides examples on how the typical system frequency of fsys = 144 MHz and maximum frequency of 160 MHz (CPU clock = 26.67 MHz)can be obtained for the different oscillator sources.

Table 26 System frequency (f_{sys} = 144 MHz)

Oscillator	fosc	N	P	K	fsys
On-chip	4 MHz	72	2	1	144 MHz
	4 MHz	80	2	1	160 MHz
External	8 MHz	72	4	1	144 MHz
	6 MHz	72	3	1	144 MHz
	4 MHz	72	2	1	144 MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 2 MHz to 20 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. An external feedback resistor R_f is also required in the external oscillator circuitry. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative

– Interrupt enabling and corresponding flag

3.13 UART and UART1

The XC87x provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
  – 8-bit or 9-bit data frames, LSB first
  – Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 30**.

Table 30 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$[1)]
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and

Table 32 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
24 MHz	1	6 (6_H)	59 ($3B_H$)	+0.03 %
12 MHz	1	3 (3_H)	59 ($3B_H$)	+0.03 %
8 MHz	1	2 (2_H)	59 ($3B_H$)	+0.03 %
6 MHz	1	6 (6_H)	236 (EC_H)	+0.03 %

3.13.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)} \tag{3.6}$$

3.14 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 26**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV}, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP} \tag{3.7}$$

3.22 Analog-to-Digital Converter

The XC87x includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at AN0 - AN7.

Features

- Successive approximation
- 8-bit or 10-bit resolution
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.22.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

Figure 31 shows the clocking scheme of the ADC module. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

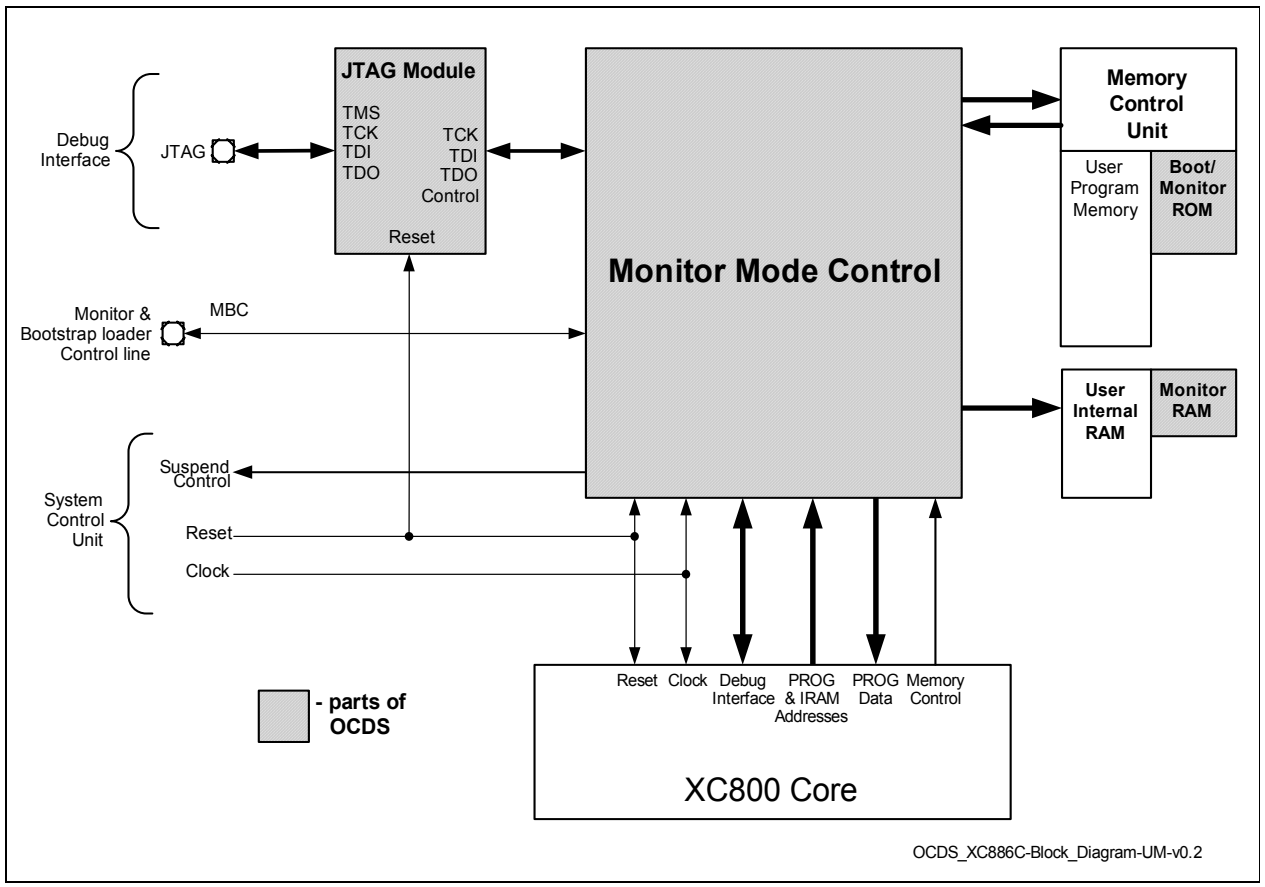


Figure 33 OCDS Block Diagram

3.23.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC87x Flash devices are given in **Table 36**.

Table 36 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC87x*-16FF	$1018\ 2083_H$
	XC87x*-13FF	$1018\ 3083_H$

Note: The asterisk (*) above denotes all possible device configurations.

4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 42 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	V_{AREF}	SR	V_{AGND} + 1	V_{DDP}	V_{DDP} + 0.05	V	[1]
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{SS}	V_{AREF} - 1	V	[1]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}		–	24	–	MHz	module clock[1]
	f_{ADCI}		–	–	14[2]	MHz	internal analog clock[1] See **Figure 31**
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	[1]
Conversion time	t_C	CC	See **Section 4.2.3.1**			µs	[1]
Differential Nonlinearity	$\lvert EA_{DNL}\rvert$	CC	–	–	1.5	LSB	10-bit conversion
Integral Nonlinearity	$\lvert EA_{INL}\rvert$	CC	–	–	2	LSB	10-bit conversion
Offset	$\lvert EA_{OFF}\rvert$	CC	–	–	3	LSB	10-bit conversion
Gain	$\lvert EA_{GAIN}\rvert$	CC	–	–	2.5	LSB	10-bit conversion
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	14	pF	[1][3]
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	4	5	pF	[1][4]

Table 44 Power Down Current[1](Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[2]	max.[3]		
V_{DDP} = 5V Range					
Power-Down Mode	I_{PDP}	20	80	µA	T_A = + 25 °C[4][5]
		-	250	µA	T_A = + 85 °C[5][6]

1) The table is only applicable to SAF and SAX variants. SAK variant does not support power-down mode

2) The typical I_{PDP} values are based on preliminary measurements and are to be used as reference only. These values are measured at V_{DDP} = 5.0 V.

3) The maximum I_{PDP} values are measured at V_{DDP} = 5.5 V.

4) I_{PDP} has a maximum value of 450 µA at T_A = + 105 °C.

5) I_{PDP} is measured with: $\overline{\text{RESET}}$ = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0 = V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

6) Not subjected to production test, verified by design/characterization.

4.3.3 Power-on Reset and PLL Timing

Table 48 provides the characteristics of the power-on reset and PLL timing in the XC87x.

Table 48 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
On-Chip Oscillator start-up time	t_{OSCST}	CC	–	–	500	ns	1)
PLL lock-in in time	t_{LOCK}	CC	–	–	200	µs	1)
PLL accumulated jitter	D_P		–	–	1.8	ns	1)2)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) PLL lock at 144 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 72 and P = 1.

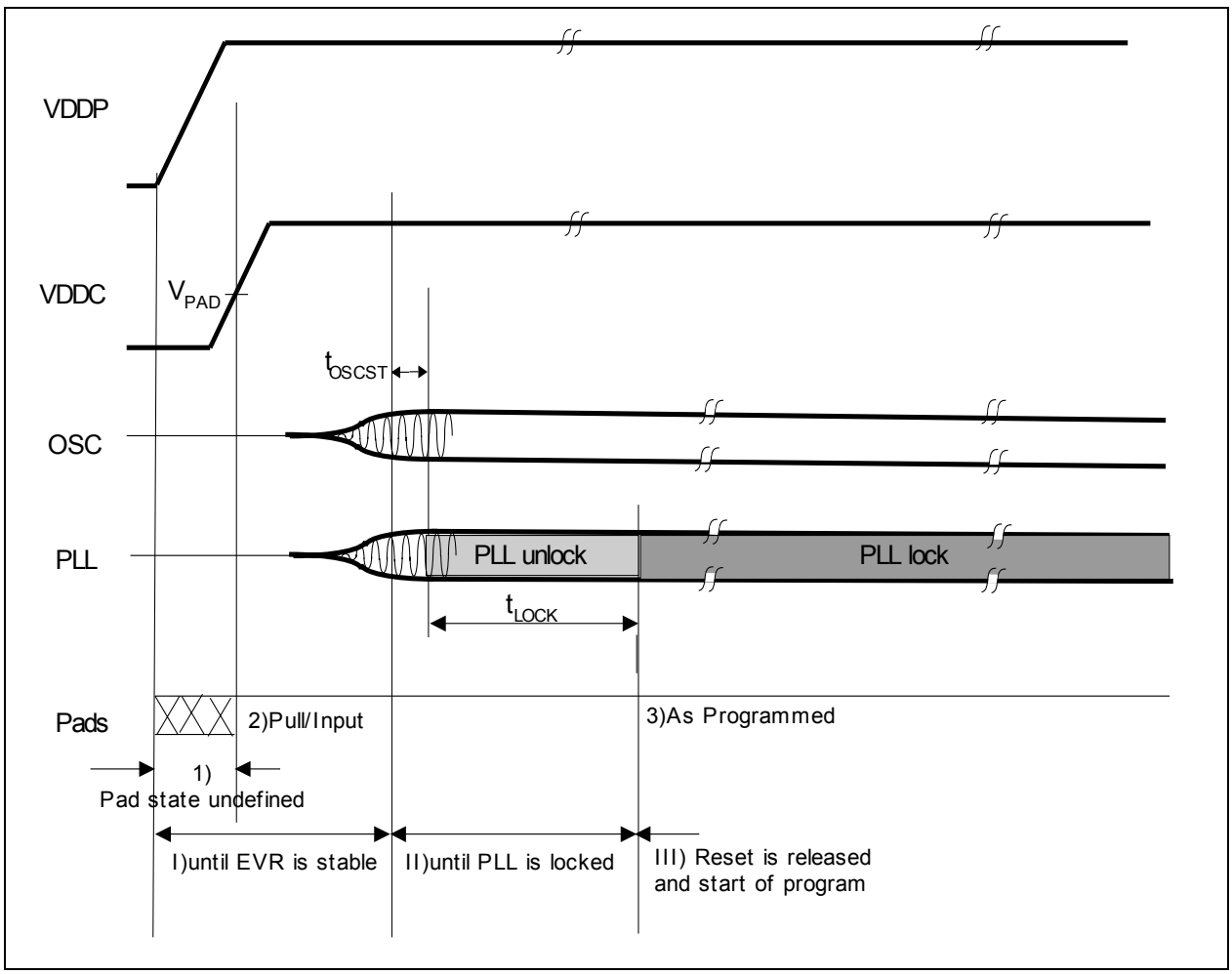


Figure 40 Power-on Reset Timing

4.3.4 On-Chip Oscillator Characteristics

Table 49 provides the characteristics of the on-chip oscillator in the XC87x.

Table 49 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM}	CC	3.88	4	4.12	MHz	under nominal conditions[1] after IFX-backend trimming
Long term frequency deviation	Δf_{LT}	CC	-5	–	5	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to 105°C), for one given device after trimming
Short term frequency deviation	Δf_{ST}	CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

4.3.7 JTAG Timing

Table 53 provides the characteristics of the JTAG timing in the XC87x.

Table 53 TCK Clock Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TCK clock period	t_{TCK}	SR	50	-	ns	1)
TCK high time	t_1	SR	20	-	ns	1)
TCK low time	t_2	SR	20	-	ns	1)
TCK clock rise time	t_3	SR	-	4	ns	1)
TCK clock fall time	t_4	SR	-	4	ns	1)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

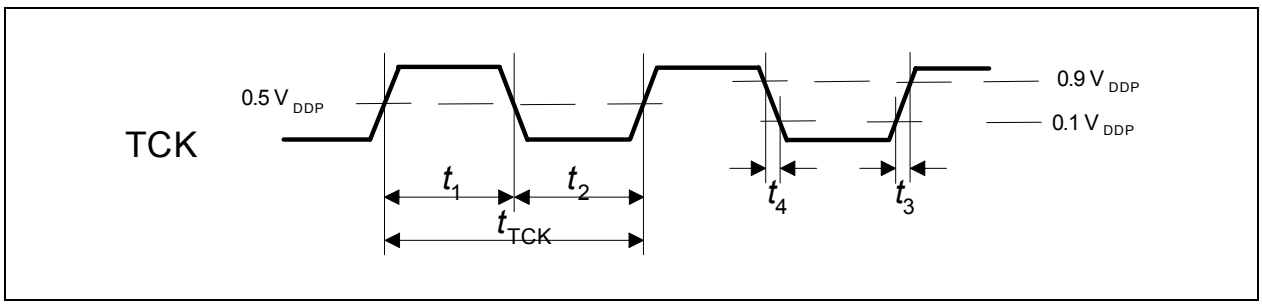


Figure 44 TCK Clock Timing

Table 54 JTAG Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TMS setup to TCK	t_1	SR	8	-	ns	1)
TMS hold to TCK	t_2	SR	0	-	ns	1)
TDI setup to TCK	t_1	SR	8	-	ns	1)
TDI hold to TCK	t_2	SR	4	-	ns	1)
TDO valid output from TCK	t_3	CC	-	24	ns	5V Device[1)]
			-	31	ns	3.3V Device[1)]

4.3.8 SSC Master Mode Timing

Table 55 provides the characteristics of the SSC timing in the XC87x.

Table 55 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
SCLK clock period	t_0	CC	$2*T_{SSC}$	–	ns	1)2)
MTSR delay from SCLK ↓	t_1	CC	0	5	ns	2)
MRST setup to SCLK ↓	t_2	SR	13	–	ns	2)
MRST hold from SCLK ↓	t_3	SR	0	–	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3ns. T_{CPU} is the CPU clock period.

2) 1Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

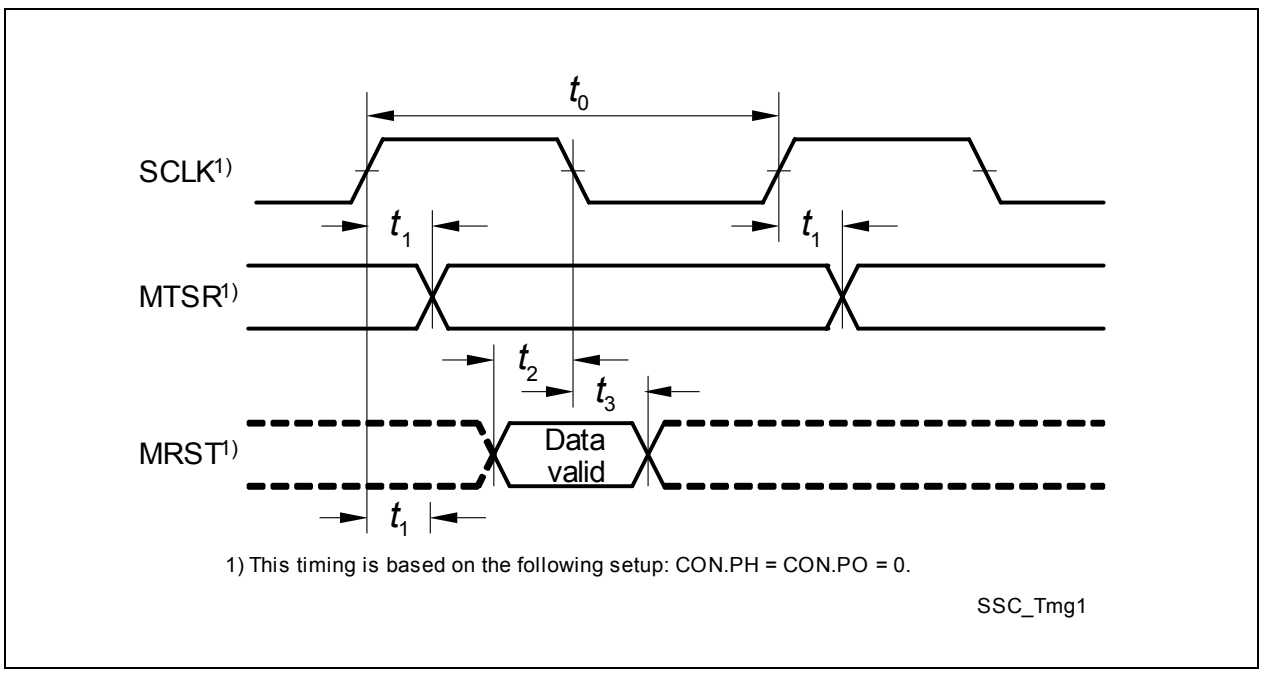


Figure 46 SSC Master Mode Timing