Infineon Technologies - SAX-XC878L-16FFA 5V AA Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	LINbus, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sax-xc878l-16ffa-5v-aa

Never stop thinking

8-Bit

XC87xCLM

8-Bit Single-Chip Microcontroller

Data Sheet

V1.5 2011-03

Microcontrollers

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - Loss-of-Clock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINT0[1)]
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Five ports
  - Up to 40 pins as digital I/O
  - 8 dedicated analog inputs used as A/D converter input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Two Capture/compare units
  - Capture/compare unit 6 for PWM signal generation (CCU6)
  - Timer 2 Capture/compare unit for vaious digital signal generation (T2CCU)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Packages:
  - PG-LQFP-64
  - PG-VQFN-48
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAX (-40 to 105 °C)
  - SAK (-40 to 125 °C)

1) SAK product variant does not support power-down mode.

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P0.3	63/1		Hi-Z	SCK_1 COUT63_1 RXDO1_0 A17	SSC Clock Input/Output Output of Capture/Compare channel 3 UART1 Transmit Data Output Address Line 17 Output
P0.4	64/2		Hi-Z	MTSR_1 CC62_1 TXD1_0 A18	SSC Master Transmit Output/ Slave Receive Input Input/Output of Capture/Compare channel 2 UART1 Transmit Data Output/Clock Output Address Line 18 Output
P0.5	1/3		Hi-Z	MRST_1 EXINT0_0 T2EX1_1 RXD1_0 COUT62_1 A19	SSC Master Receive Input/Slave Transmit Output External Interrupt Input 0 Timer 21 External Trigger Input UART1 Receive Data Input Output of Capture/Compare channel 2 Address Line 19 Output
P0.6	2/4		PU	$\overline{\text{T2CC4\_1}}$ $\overline{\text{WR}}$	Compare Output Channel 4 External Data Write Control Output
P0.7	62/48		PU	CLKOUT_1 $\overline{\text{T2CC5\_1}}$ $\overline{\text{RD}}$	Clock Output Compare Output Channel 5 External Data Read Control Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P1.5	39/30		PU	CCPOS0_1 CCU6 Hall Input 0 EXINT5_0 External Interrupt Input 5 T1_1 Timer 1 Input MRST_2 SSC Master Receive Input/ Slave Transmit Output EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output
P1.6	10/9		PU	CCPOS1_1 CCU6 Hall Input 1 T12HR_0 CCU6 Timer 12 Hardware Run Input EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	11/10		PU	CCPOS2_1 CCU6 Hall Input 2 T13HR_0 CCU6 Timer 13 Hardware Run Input T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P3.4	51/37		Hi-Z	CC62_0	Input/Output of Capture/Compare channel 2
				RXDC0_1	MultiCAN Node 0 Receiver Input
				T2EX1_0	Timer 21 External Trigger Input
				T2CC3_1/ EXINT6_3	External Interrupt Input 6/T2CCU Capture/Compare Channel 3
				A14	Address Line 14 Output
P3.5	52/38		Hi-Z	COUT62_0	Output of Capture/Compare channel 2
				EXF21_0	Timer 21 External Flag Output
				TXDC0_1	MultiCAN Node 0 Transmitter Output
				A15	Address Line 15 Output
P3.6	41/32		PU	$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
P3.7	42/-		Hi-Z	EXINT4_0	External Interrupt Input 4
				COUT63_0	Output of Capture/Compare channel 3
				A16	Address Line 16 Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P4.5	46/-		Hi-Z	CCPOS1_3 T1_0 COUT61_2 T2CC3_0/ EXINT6_2 D5	CCU6 Hall Input 1 Timer 1 Input Output of Capture/Compare channel 1 External Interrupt Input 6/T2CCU Capture/Compare Channel 3 Data Line 5 Input/Output
P4.6	47/-		Hi-Z	CCPOS2_3 T2_0 CC62_2 T2CC4_0 D6	CCU6 Hall Input 2 Timer 2 Input Output of Capture/Compare channel 2 Compare Output Channel 4 Data Line 6 Input/Output
P4.7	48/-		Hi-Z	$\overline{\text{CTRAP}}$_3 COUT62_2 T2CC5_0 D7	CCU6 Trap Input Output of Capture/Compare channel 2 Compare Output Channel 5 Data Line 7 Input/Output

3 Functional Description

Chapter 3 provides an overview of the XC87x functional description.

3.1 Processor Architecture

The XC87x is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC87x CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC87x CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 6 shows the CPU functional blocks.

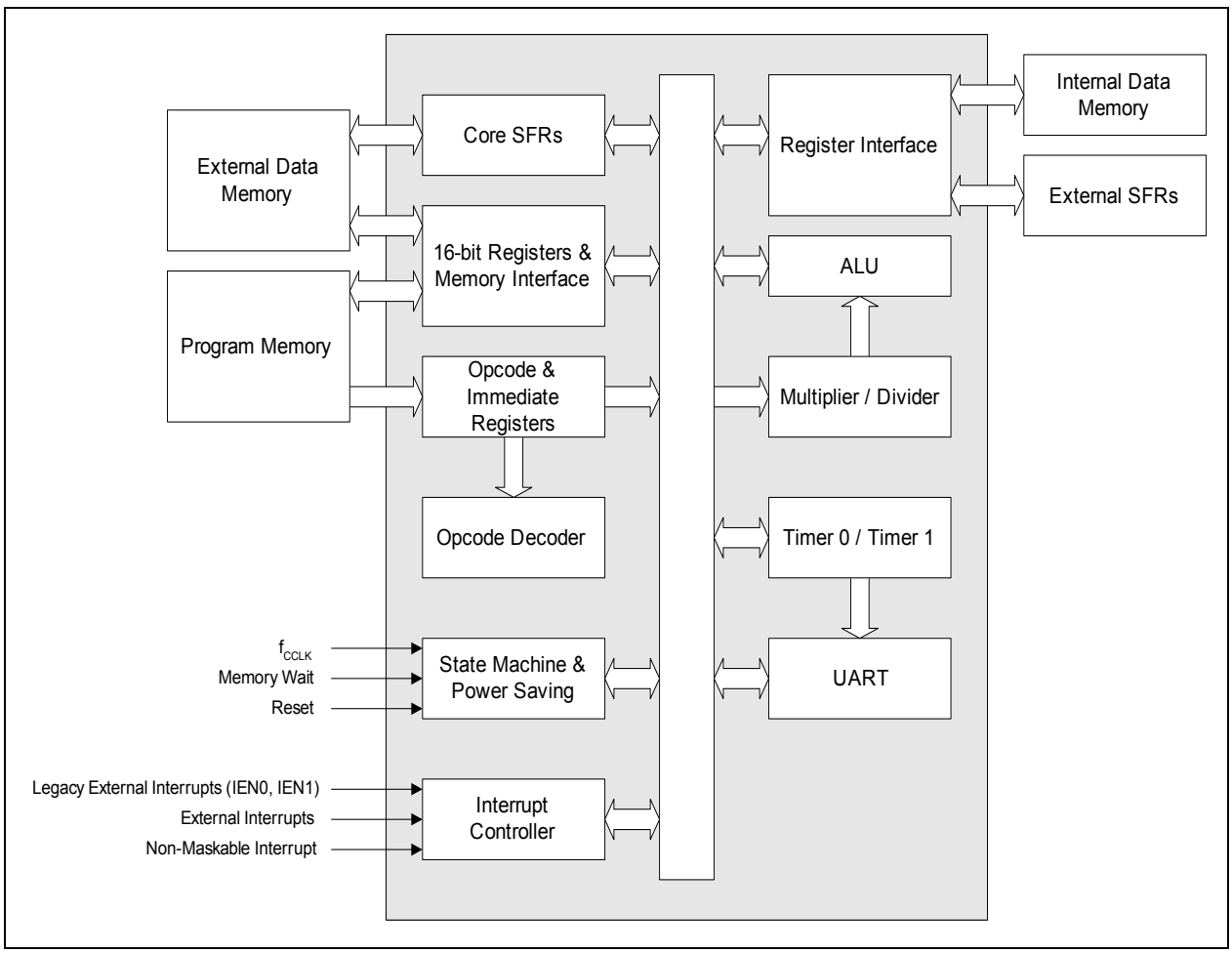

Figure 6 CPU Block Diagram

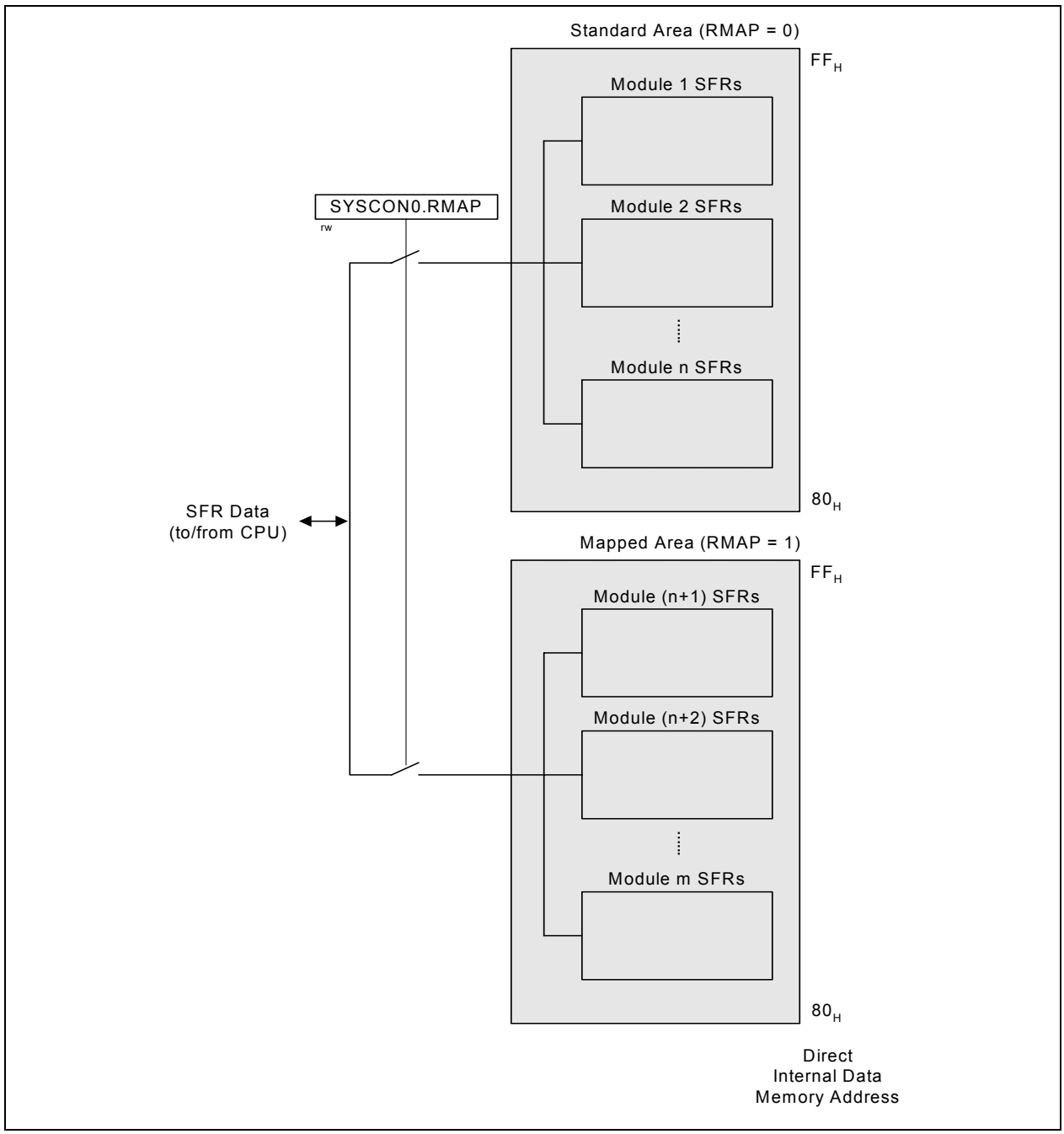

Figure 9 Address Extension by Mapping

Table 5 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
97_H	**MEXSP** **Reset: $7F_H$** Memory Extension Stack Pointer Register	Bit Field	0	MXSP						
		Type	r	rwh						
98_H	**SCON** **Reset: 00_H** Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
99_H	**SBUF** **Reset: 00_H** Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
$A2_H$	**EO** **Reset: 00_H** Extended Operation Register	Bit Field	0			TRAP_EN	0			DPSEL0
		Type	r			rw	r			rw
$A8_H$	**IEN0** **Reset: 00_H** Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
$B8_H$	**IP** **Reset: 00_H** Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
$B9_H$	**IPH** **Reset: 00_H** Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
$D0_H$	**PSW** **Reset: 00_H** Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
$E0_H$	**ACC** **Reset: 00_H** Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$E8_H$	**IEN1** **Reset: 00_H** Interrupt Enable Register 1	Bit Field	ECCIP3	ECCIP2	ECCIP1	ECCIP0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F0_H$	**B** **Reset: 00_H** B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F8_H$	**IP1** **Reset: 00_H** Interrupt Priority 1 Register	Bit Field	PCCIP3	PCCIP2	PCCIP1	PCCIP0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F9_H$	**IPH1** **Reset: 00_H** Interrupt Priority 1 High Register	Bit Field	PCCIP3H	PCCIP2H	PCCIP1H	PCCIP0H	PXMH	PX2H	PSSCH	PADCH
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 MDU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$B0_H$	**MDUSTAT** **Reset: 00_H** MDU Status Register	Bit Field	0					BSY	IERR	IRDY
		Type	r					rh	rwh	rwh

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 4										
$C2_H$	**T2CCU_CCTDTCLReset: 00_H** T2CCU Capture/Compare Timer Dead-Time Control Register Low	Bit Field	DTM							
		Type	rw							
$C3_H$	**T2CCU_CCTDTCHReset: 00_H** T2CCU Capture/Compare Timer Dead-Time Control Register High	Bit Field	DTRES	DTR2	DTR1	DTR0	DTLEV	DTE2	DTE1	DTE0
		Type	rwh	rh	rh	rh	rw	rw	rw	rw

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C0_H$	**T21_T2CON Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T21_T2MOD Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C2_H$	**T21_RC2L Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T21_RC2H Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T21_T2L Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
$C5_H$	**T21_T2H Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							
$C6_H$	**T21_T2CON1 Reset: 03_H** Timer 2 Control Register 1	Bit Field	0						TF2EN	EXF2EN
		Type	r						rw	rw

3.2.4.15 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 19 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$D1_H$	**FCON** **Reset: 10_H** P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVSTR	MAS1	ERASE	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
$D2_H$	**EECON** **Reset: 10_H** D-Flash Control Register	Bit Field	0	EEBSY	YE	1	NVSTR	MAS1	ERASE	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
$D3_H$	**FCS** **Reset: 80_H** Flash Control and Status Register	Bit Field	1	SBEIE	FTEN	0	EEDERR	EESERR	FDERR	FSERR
		Type	r	rw	rwh	r	rwh	rwh	rwh	rwh
$D4_H$	**FEAL** **Reset: 00_H** Flash Error Address Register, Low Byte	Bit Field	ECCEADDR							
		Type	rh							
$D5_H$	**FEAH** **Reset: 00_H** Flash Error Address Register, High Byte	Bit Field	ECCEADDR							
		Type	rh							
$D6_H$	**FTVAL** **Reset: 78_H** Flash Timer Value Register	Bit Field	MODE	OFVAL						
		Type	rw	rw						
DD_H	**FCS1** **Reset: 00_H** Flash Control and Status Register 1	Bit Field	0							EEABORT
		Type	r							rwh

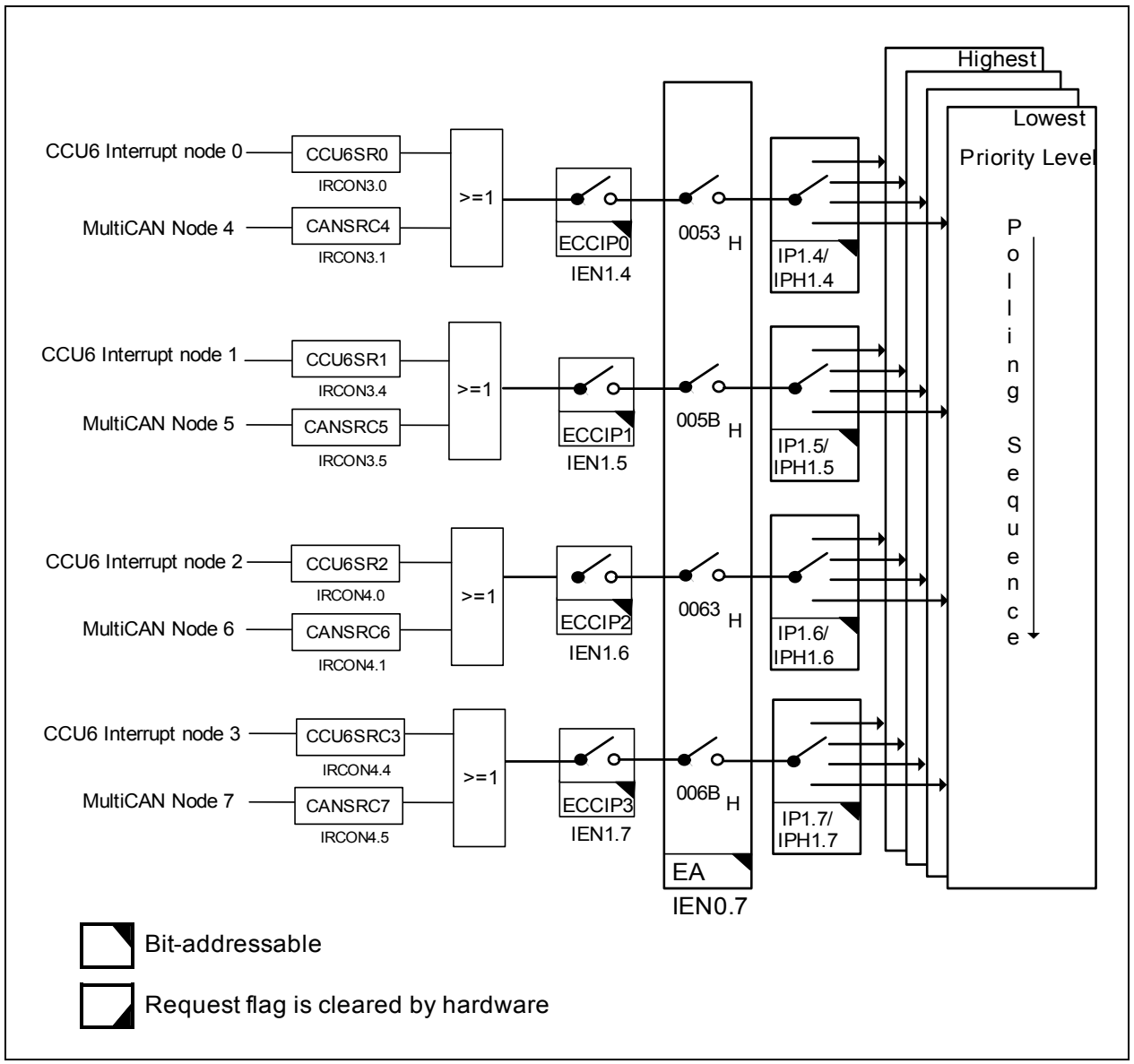

Figure 17 Interrupt Request Sources (Part 5)

3.9 Power Saving Modes

The power saving modes of the XC87x provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 23**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

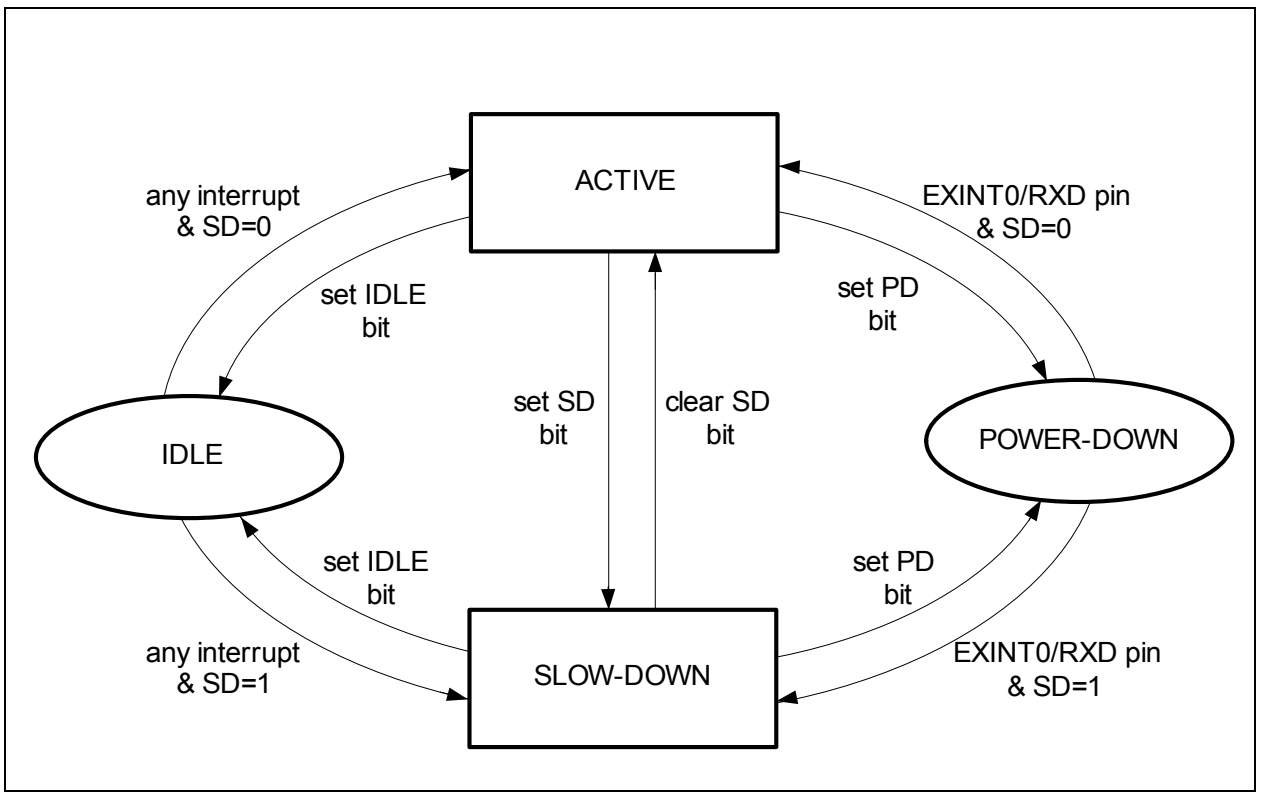

Figure 23 Transition between Power Saving Modes

Note: SAK product variant does not support power-down mode.

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC87x system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC87x will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 24** shows the block diagram of the WDT unit.

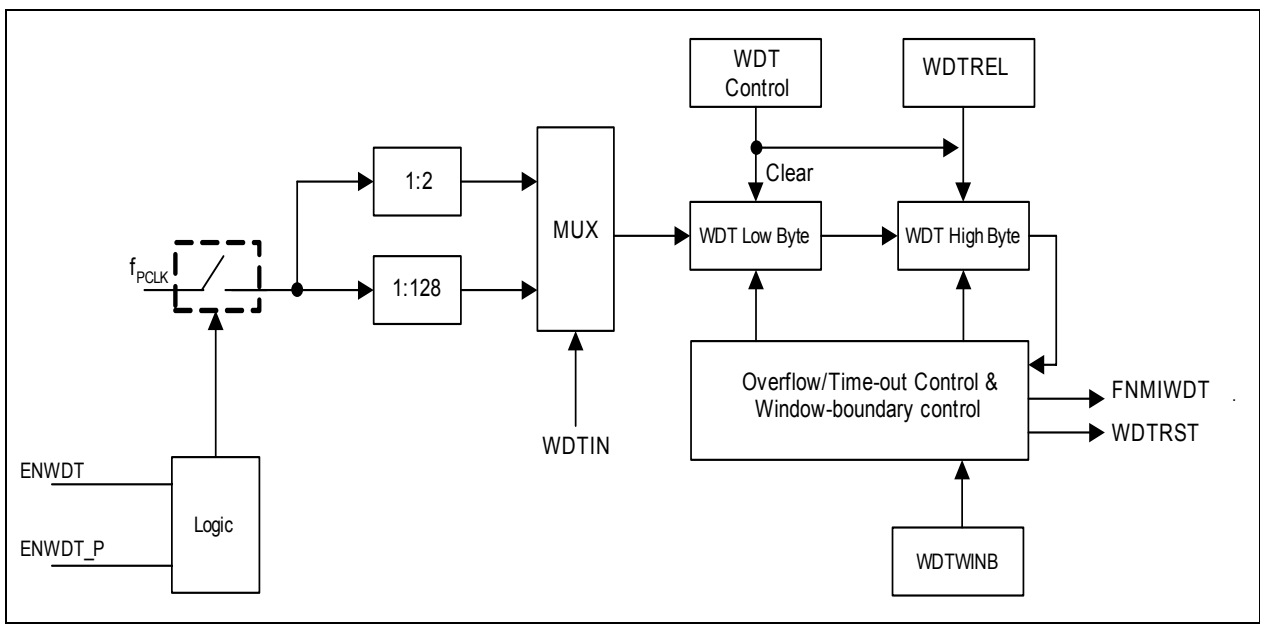

Figure 24 WDT Block Diagram

3.11 Multiplication/Division Unit

The Multiplication/Division Unit (MDU) provides fast 16-bit multiplication, 16-bit and 32-bit division as well as shift and normalize features. It has been integrated to support the XC87x Core in real-time control applications, which require fast mathematical computations.

Features

- Fast signed/unsigned 16-bit multiplication
- Fast signed/unsigned 32-bit divide by 16-bit and 16-bit divide by 16-bit operations
- 32-bit unsigned normalize operation
- 32-bit arithmetic/logical shift operations

Table 29 specifies the number of clock cycles used for calculation in various operations.

Table 29 MDU Operation Characteristics

Operation	Result	Remainder	No. of Clock Cycles used for calculation
Signed 32-bit/16-bit	32-bit	16-bit	33
Signed 16-bit/16bit	16-bit	16-bit	17
Signed 16-bit x 16-bit	32-bit	-	16
Unsigned 32-bit/16-bit	32-bit	16-bit	32
Unsigned 16-bit/16-bit	16-bit	16-bit	16
Unsigned 16-bit x 16-bit	32-bit	-	16
32-bit normalize	-	-	No. of shifts + 1 (Max. 32)
32-bit shift L/R	-	-	No. of shifts + 1 (Max. 32)

3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits.The clock frequency of T2CCU, f_{T2CCU}, could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be ‘reset’ immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
  – Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
  – Active level can be defined by register bit for channel groups A and B.
  – Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 42 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	V_{AREF}	SR	V_{AGND} + 1	V_{DDP}	V_{DDP} + 0.05	V	[1]
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{SS}	V_{AREF} - 1	V	[1]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}		–	24	–	MHz	module clock[1]
	f_{ADCI}		–	–	14[2]	MHz	internal analog clock[1] See **Figure 31**
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	[1]
Conversion time	t_C	CC	See **Section 4.2.3.1**			µs	[1]
Differential Nonlinearity	$\lvert EA_{DNL}\rvert$	CC	–	–	1.5	LSB	10-bit conversion
Integral Nonlinearity	$\lvert EA_{INL}\rvert$	CC	–	–	2	LSB	10-bit conversion
Offset	$\lvert EA_{OFF}\rvert$	CC	–	–	3	LSB	10-bit conversion
Gain	$\lvert EA_{GAIN}\rvert$	CC	–	–	2.5	LSB	10-bit conversion
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	14	pF	[1][3]
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	4	5	pF	[1][4]

4.2.4 Power Supply Current

Table 43, **Table 44**, **Table 45** and **Table 46** provide the characteristics of the power supply current in the XC87x.

Table 43 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	37.5	45	mA	[3] SAF and SAX variants
		40.5	48	mA	[3] SAK variant
Idle Mode	I_{DDP}	29.2	35	mA	[4] SAF and SAX variants
		32.2	38	mA	[4] SAK variant
Active Mode with slow-down enabled	I_{DDP}	10	15	mA	[5] SAF and SAX variants
		13	18	mA	[5] SAK variant
Idle Mode with slow-down enabled	I_{DDP}	9.2	14	mA	[6] SAF and SAX variants
		12.2	17	mA	[6] SAK variant

1) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 105 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

4.3.8 SSC Master Mode Timing

Table 55 provides the characteristics of the SSC timing in the XC87x.

Table 55 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
SCLK clock period	t_0	CC	$2*T_{SSC}$	–	ns	1)2)
MTSR delay from SCLK ↓	t_1	CC	0	5	ns	2)
MRST setup to SCLK ↓	t_2	SR	13	–	ns	2)
MRST hold from SCLK ↓	t_3	SR	0	–	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3ns. T_{CPU} is the CPU clock period.

2) 1Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

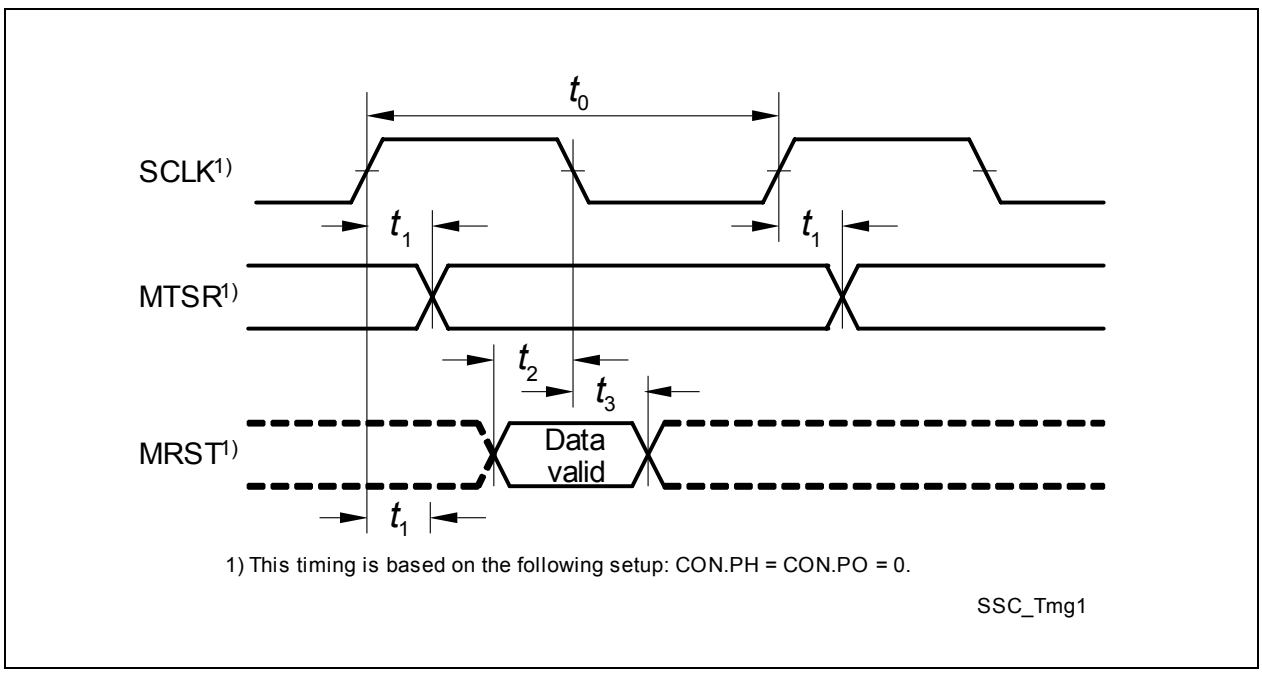

Figure 46 SSC Master Mode Timing

5 Package and Quality Declaration

Chapter 5 provides the information of the XC87x package and reliability section.

5.1 Package Parameters

Table 56 provides the thermal characteristics of the package used in XC878 and XC874.

Table 56 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
PG-LQFP-64-4 (XC878)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	34.6	K/W	-
PG-VQFN-48-22 (XC874)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	16.6	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	30.7	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.