Infineon Technologies - SAX-XC878LM-16FFA 5V AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	LINbus, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sax-xc878lm-16ffa-5v-ac

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Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P4		I/O		**Port 4** Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Bus Interface. *Note: External Bus Interface is not available in XC874.*	
P4.0	59/45		Hi-Z	RXDC0_3 CC60_1 T2CC0_0/ EXINT3_1 D0	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0 External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Data Line 0 Input/Output
P4.1	60/46		Hi-Z	TXDC0_3 COUT60_1 T2CC1_0/ EXINT4_1 D1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0 External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Data Line 1 Input/Output
P4.2	61/47		PU	EXINT6_1 T21_0 D2	External Interrupt Input 6 Timer 21 Input Data Line 2 Input/Output
P4.3	40/31		Hi-Z	T2EX_1 EXF21_1 COUT63_2 D3	Timer 2 External Trigger Input Timer 21 External Flag Output Output of Capture/Compare channel 3 Data Line 3 Input/Output
P4.4	45/-		Hi-Z	CCPOS0_3 T0_0 CC61_4 T2CC2_0/ EXINT5_1 D4	CCU6 Hall Input 0 Timer 0 Input Output of Capture/Compare channel 1 External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Data Line 4 Input/Output

Table 4 Flash Protection Modes (cont'd)

Flash Protection	Without hardware protection	With hardware protection	
P-Flash program and erase	Possible	Possible only on the condition that MSB - 1 of password is set to 1	Possible only on the condition that MSB - 1 of password is set to 1
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
External access to D-Flash	Not possible	Not possible	Not possible
D-Flash program	Possible	Possible	Possible, on the condition that MSB - 1 of password is set to 1
D-Flash erase	Possible	Possible, on these conditions: • MISC_CON.DFLASHEN bit is set to 1 prior to each erase operation; or • the MSB - 1 of password is set to 1	Possible, on the condition that MSB - 1 of password is set to 1

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. To disable the flash protection, a password match is required. A password match triggers an automatic erase of the protected P-Flash and D-Flash contents, including the programmed password. With a valid password, the Flash hardware protection is then enabled or disabled upon next reset. For the other protection strategies, no reset is necessary.

Although no protection scheme can be considered infallible, the XC87x memory protection strategy provides a very high level of protection for a general purpose microcontroller.

Note: If ROM read-out protection is enabled, only read instructions in the ROM memory can target the ROM contents.

SYSCON0
System Control Register 0 **Reset Value: 04_H**

7	6	5	4	3	2	1	0
	0		**IMODE**	**0**	**1**	**0**	**RMAP**
	r		rw	r	r	r	rw

Field	Bits	Type	Description
RMAP	0	rw	**Interrupt Node XINTR0 Enable** 0 The access to the standard SFR area is enabled 1 The access to the mapped SFR area is enabled
1	2	r	**Reserved** Returns 1 if read; should be written with 1.
0	[7:5], 3,1	r	**Reserved** Returns 0 if read; should be written with 0.

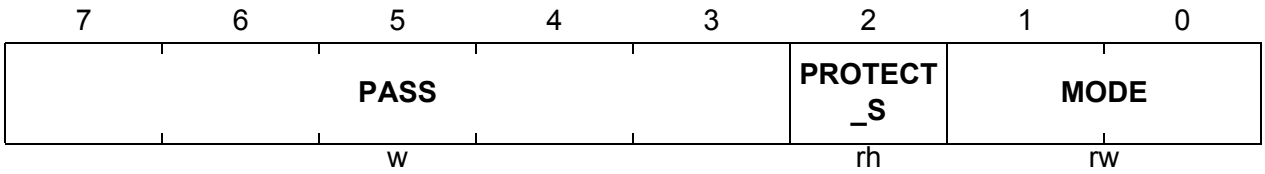
Note: The RMAP bit should be cleared/set by ANL or ORL instructions.The rest bits of SYSCON0 should not be modified.

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC87x has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 10**.

3.2.3.1 Password Register

PASSWD
Password Register **Reset Value: 07_H**



Field	Bits	Type	Description
MODE	[1:0]	rw	**Bit Protection Scheme Control Bits** 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others:Scheme Enabled. These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	**Bit Protection Signal Status Bit** This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits.
PASS	[7:3]	w	**Password Bits** The Bit Protection Scheme only recognizes three patterns. 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits

Table 6 MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B1_H$	**MDUCON** **Reset: 00_H** MDU Control Register	Bit Field	IE	IR	RSEL	START	OPCODE			
		Type	rw	rw	rw	rwh	rw			
$B2_H$	**MD0** **Reset: 00_H** MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
$B2_H$	**MR0** **Reset: 00_H** MDU Result Register 0	Bit Field	DATA							
		Type	rh							
$B3_H$	**MD1** **Reset: 00_H** MDU Operand Register 1	Bit Field	DATA							
		Type	rw							
$B3_H$	**MR1** **Reset: 00_H** MDU Result Register 1	Bit Field	DATA							
		Type	rh							
$B4_H$	**MD2** **Reset: 00_H** MDU Operand Register 2	Bit Field	DATA							
		Type	rw							
$B4_H$	**MR2** **Reset: 00_H** MDU Result Register 2	Bit Field	DATA							
		Type	rh							
$B5_H$	**MD3** **Reset: 00_H** MDU Operand Register 3	Bit Field	DATA							
		Type	rw							
$B5_H$	**MR3** **Reset: 00_H** MDU Result Register 3	Bit Field	DATA							
		Type	rh							
$B6_H$	**MD4** **Reset: 00_H** MDU Operand Register 4	Bit Field	DATA							
		Type	rw							
$B6_H$	**MR4** **Reset: 00_H** MDU Result Register 4	Bit Field	DATA							
		Type	rh							
$B7_H$	**MD5** **Reset: 00_H** MDU Operand Register 5	Bit Field	DATA							
		Type	rw							
$B7_H$	**MR5** **Reset: 00_H** MDU Result Register 5	Bit Field	DATA							
		Type	rh							

3.2.4.3 CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7 CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$9A_H$	**CD_CORDXL** **Reset: 00_H** CORDIC X Data Low Byte	Bit Field	DATAL							
		Type	rw							
$9B_H$	**CD_CORDXH** **Reset: 00_H** CORDIC X Data High Byte	Bit Field	DATAH							
		Type	rw							

3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB_H	**WDTCON** **Reset: 00_H** Watchdog Timer Control Register	Bit Field	0		WINBEN	WDTPR	0	WDTEN	WDTRS	WDTIN
		Type	r		rw	rh	r	rw	rwh	rw
BC_H	**WDTREL** **Reset: 00_H** Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD_H	**WDTWINB** **Reset: 00_H** Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_DATA** **Reset: 00_H** P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
93_H	**P5_DIR** **Reset: 00_H** P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T2CCU_CCTH Reset: 00_H** T2CCU Capture/Compare Timer Register High	Bit Field	CCT							
		Type	rwh							
$C6_H$	**T2CCU_CCTCON Reset: 00_H** T2CCU CaptureCcompare Timer Control Register	Bit Field	CCTPRE				CCTOVF	CCTOVEN	TIMSYN	CCTST
		Type	rw				rwh	rw	rw	rw
RMAP = 0, PAGE 2										
$C0_H$	**T2CCU_COSHDWReset: 00_H** T2CCU Capture/compare Enable Register	Bit Field	ENSHDW	TXOV	COOUT5	COOUT4	COOUT3	COOUT2	COOUT1	COOUT0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$C1_H$	**T2CCU_CC0L Reset: 00_H** T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC0H Reset: 00_H** T2CCU Capture/compare Register 0 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC1L Reset: 00_H** T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC1H Reset: 00_H** T2CCU Capture/compare Register 1 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC2L Reset: 00_H** T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC2H Reset: 00_H** T2CCU Capture/compare Register 2 High	Bit Field	CCVALH							
		Type	rwh							
RMAP = 0, PAGE 3										
$C0_H$	**T2CCU_COCON Reset: 00_H** T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD	
		Type	rw	rw	rwh	rwh	rw	rw	rw	
$C1_H$	**T2CCU_CC3L Reset: 00_H** T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC3H Reset: 00_H** T2CCU Capture/compare Register 3 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC4L Reset: 00_H** T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC4H Reset: 00_H** T2CCU Capture/compare Register 4 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC5L Reset: 00_H** T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC5H Reset: 00_H** T2CCU Capture/compare Register 5 High	Bit Field	CCVALH							
		Type	rwh							

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD_H	**CCU6_MODCTRH Reset: 00_H** Modulation Control Register High	Bit Field	ECT13O	0	T13MODEN					
		Type	rw	r	rw					
FE_H	**CCU6_TRPCTRL Reset: 00_H** Trap Control Register Low	Bit Field	0					TRPM2	TRPM1	TRPM0
		Type	r					rw	rw	rw
FF_H	**CCU6_TRPCTRH Reset: 00_H** Trap Control Register High	Bit Field	TRPPEN	TRPEN13	TRPEN					
		Type	rw	rw	rw					
RMAP = 0, PAGE 3										
$9A_H$	**CCU6_MCMOUTL Reset: 00_H** Multi-Channel Mode Output Register Low	Bit Field	0	R	MCMP					
		Type	r	rh	rh					
$9B_H$	**CCU6_MCMOUTH Reset: 00_H** Multi-Channel Mode Output Register High	Bit Field	0		CURH			EXPH		
		Type	r		rh			rh		
$9C_H$	**CCU6_ISL Reset: 00_H** Capture/Compare Interrupt Status Register Low	Bit Field	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9D_H$	**CCU6_ISH Reset: 00_H** Capture/Compare Interrupt Status Register High	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9E_H$	**CCU6_PISEL0L Reset: 00_H** Port Input Select Register 0 Low	Bit Field	ISTRP		ISCC62		ISCC61		ISCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_PISEL0H Reset: 00_H** Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2		ISPOS1		ISPOS0	
		Type	rw		rw		rw		rw	
$A4_H$	**CCU6_PISEL2 Reset: 00_H** Port Input Select Register 2	Bit Field	0						IST13HR	
		Type	r						rw	
FA_H	**CCU6_T12L Reset: 00_H** Timer T12 Counter Register Low	Bit Field	T12CVL							
		Type	rwh							
FB_H	**CCU6_T12H Reset: 00_H** Timer T12 Counter Register High	Bit Field	T12CVH							
		Type	rwh							
FC_H	**CCU6_T13L Reset: 00_H** Timer T13 Counter Register Low	Bit Field	T13CVL							
		Type	rwh							
FD_H	**CCU6_T13H Reset: 00_H** Timer T13 Counter Register High	Bit Field	T13CVH							
		Type	rwh							
FE_H	**CCU6_CMPSTATL Reset: 00_H** Compare State Register Low	Bit Field	0	CC63ST	CCPOS2	CCPOS1	CCPOS0	CC62ST	CC61ST	CC60ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

3.3.1 Flash Bank Pagination

The XC87x product family offers Flash devices with either 64 Kbytes or 52 Kbytes of embedded Flash memory. Each Flash device consists of a Program Flash (P-Flash) and a single Data Flash (D-Flash) bank. P-Flash has 120 pages of 8 wordlines per page with 64 bytes per wordline. D-Flash has 64 pages of 2 wordlines per page with 32 bytes per wordline. Both types can be used for code and data storage.. The label “Data” neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different page width and wordline of each Flash bank.

The internal structure of each Flash bank represents a page architecture for flexible erase capability. The minimum erase width is always a complete page. The D-Flash bank is divided into smaller size for extended erasing and reprogramming capability; even numbers for each page size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

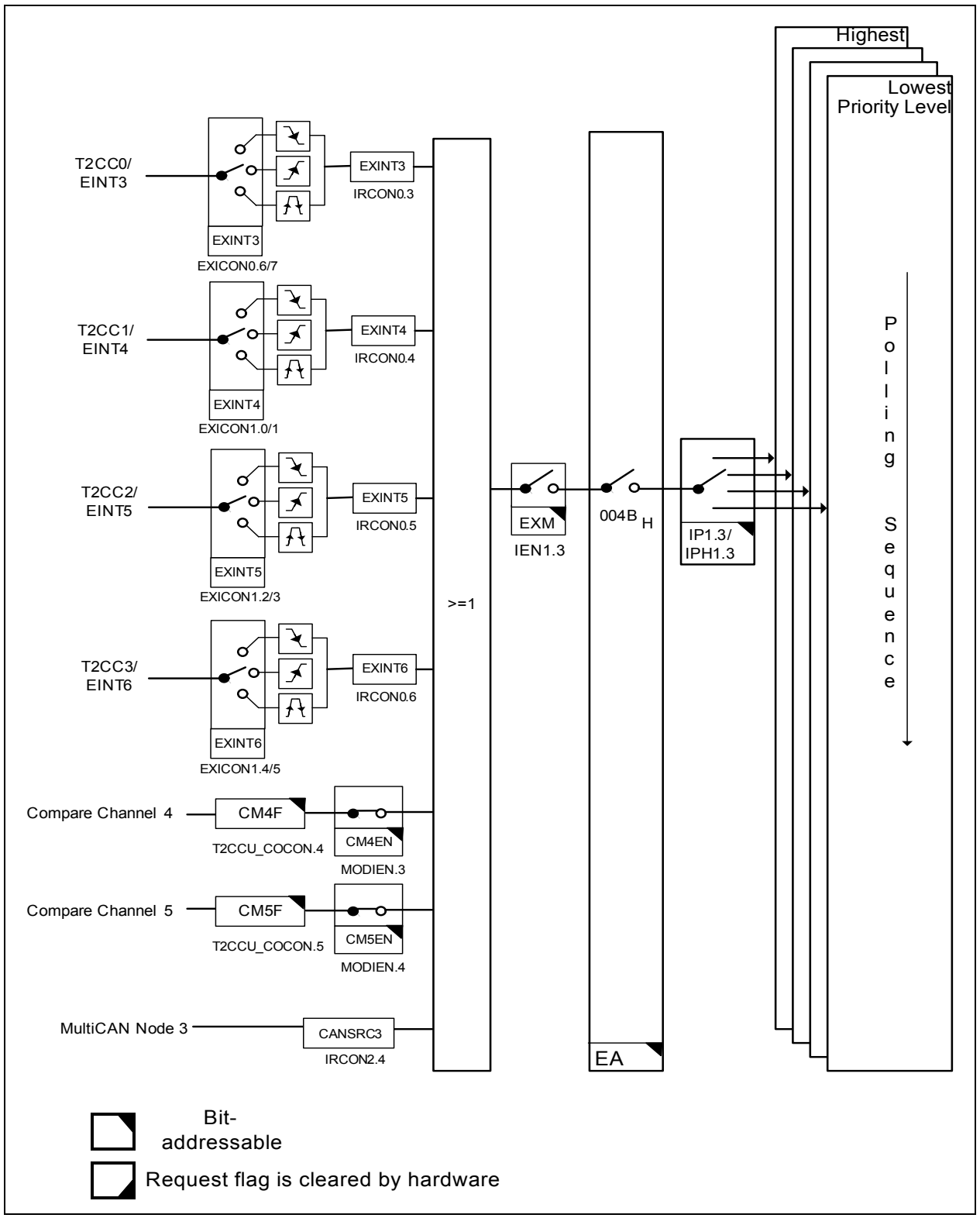


Figure 16 Interrupt Request Sources (Part 4)

For power saving purposes, the clocks may be disabled or slowed down according to Table 27.

Table 27 System frequency (f_{sys} = 144 MHz)

Power Saving Mode	Action
Idle	Clock to the CPU is disabled.
Slow-down	Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL.
Power-down[1)]	Oscillator and PLL are switched off.

1) SAK product variant does not support power-down mode.

fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 26**.

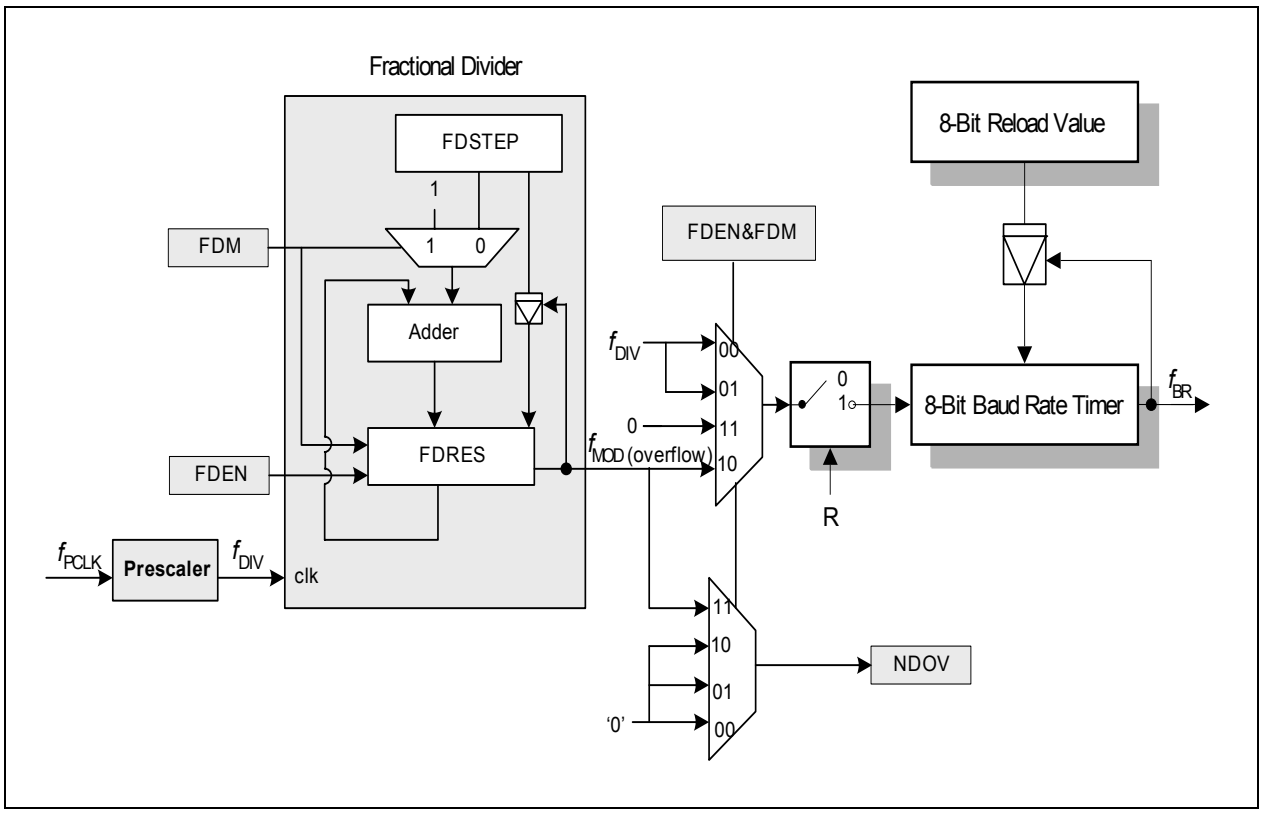


Figure 26 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

3.17 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at their respective external input pins, T0 or T1.

Timer 0 and 1 are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 33**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 33 Timer 0 and Timer 1 Modes

Mode	Operation
0	**13-bit timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**16-bit timer** The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	**8-bit timer with auto-reload** The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	**Timer 0 operates as two 8-bit timers** The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.

3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits.The clock frequency of T2CCU, f_{T2CCU}, could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be ‘reset’ immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
  – Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
  – Active level can be defined by register bit for channel groups A and B.
  – Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

3.24 Chip Identification Number

The XC87x identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 49_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

Table 37 lists the chip identification numbers of available XC87x Flash device variants.

Table 37 Chip Identification Number

Product Variant	Chip Identification Number
	AC-step
Flash Devices	
XC878-16FF 5V	$4B580063_H$
XC878M-16FF 5V	$4B580023_H$
XC878CM-16FF 5V	$4B580003_H$
XC878LM-16FF 5V	$4B500023_H$
XC878CLM-16FF 5V	$4B500003_H$
XC878-13FF 5V	$4B590463_H$
XC878M-13FF 5V	$4B590423_H$
XC878CM-13FF 5V	$4B590403_H$
XC878LM-13FF 5V	$4B510423_H$
XC878CLM-13FF 5V	$4B510403_H$
XC878-16FF 3V3	$4B180063_H$
XC878M-16FF 3V3	$4B180023_H$
XC878CM-16FF 3V3	$4B180003_H$
XC878-13FF 3V3	$4B190463_H$
XC878M-13FF 3V3	$4B190423_H$
XC878CM-13FF 3V3	$4B190403_H$
XC874CM-16FV 5V	$4B580002_H$
XC874LM-16FV 5V	$4B500022_H$
XC874-16FV 5V	$4B580062_H$

4.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 36**, **Figure 37** and **Figure 38**.

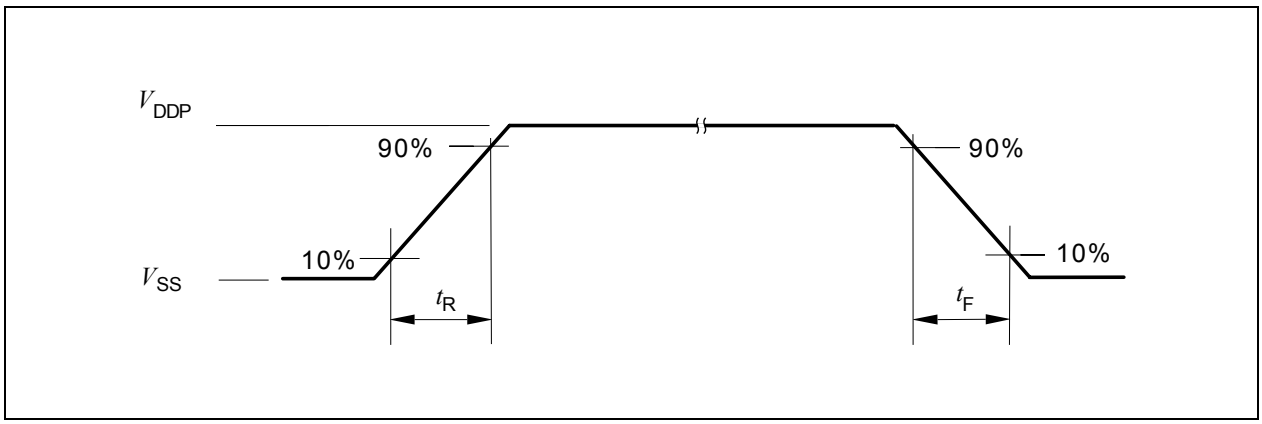


Figure 36 Rise/Fall Time Parameters

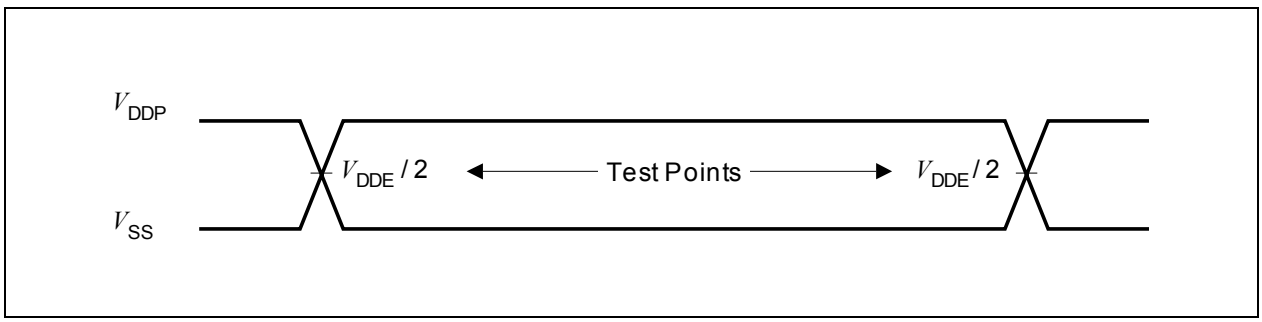


Figure 37 Testing Waveform, Output Delay

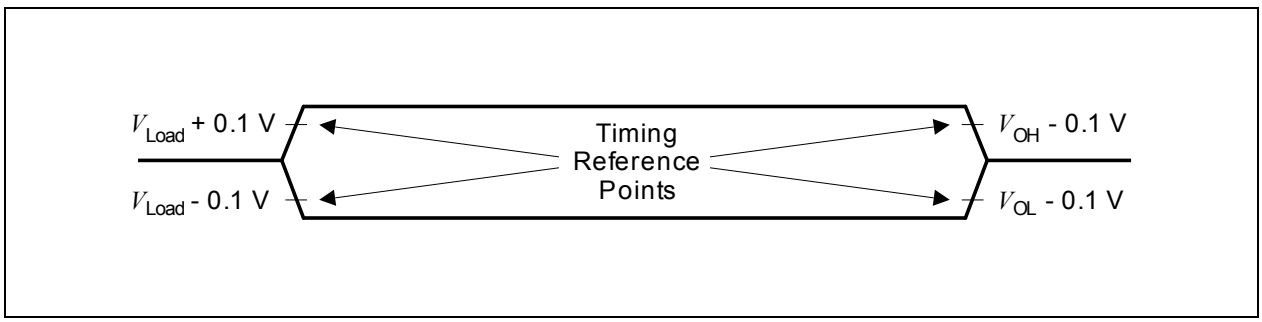


Figure 38 Testing Waveform, Output High Impedance

5 Package and Quality Declaration

Chapter 5 provides the information of the XC87x package and reliability section.

5.1 Package Parameters

Table 56 provides the thermal characteristics of the package used in XC878 and XC874.

Table 56 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
PG-LQFP-64-4 (XC878)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	34.6	K/W	-
PG-VQFN-48-22 (XC874)						
Thermal resistance junction case[1)]	R_{TJC}	CC	-	16.6	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	30.7	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.