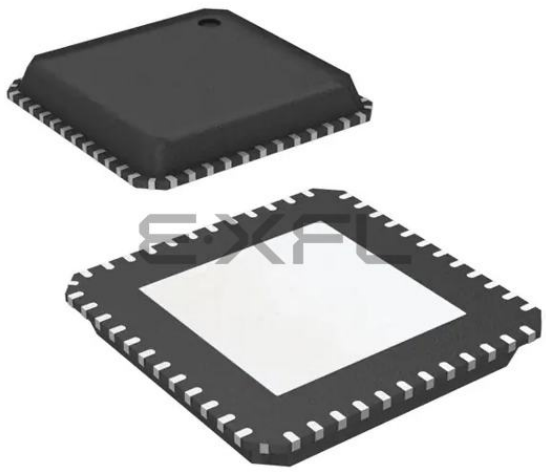

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	CANbus, LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-22
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc874clm16fva5vackxuma1

Table 2 Device Profile (cont'd)

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp-erature (°C)	Quality Profile
SAF-XC874CM-16FVA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC874CM-13FVA 5V	Flash	52	5.0	-40 to 85	Automotive
SAK-XC874LM-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874CM-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874LM-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC874CM-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC874-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC87x throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC87x, please refer to your responsible sales representative or your local distributor.

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface. *Note: External Bus Interface is not available in XC874.*
P1.0	34/25		PU	RXD_0 UART Receive Data Input T2EX_0 Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input A8 Address Line 8 Output
P1.1	35/26		PU	EXINT3_0 External Interrupt Input 3 T0_1 Timer 0 Input TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output A9 Address Line 9 Output
P1.2	36/27		PU	SCK_0 SSC Clock Input/Output A10 Address Line 10 Output
P1.3	37/28		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input SCK_2 SSC Clock Input/Output TXDC1_3 MultiCAN Node 1 Transmitter Output A11 Address Line 11 Output
P1.4	38/29		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input MTSR_2 SSC Master Transmit Output/Slave Receive Input A12 Address Line 12 Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P5		I/O		**Port 5** Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External Interface.	
P5.0	8/-		PU	EXINT1_1 A0	External Interrupt Input 1 Address Line 0 Output
P5.1	9/-		PU	EXINT2_1 A1	External Interrupt Input 2 Address Line 1 Output
P5.2	12/-		PU	RXD_2 T2CC2_2/ EXINT5_3 A2	UART Receive Data Input External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Address Line 2 Output
P5.3	13/-		PU	CCPOS0_0 EXINT1_0 T12HR_2 CC61_3 TXD_2 T2CC5_2 A3	CCU6 Hall Input 0 External Interrupt Input 1 CCU6 Timer 12 Hardware Run Input Input of Capture/Compare channel 1 UART Transmit Data Output/Clock Output Compare Output Channel 5 Address Line 3 Output
P5.4	14/-		PU	CCPOS1_0 EXINT2_0 T13HR_2 CC62_3 RXDO_2 T2CC4_2 A4	CCU6 Hall Input 1 External Interrupt Input 2 CCU6 Timer 13 Hardware Run Input Input of Capture/Compare channel 2 UART Transmit Data Output Compare Output Channel 4 Address Line 4 Output

3.2.1 Memory Protection Strategy

The XC87x memory protection strategy includes:

- Basic protection: The user is able to block any external access via the boot option to any memory
- Read-out protection: The user is able to protect the contents in the Flash
- Flash program and erase protection

These protection strategies are enabled by programming a valid password (16-bit non-one value) via Bootstrap Loader (BSL) mode 6.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in Table 4.

Table 4 Flash Protection Modes

Flash Protection	**Without hardware protection**	**With hardware protection**	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 13 of password = 0	Bit 13 of password = 1 MSB of password = 0	Bit 13 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 9**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

Table 6 MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B1_H$	**MDUCON** **Reset: 00_H** MDU Control Register	Bit Field	IE	IR	RSEL	STAR T	OPCODE			
		Type	rw	rw	rw	rwh	rw			
$B2_H$	**MD0** **Reset: 00_H** MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
$B2_H$	**MR0** **Reset: 00_H** MDU Result Register 0	Bit Field	DATA							
		Type	rh							
$B3_H$	**MD1** **Reset: 00_H** MDU Operand Register 1	Bit Field	DATA							
		Type	rw							
$B3_H$	**MR1** **Reset: 00_H** MDU Result Register 1	Bit Field	DATA							
		Type	rh							
$B4_H$	**MD2** **Reset: 00_H** MDU Operand Register 2	Bit Field	DATA							
		Type	rw							
$B4_H$	**MR2** **Reset: 00_H** MDU Result Register 2	Bit Field	DATA							
		Type	rh							
$B5_H$	**MD3** **Reset: 00_H** MDU Operand Register 3	Bit Field	DATA							
		Type	rw							
$B5_H$	**MR3** **Reset: 00_H** MDU Result Register 3	Bit Field	DATA							
		Type	rh							
$B6_H$	**MD4** **Reset: 00_H** MDU Operand Register 4	Bit Field	DATA							
		Type	rw							
$B6_H$	**MR4** **Reset: 00_H** MDU Result Register 4	Bit Field	DATA							
		Type	rh							
$B7_H$	**MD5** **Reset: 00_H** MDU Operand Register 5	Bit Field	DATA							
		Type	rw							
$B7_H$	**MR5** **Reset: 00_H** MDU Result Register 5	Bit Field	DATA							
		Type	rh							

3.2.4.3 CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7 CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$9A_H$	**CD_CORDXL** **Reset: 00_H** CORDIC X Data Low Byte	Bit Field	DATAL							
		Type	rw							
$9B_H$	**CD_CORDXH** **Reset: 00_H** CORDIC X Data High Byte	Bit Field	DATAH							
		Type	rw							

Table 8 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B7$_H$	**EXICON0** **Reset: F0$_H$** External Interrupt Control Register 0	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0	
		Type	rw		rw		rw		rw	
BA$_H$	**EXICON1** **Reset: 3F$_H$** External Interrupt Control Register 1	Bit Field	0		EXINT6		EXINT5		EXINT4	
		Type	r		rw		rw		rw	
BB$_H$	**NMICON** **Reset: 00$_H$** NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	0	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Type	r	rw	rw	r	rw	rw	rw	rw
BC$_H$	**NMISR** **Reset: 00$_H$** NMI Status Register	Bit Field	0	FNMI ECC	FNMI VDDP	0	FNMI OCDS	FNMI FLASH	FNMI PLL	FNMI WDT
		Type	r	rwh	rwh	r	rwh	rwh	rwh	rwh
BD$_H$	**BCON** **Reset: 20$_H$** Baud Rate Control Register	Bit Field	BGSEL		NDOV EN	BRDIS	BRPRE			R
		Type	rw		rw	rw	rw			rw
BE$_H$	**BG** **Reset: 00$_H$** Baud Rate Timer/Reload Register	Bit Field	BR_VALUE							
		Type	rwh							
E9$_H$	**FDCON** **Reset: 00$_H$** Fractional Divider Control Register	Bit Field	BGS	SYNE N	ERRS YN	EOFS YN	BRK	NDOV	FDM	FDEN
		Type	rw	rw	rwh	rwh	rwh	rwh	rw	rw
EA$_H$	**FDSTEP** **Reset: 00$_H$** Fractional Divider Reload Register	Bit Field	STEP							
		Type	rw							
EB$_H$	**FDRES** **Reset: 00$_H$** Fractional Divider Result Register	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 1										
B3$_H$	**ID** **Reset: 49$_H$** Identity Register	Bit Field	PRODID					VERID		
		Type	r					r		
B4$_H$	**PMCON0** **Reset: 80$_H$** Power Mode Control Register 0	Bit Field	VDDP WARN	WDT RST	WKRS	WK SEL	SD	PD	WS	
		Type	rh	rwh	rwh	rw	rw	rwh	rw	
B5$_H$	**PMCON1** **Reset: 00$_H$** Power Mode Control Register 1	Bit Field	0	CDC_ DIS	CAN_ DIS	MDU_ DIS	T2CC U_DIS	CCU_ DIS	SSC_ DIS	ADC_ DIS
		Type	r	rw	rw	rw	rw	rw	rw	rw
B6$_H$	**OSC_CON** **Reset: XX$_H$** OSC Control Register	Bit Field	PLLRD RES	PLLBY P	PLLPD	0	XPD	OSC SS	EORD RES	EXTO SCR
		Type	rwh	rwh	rw	r	rw	rwh	rwh	rh
B7$_H$	**PLL_CON** **Reset: 18$_H$** PLL Control Register	Bit Field	NDIV						PLLR	PLL_L OCK
		Type	rw						rh	rh
BA$_H$	**CMCON** **Reset: 10$_H$** Clock Control Register	Bit Field	KDIV		0	FCCF G	CLKREL			
		Type	rw		r	rw	rw			

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CC_H	**ADC_CRMR1** **Reset: 00_H** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRPND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD_H	**ADC_QMR0** **Reset: 00_H** Queue Mode Register 0	Bit Field	CEV	TREV	FLUSH	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE_H	**ADC_QSR0** **Reset: 20_H** Queue Status Register 0	Bit Field	Rsv	0	EMPTY	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF_H	**ADC_Q0R0** **Reset: 00_H** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QBUR0** **Reset: 00_H** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QINR0** **Reset: 00_H** Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A3_H$	**CCU6_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
$9A_H$	**CCU6_CC63SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 Low	Bit Field	CC63SL							
		Type	rw							
$9B_H$	**CCU6_CC63SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 High	Bit Field	CC63SH							
		Type	rw							
$9C_H$	**CCU6_TCTR4L** **Reset: 00_H** Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	0		DT RES	T12 RES	T12R S	T12R R
		Type	w	w	r		w	w	w	w
$9D_H$	**CCU6_TCTR4H** **Reset: 00_H** Timer Control Register 4 High	Bit Field	T13 STD	T13 STR	0			T13 RES	T13R S	T13R R
		Type	w	w	r			w	w	w
$9E_H$	**CCU6_MCMOUTSL** **Reset: 00_H** Multi-Channel Mode Output Shadow Register Low	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
$9F_H$	**CCU6_MCMOUTSH** **Reset: 00_H** Multi-Channel Mode Output Shadow Register High	Bit Field	STRH P	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
$A4_H$	**CCU6_ISRL** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register Low	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISRH** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register High	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
$A6_H$	**CCU6_CMPMODIFL** **Reset: 00_H** Compare State Modification Register Low	Bit Field	0	MCC6 3S	0			MCC6 2S	MCC6 1S	MCC6 0S
		Type	r	w	r			w	w	w
$A7_H$	**CCU6_CMPMODIFH** **Reset: 00_H** Compare State Modification Register High	Bit Field	0	MCC6 3R	0			MCC6 2R	MCC6 1R	MCC6 0R
		Type	r	w	r			w	w	w
FA_H	**CCU6_CC60SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 Low	Bit Field	CC60SL							
		Type	rwh							
FB_H	**CCU6_CC60SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 High	Bit Field	CC60SH							
		Type	rwh							

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD_H	**CCU6_MODCTRH** **Reset: 00_H** Modulation Control Register High	Bit Field	ECT13O	0	T13MODEN					
		Type	rw	r	rw					
FE_H	**CCU6_TRPCTRL** **Reset: 00_H** Trap Control Register Low	Bit Field	0					TRPM2	TRPM1	TRPM0
		Type	r					rw	rw	rw
FF_H	**CCU6_TRPCTRH** **Reset: 00_H** Trap Control Register High	Bit Field	TRPPEN	TRPEN13	TRPEN					
		Type	rw	rw	rw					
RMAP = 0, PAGE 3										
$9A_H$	**CCU6_MCMOUTL** **Reset: 00_H** Multi-Channel Mode Output Register Low	Bit Field	0	R	MCMP					
		Type	r	rh	rh					
$9B_H$	**CCU6_MCMOUTH** **Reset: 00_H** Multi-Channel Mode Output Register High	Bit Field	0		CURH			EXPH		
		Type	r		rh			rh		
$9C_H$	**CCU6_ISL** **Reset: 00_H** Capture/Compare Interrupt Status Register Low	Bit Field	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9D_H$	**CCU6_ISH** **Reset: 00_H** Capture/Compare Interrupt Status Register High	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9E_H$	**CCU6_PISEL0L** **Reset: 00_H** Port Input Select Register 0 Low	Bit Field	ISTRP		ISCC62		ISCC61		ISCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_PISEL0H** **Reset: 00_H** Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2		ISPOS1		ISPOS0	
		Type	rw		rw		rw		rw	
$A4_H$	**CCU6_PISEL2** **Reset: 00_H** Port Input Select Register 2	Bit Field	0						IST13HR	
		Type	r						rw	
FA_H	**CCU6_T12L** **Reset: 00_H** Timer T12 Counter Register Low	Bit Field	T12CVL							
		Type	rwh							
FB_H	**CCU6_T12H** **Reset: 00_H** Timer T12 Counter Register High	Bit Field	T12CVH							
		Type	rwh							
FC_H	**CCU6_T13L** **Reset: 00_H** Timer T13 Counter Register Low	Bit Field	T13CVL							
		Type	rwh							
FD_H	**CCU6_T13H** **Reset: 00_H** Timer T13 Counter Register High	Bit Field	T13CVH							
		Type	rwh							
FE_H	**CCU6_CMPSTATL** **Reset: 00_H** Compare State Register Low	Bit Field	0	CC63ST	CCPOS2	CCPOS1	CCPOS0	CC62ST	CC61ST	CC60ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH** **Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

3.7 Reset Control

The XC87x has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC87x is first powered up, the status of certain pins (see **Table 25**) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

The second type of reset in XC87x is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin $\overline{\text{RESET}}$ is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.

3.7.1 Module Reset Behavior

Table 24 lists the functions of the XC87x and the various reset types that affect these functions. The symbol "■" signifies that the particular function is reset to its default state.

Table 24 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core	■	■	■	■	■
Peripherals	■	■	■	■	■
On-Chip Static RAM	Not affected, Reliable	Not affected, Reliable	Not affected, Reliable	Affected, un-reliable	Affected, un-reliable
Oscillator, PLL	■	Not affected	■	■	■
Port Pins	■	■	■	■	■
EVR	The voltage regulator is switched on	Not affected	Not affected	■	■
FLASH	■	■	■	■	■
NMI	Disabled	Disabled	■	■	■

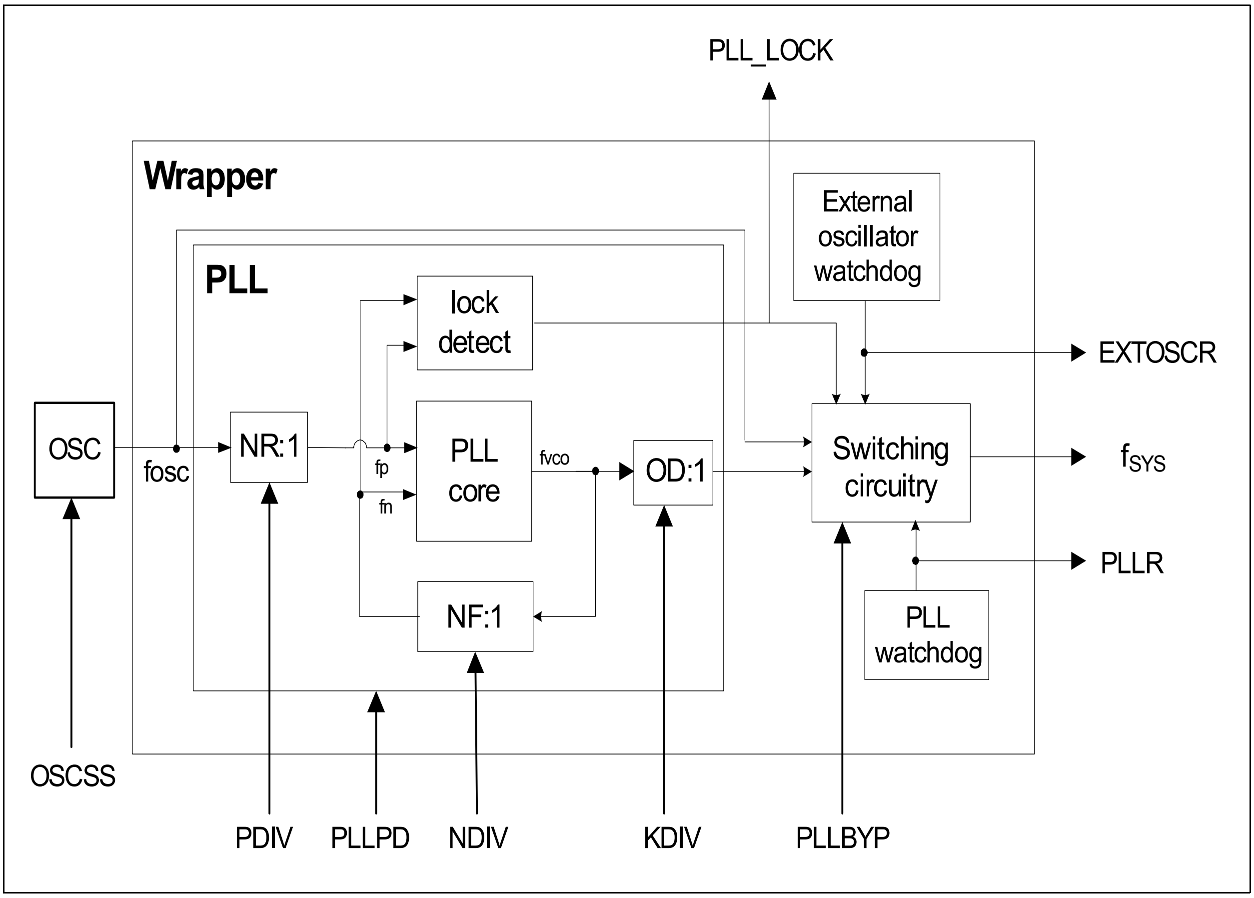

Figure 20 CGU Block Diagram

Direct Drive (PLL Bypass Operation)

During PLL bypass operation, the system clock has the same frequency as the external clock source.

(3.1)

$$f_{SYS} = f_{OSC}$$

PLL Mode

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- MultiCAN clock : MCANCLK = 24 or 48 MHz
- MDU clock : MDUCLK = 24 or 48 MHz
- CORDIC clock : CORDICCLK = 24 or 48 MHz
- CCU6 clock : CCU6CLK = 24 or 48 MHz
- T2CCU clock : T2CCUCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 22** shows the clock distribution of the XC87x.

fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 26**.

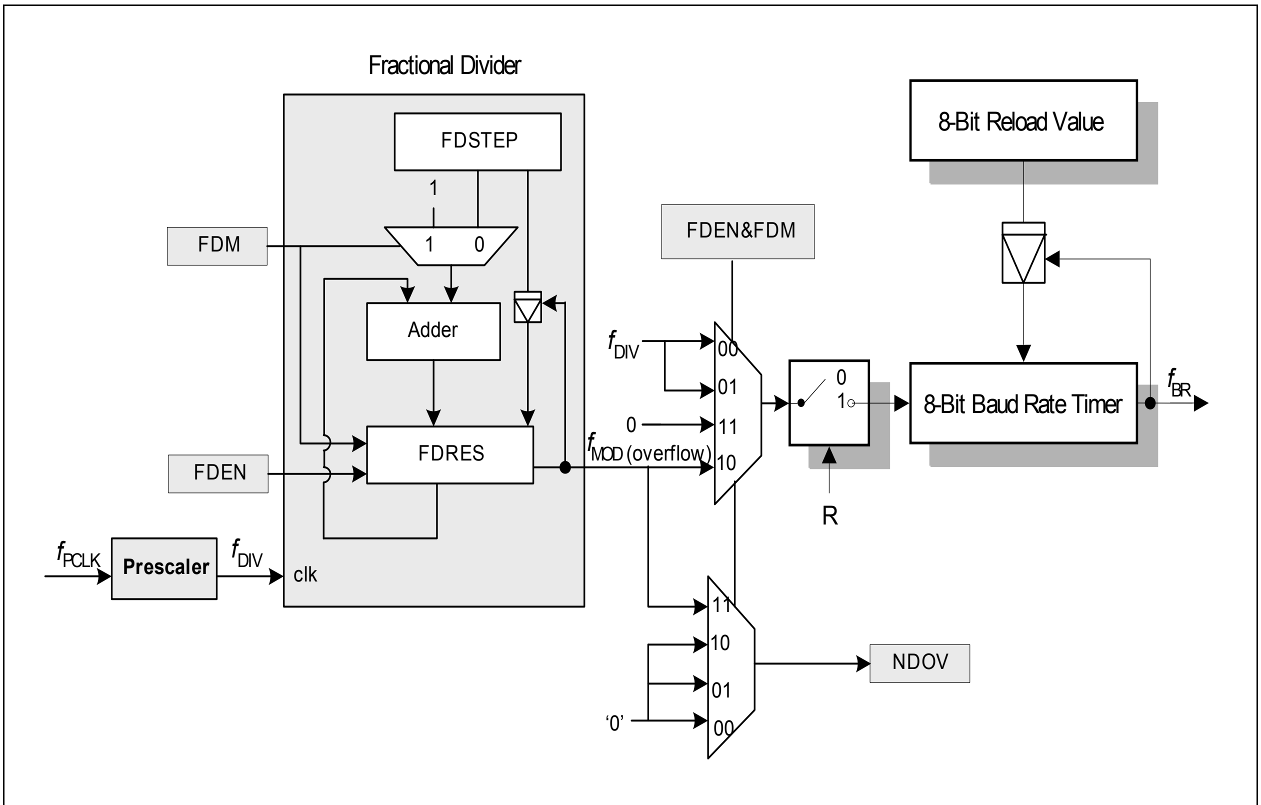

Figure 26 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP (to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

3.20 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Timer T12 Features

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Generation of center-aligned and edge-aligned PWM
- Supports single-shot mode
- Supports many interrupt request sources
- Hysteresis-like control mode

Timer T13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Supports single-shot mode

Additional Features

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The block diagram of the CCU6 module is shown in **Figure 29**.

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

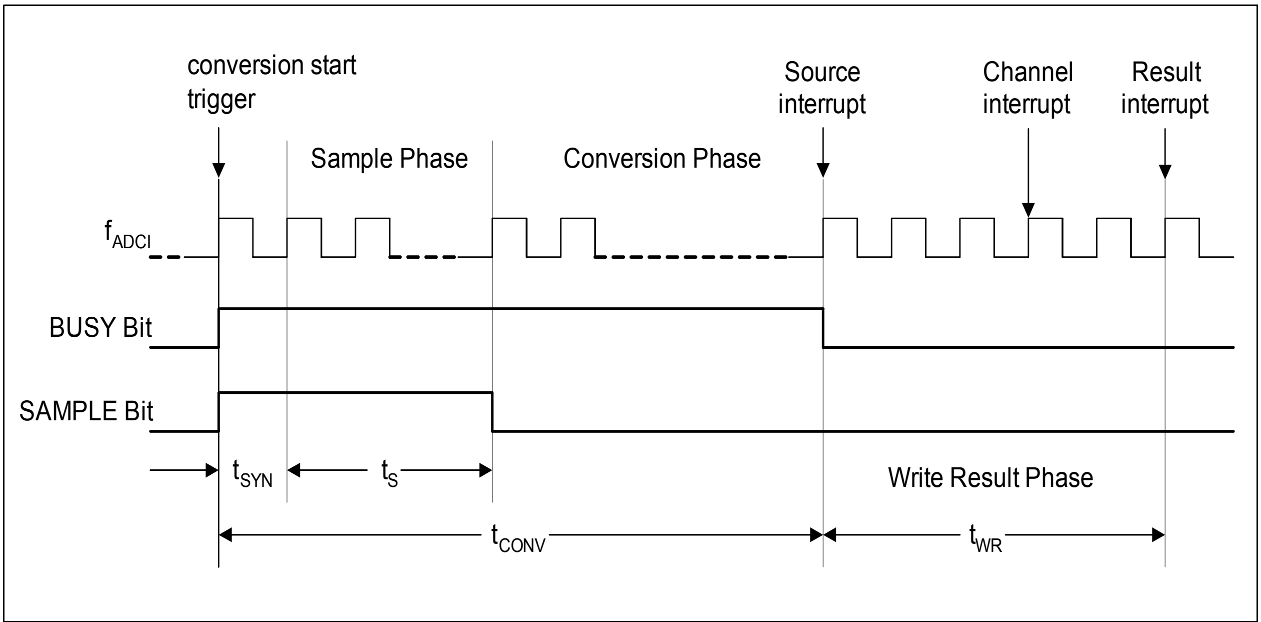

Figure 32 ADC Conversion Timing

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Characteristics

Table 40 provides the characteristics of the input/output pins of the XC87x.

Table 40 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
V_{DDP} = 5 V Range						
Output low voltage	V_{OL}	CC	–	0.6	V	I_{OL} = 9 mA (DS = 0)[1)] I_{OL} = 12 mA (DS = 1)[2)]
Output high voltage	V_{OH}	CC	2.4	–	V	I_{OH} = -20 mA (DS = 0)[1)] I_{OH} = -25 mA (DS = 1)[2)]
Input low voltage	V_{IL}	SR	-0.3	0.8	V	CMOS Mode
Input high voltage	V_{IH}	SR	2.2	V_{DDP}	V	CMOS Mode
Input Hysteresis	HYS	CC	0.35	–	V	CMOS Mode[3)7)]
Input low voltage at XTAL1	V_{ILX}	SR	-0.3	0.8	V	
Input high voltage at XTAL1	V_{IHX}	SR	3.4	V_{DDP}	V	
Pull-up current	I_{PU}	SR	–	-20	µA	$V_{IH,min}$
			-88	–	µA	$V_{IL,max}$
Pull-down current	I_{PD}	SR	–	10	µA	$V_{IL,max}$
			66	–	µA	$V_{IH,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105°C$[4)]
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	5)
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	6)

Table 40 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	6)
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	8	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	150	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	200	mA	5)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	200	mA	5)

1) DS = 0 refers to the pin having a weak drive strength which is programmable via Px_DS register.

2) DS = 1 refers to the pin having a strong drive strength which is programmable via Px_DS register.

3) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

4) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

5) Not subjected to production test, verified by design/characterization.

6) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

7) P0.1 has a minimum input hysteresis of 0.25V.

Table 42 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	[1]
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	3	kΩ	[1]

1) Not subjected to production test, verified by design/characterization.

2) This value includes the maximum oscillator deviation.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

4) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

4.2.4 Power Supply Current

Table 43, **Table 44**, **Table 45** and **Table 46** provide the characteristics of the power supply current in the XC87x.

Table 43 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	37.5	45	mA	[3] SAF and SAX variants
		40.5	48	mA	[3] SAK variant
Idle Mode	I_{DDP}	29.2	35	mA	[4] SAF and SAX variants
		32.2	38	mA	[4] SAK variant
Active Mode with slow-down enabled	I_{DDP}	10	15	mA	[5] SAF and SAX variants
		13	18	mA	[5] SAK variant
Idle Mode with slow-down enabled	I_{DDP}	9.2	14	mA	[6] SAF and SAX variants
		12.2	17	mA	[6] SAK variant

1) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 105 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}}$ = V_{DDP}; all other pins are disconnected, no load on ports.