Infineon Technologies - XC87813FFA5VACKXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc87813ffa5vackxuma1

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P0.3	63/1		Hi-Z	SCK_1 COUT63_1 RXDO1_0 A17	SSC Clock Input/Output Output of Capture/Compare channel 3 UART1 Transmit Data Output Address Line 17 Output
P0.4	64/2		Hi-Z	MTSR_1 CC62_1 TXD1_0 A18	SSC Master Transmit Output/ Slave Receive Input Input/Output of Capture/Compare channel 2 UART1 Transmit Data Output/Clock Output Address Line 18 Output
P0.5	1/3		Hi-Z	MRST_1 EXINT0_0 T2EX1_1 RXD1_0 COUT62_1 A19	SSC Master Receive Input/Slave Transmit Output External Interrupt Input 0 Timer 21 External Trigger Input UART1 Receive Data Input Output of Capture/Compare channel 2 Address Line 19 Output
P0.6	2/4		PU	$\overline{\text{T2CC4\_1}}$ $\overline{\text{WR}}$	Compare Output Channel 4 External Data Write Control Output
P0.7	62/48		PU	CLKOUT_1 $\overline{\text{T2CC5\_1}}$ $\overline{\text{RD}}$	Clock Output Compare Output Channel 5 External Data Read Control Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, T2CCU, Timer 21, MultiCAN and External Bus Interface. *Note: External Bus Interface is not available in XC874.*
P3.0	43/33		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output T2CC0_1/ EXINT3_2 External Interrupt Input 3/T2CCU Capture/Compare Channel 0
P3.1	44/34		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	49/35		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1 T2CC1_1/ EXINT4_2 External Interrupt Input 4/T2CCU Capture/Compare Channel 1
P3.3	50/36		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output T2CC2_1/ EXINT5_2 External Interrupt Input 5/T2CCU Capture/Compare Channel 2 A13 Address Line 13 Output

3.2.1 Memory Protection Strategy

The XC87x memory protection strategy includes:

- Basic protection: The user is able to block any external access via the boot option to any memory
- Read-out protection: The user is able to protect the contents in the Flash
- Flash program and erase protection

These protection strategies are enabled by programming a valid password (16-bit non-one value) via Bootstrap Loader (BSL) mode 6.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in Table 4.

Table 4 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 13 of password = 0	Bit 13 of password = 1 MSB of password = 0	Bit 13 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible

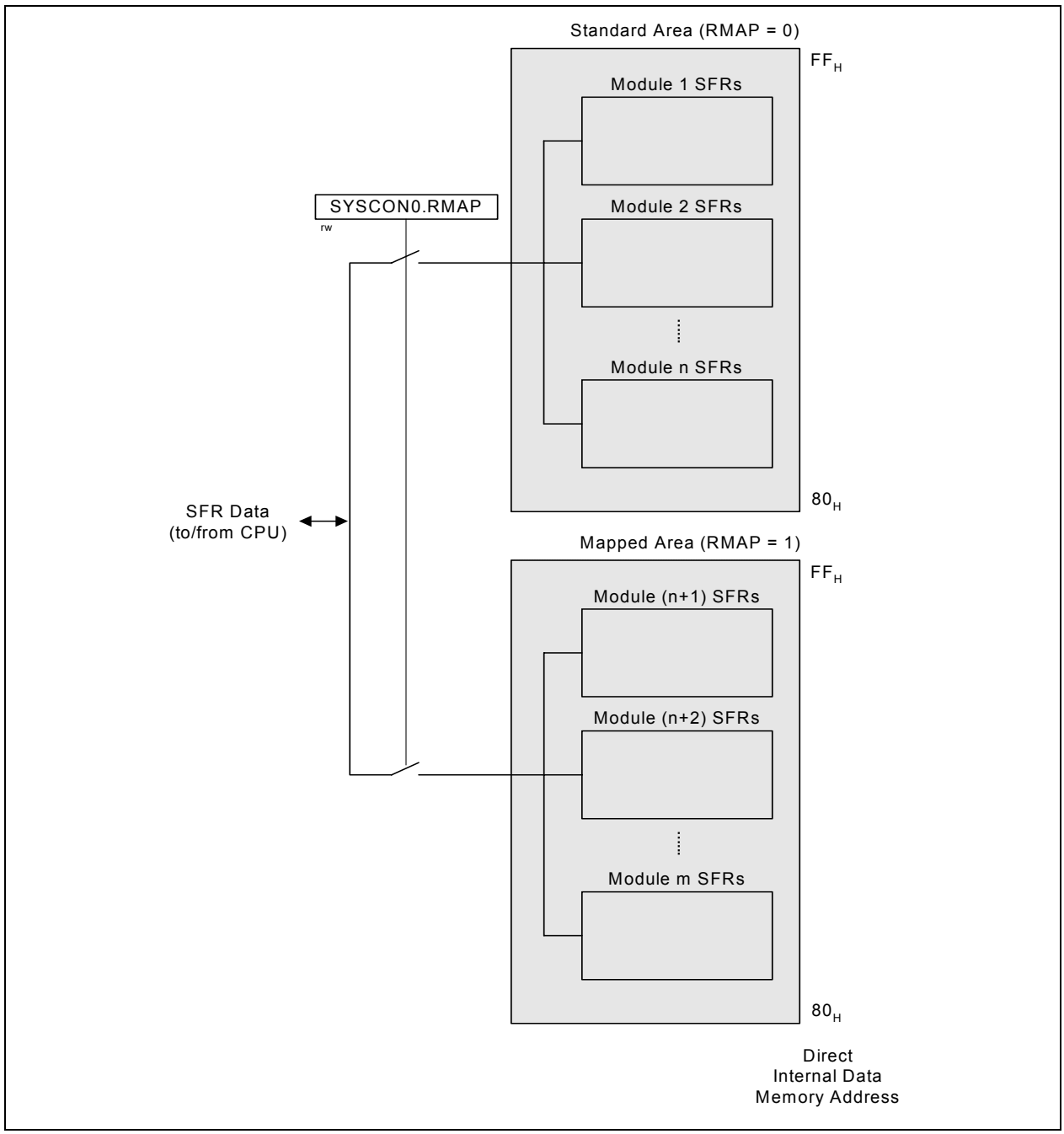

Figure 9 Address Extension by Mapping

3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB_H	**WDTCON** **Reset: 00_H** Watchdog Timer Control Register	Bit Field	0		WINBEN	WDTPR	0	WDTEN	WDTRS	WDTIN
		Type	r		rw	rh	r	rw	rwh	rw
BC_H	**WDTREL** **Reset: 00_H** Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD_H	**WDTWINB** **Reset: 00_H** Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_DATA** **Reset: 00_H** P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
93_H	**P5_DIR** **Reset: 00_H** P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CB_H	**ADC_RCR1 Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2 Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3 Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA_H	**ADC_CHINFR Reset: 00_H** Channel Interrupt Flag Register	Bit Field	CHINF7	CHINF6	CHINF5	CHINF4	CHINF3	CHINF2	CHINF1	CHINF0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB_H	**ADC_CHINCR Reset: 00_H** Channel Interrupt Clear Register	Bit Field	CHINC7	CHINC6	CHINC5	CHINC4	CHINC3	CHINC2	CHINC1	CHINC0
		Type	w	w	w	w	w	w	w	w
CC_H	**ADC_CHINSR Reset: 00_H** Channel Interrupt Set Register	Bit Field	CHINS7	CHINS6	CHINS5	CHINS4	CHINS3	CHINS2	CHINS1	CHINS0
		Type	w	w	w	w	w	w	w	w
CD_H	**ADC_CHINPR Reset: 00_H** Channel Interrupt Node Pointer Register	Bit Field	CHINP7	CHINP6	CHINP5	CHINP4	CHINP3	CHINP2	CHINP1	CHINP0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE_H	**ADC_EVINFR Reset: 00_H** Event Interrupt Flag Register	Bit Field	EVINF7	EVINF6	EVINF5	EVINF4	0		EVINF1	EVINF0
		Type	rh	rh	rh	rh	r		rh	rh
CF_H	**ADC_EVINCR Reset: 00_H** Event Interrupt Clear Flag Register	Bit Field	EVINC7	EVINC6	EVINC5	EVINC4	0		EVINC1	EVINC0
		Type	w	w	w	w	r		w	w
$D2_H$	**ADC_EVINSR Reset: 00_H** Event Interrupt Set Flag Register	Bit Field	EVINS7	EVINS6	EVINS5	EVINS4	0		EVINS1	EVINS0
		Type	w	w	w	w	r		w	w
$D3_H$	**ADC_EVINPR Reset: 00_H** Event Interrupt Node Pointer Register	Bit Field	EVINP7	EVINP6	EVINP5	EVINP4	0		EVINP1	EVINP0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA_H	**ADC_CRCR1 Reset: 00_H** Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB_H	**ADC_CRPR1 Reset: 00_H** Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			

Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T2CCU_CCTH Reset: 00_H** T2CCU Capture/Compare Timer Register High	Bit Field	CCT							
		Type	rwh							
$C6_H$	**T2CCU_CCTCON Reset: 00_H** T2CCU CaptureCcompare Timer Control Register	Bit Field	CCTPRE				CCTOVF	CCTOVEN	TIMSYN	CCTST
		Type	rw				rwh	rw	rw	rw
RMAP = 0, PAGE 2										
$C0_H$	**T2CCU_COSHDWReset: 00_H** T2CCU Capture/compare Enable Register	Bit Field	ENSHDW	TXOV	COOUT5	COOUT4	COOUT3	COOUT2	COOUT1	COOUT0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$C1_H$	**T2CCU_CC0L Reset: 00_H** T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC0H Reset: 00_H** T2CCU Capture/compare Register 0 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC1L Reset: 00_H** T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC1H Reset: 00_H** T2CCU Capture/compare Register 1 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC2L Reset: 00_H** T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC2H Reset: 00_H** T2CCU Capture/compare Register 2 High	Bit Field	CCVALH							
		Type	rwh							
RMAP = 0, PAGE 3										
$C0_H$	**T2CCU_COCON Reset: 00_H** T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD	
		Type	rw	rw	rwh	rwh	rw	rw	rw	
$C1_H$	**T2CCU_CC3L Reset: 00_H** T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL							
		Type	rwh							
$C2_H$	**T2CCU_CC3H Reset: 00_H** T2CCU Capture/compare Register 3 High	Bit Field	CCVALH							
		Type	rwh							
$C3_H$	**T2CCU_CC4L Reset: 00_H** T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL							
		Type	rwh							
$C4_H$	**T2CCU_CC4H Reset: 00_H** T2CCU Capture/compare Register 4 High	Bit Field	CCVALH							
		Type	rwh							
$C5_H$	**T2CCU_CC5L Reset: 00_H** T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL							
		Type	rwh							
$C6_H$	**T2CCU_CC5H Reset: 00_H** T2CCU Capture/compare Register 5 High	Bit Field	CCVALH							
		Type	rwh							

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The pagination of the Flash memory allows each page to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width
- of 1-byte for D-Flash and 2-bytes for P-Flash
- 1-page minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all ones)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: 1 × t_{CCLK} = 38 ns[1)]
- Program time for 1 wordline: 1.6 ms[2)]
- Page erase time: 20 ms
- Mass erase time: 200 ms

1) Values shown here are typical values. f_{sys} = 144 MHz ± 7.5% (f_{CCLK} = 24 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

2) Values shown here are typical values. f_{sys} = 144 MHz ± 7.5% (f_{CCLK} = 24 MHz ± 7.5 %) is the typical frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

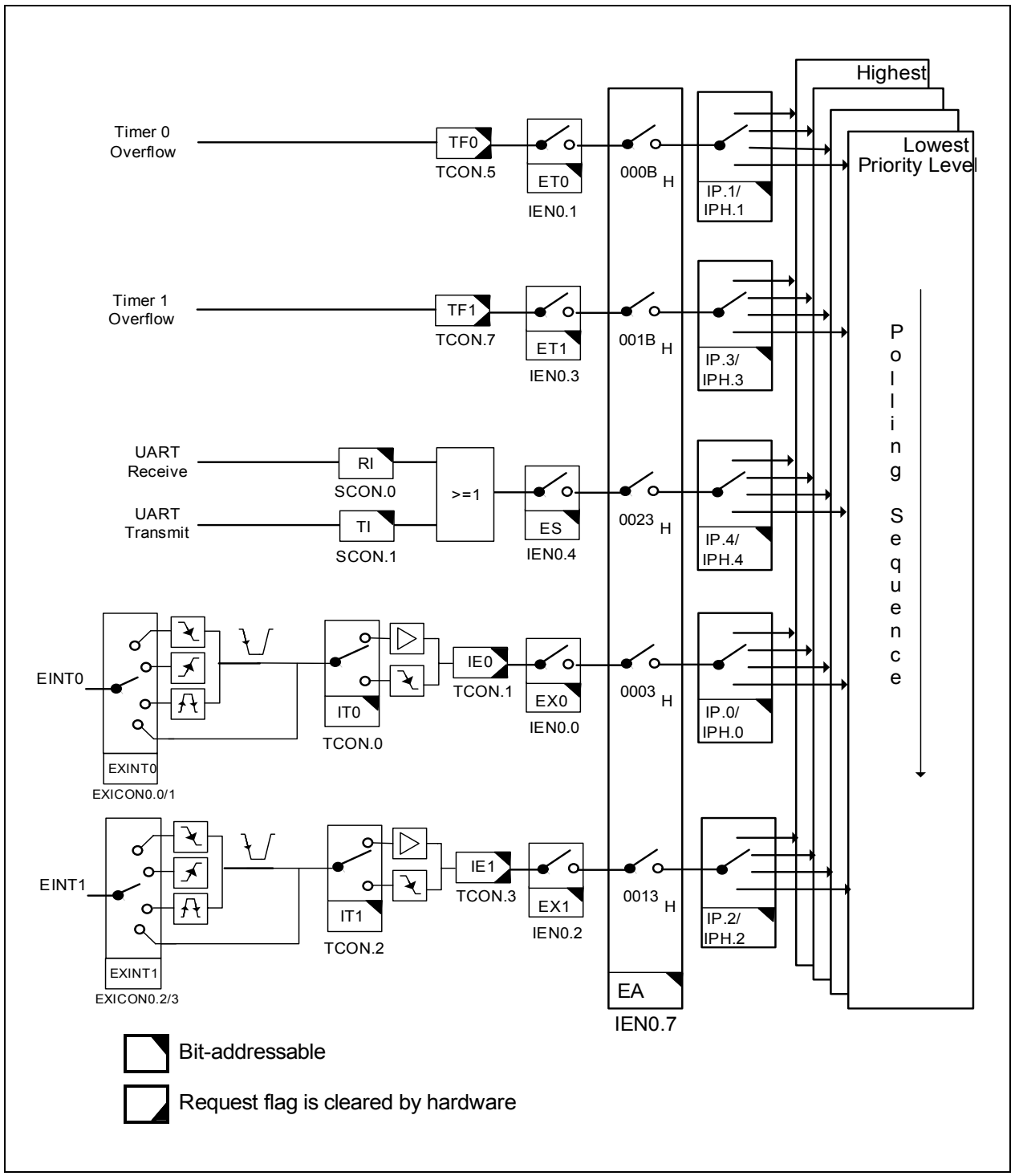

Figure 13 Interrupt Request Sources (Part 1)

Figure 18 shows the structure of a bidirectional port pin.

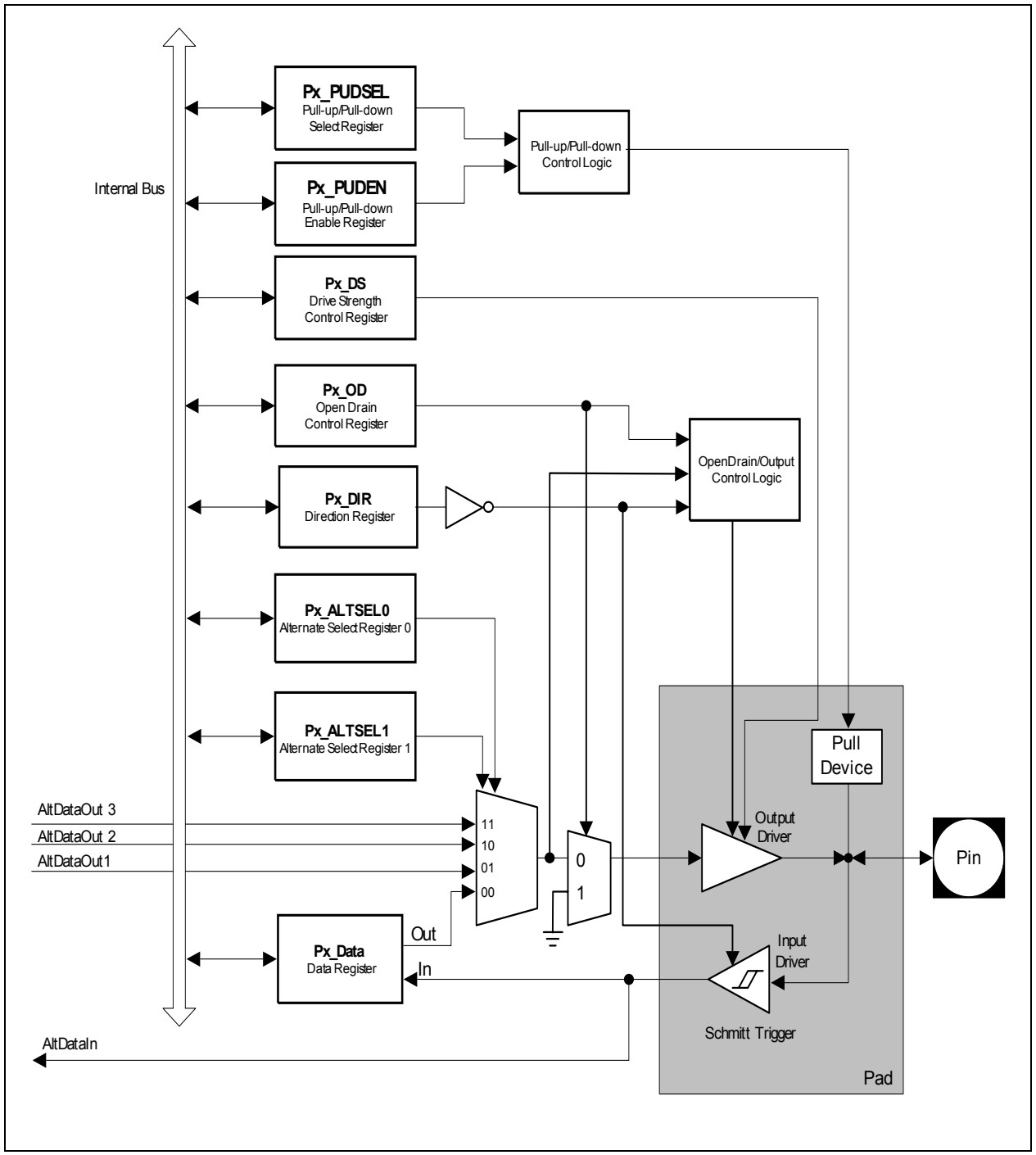

Figure 18 General Structure of Bidirectional Port

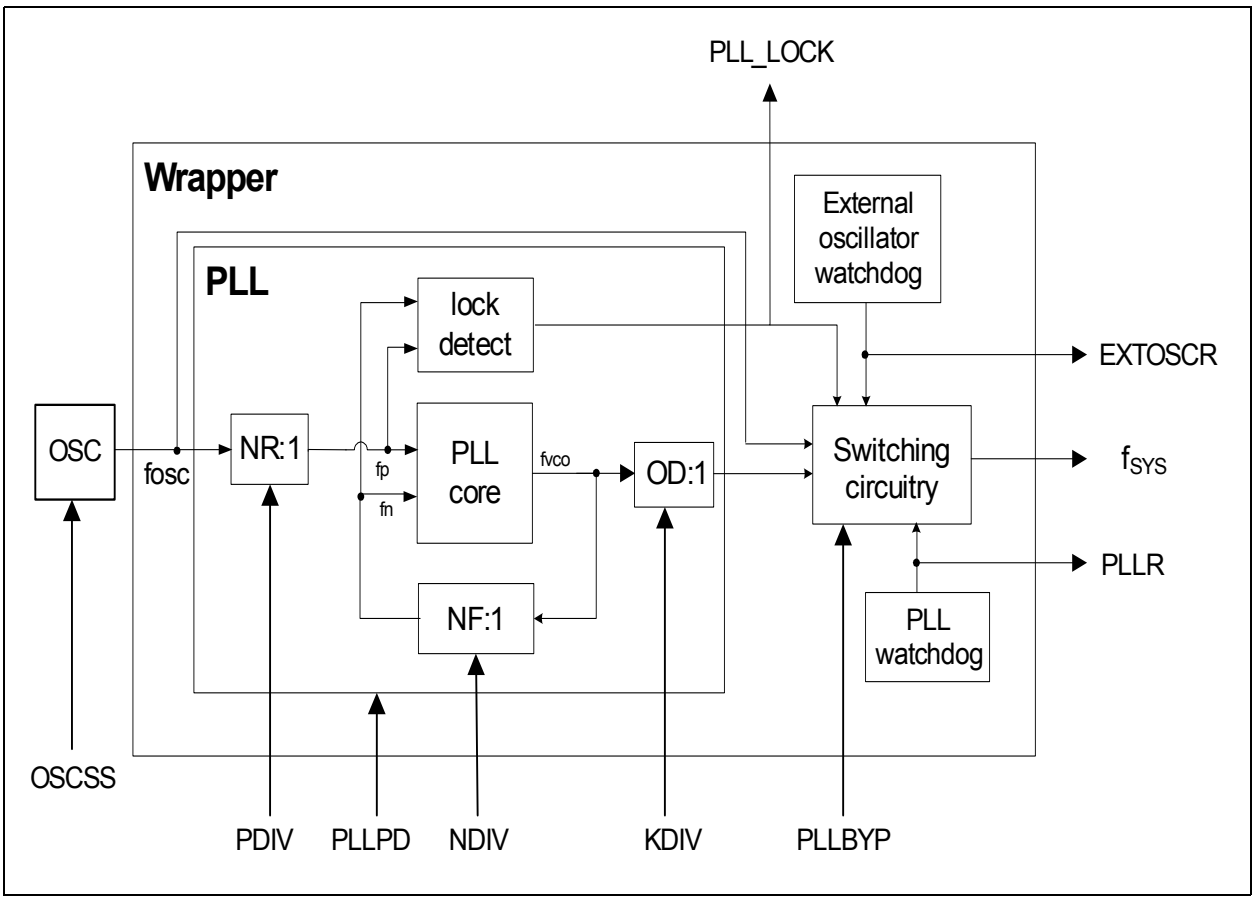

Figure 20 CGU Block Diagram

Direct Drive (PLL Bypass Operation)

During PLL bypass operation, the system clock has the same frequency as the external clock source.

(3.1)

$$f_{SYS} = f_{OSC}$$

PLL Mode

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC87x system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC87x will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 24** shows the block diagram of the WDT unit.

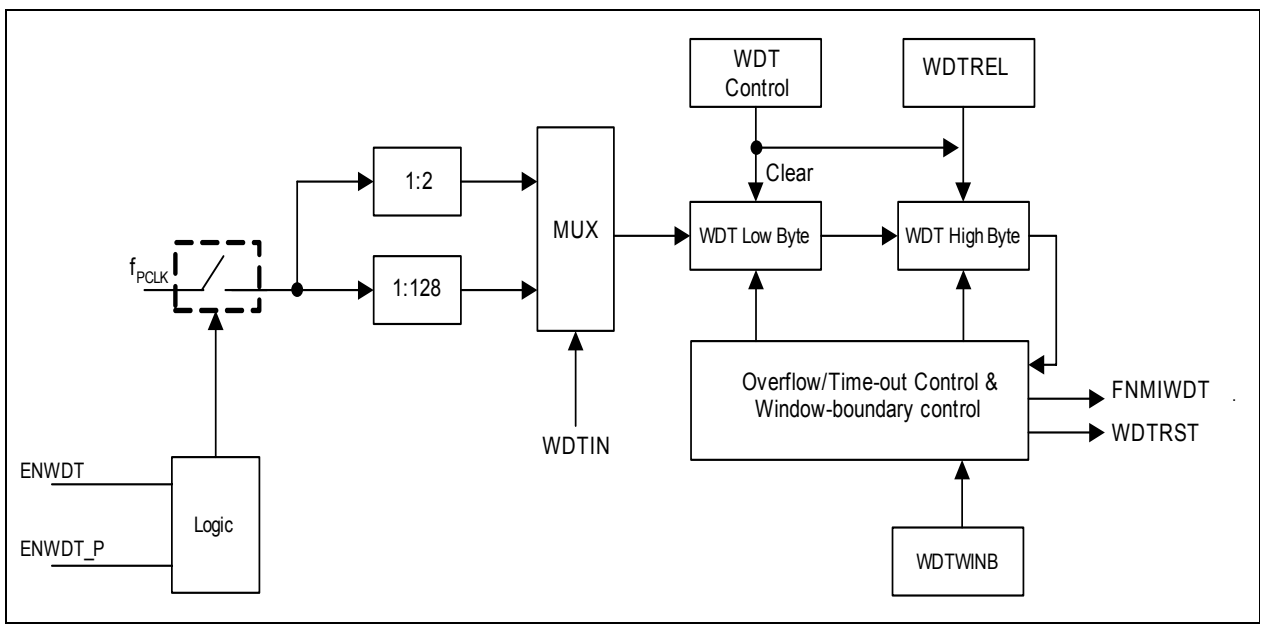

Figure 24 WDT Block Diagram

– Interrupt enabling and corresponding flag

3.13 UART and UART1

The XC87x provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
  – 8-bit or 9-bit data frames, LSB first
  – Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 30**.

Table 30 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$[1)]
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and

4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC87x. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 39 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
CPU Clock Frequency[1)]	f_{CCLK}		26.67[2)]	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC878/874...
		-40	105	°C	SAX-XC878...
		-40	125	°C	SAK-XC878/874...

1) f_{CCLK} is the input frequency to the XC800 core. Please refer to **Figure 22** for detailed description.

2)Default setting of f_{CCLK} upon reset is 24 MHz.

Table 40 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR	–	25	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	150	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	200	mA	5)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	200	mA	5)
V_{DDP} = 3.3 V Range						
Output low voltage	V_{OL}	CC	–	0.5	V	I_{OL} = 6 mA (DS = 0)[1)] I_{OL} = 8 mA (DS = 1)[2)]
Output high voltage	V_{OH}	CC	2.2	–	V	I_{OH} = -5 mA (DS = 0)[1)] I_{OH} = -7 mA (DS = 1)[2)]
Input low voltage	V_{IL}	SR	-0.3	0.7	V	CMOS Mode
Input high voltage	V_{IH}	SR	2	V_{DDP}	V	CMOS Mode
Input Hysteresis	HYS	CC	0.28	–	V	CMOS Mode[3)7)]
Input low voltage at XTAL1	V_{ILX}	SR	-0.3	0.7	V	
Input high voltage at XTAL1	V_{IHX}	SR	2.3	V_{DDP}	V	
Pull-up current	I_{PU}	SR	–	-7	µA	$V_{IH,min}$
			-35	–	µA	$V_{IL,max}$
Pull-down current	I_{PD}	SR	–	12	µA	$V_{IL,max}$
			60	–	µA	$V_{IH,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105°C$[4)]
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	5)

4.2.2 Supply Threshold Characteristics

Table 41 provides the characteristics of the supply threshold in the XC87x.

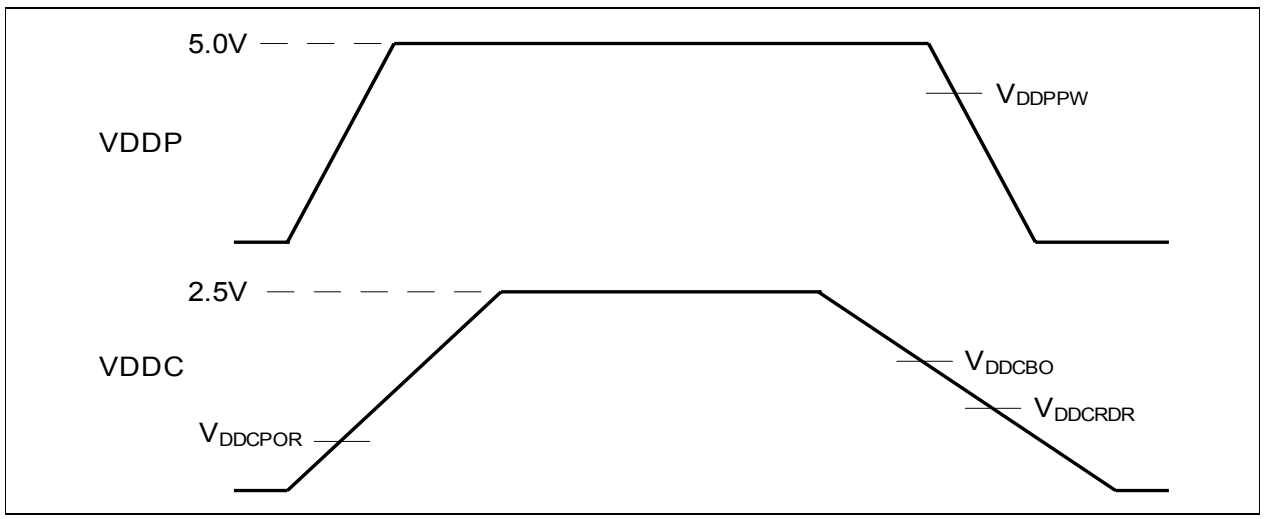

Figure 34 Supply Threshold Parameters

Table 41 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} brownout voltage[1)]	V_{DDCBO}	CC	1.7	1.9	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	1.2	–	–	V
V_{DDP} prewarning voltage[2)]	V_{DDPPW}	CC	3.8	4.2	4.5	V
Power-on reset voltage[1)3)]	V_{DDCPOR}	CC	1.7	1.9	2.2	V

1) Detection is enabled in both active and power-down mode.

2) Detection is enabled for 5.0V power supply variant.
Detection is disabled for 3.3V power supply variant.

3) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

Table 44 Power Down Current[1](Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ.[2]	max.[3]		
V_{DDP} = 5V Range					
Power-Down Mode	I_{PDP}	20	80	µA	T_A = + 25 °C[4][5]
		-	250	µA	T_A = + 85 °C[5][6]

1) The table is only applicable to SAF and SAX variants. SAK variant does not support power-down mode

2) The typical I_{PDP} values are based on preliminary measurements and are to be used as reference only. These values are measured at V_{DDP} = 5.0 V.

3) The maximum I_{PDP} values are measured at V_{DDP} = 5.5 V.

4) I_{PDP} has a maximum value of 450 µA at T_A = + 105 °C.

5) I_{PDP} is measured with: $\overline{\text{RESET}}$ = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0 = V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

6) Not subjected to production test, verified by design/characterization.

4.3.3 Power-on Reset and PLL Timing

Table 48 provides the characteristics of the power-on reset and PLL timing in the XC87x.

Table 48 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
On-Chip Oscillator start-up time	t_{OSCST}	CC	–	–	500	ns	1)
PLL lock-in in time	t_{LOCK}	CC	–	–	200	µs	1)
PLL accumulated jitter	D_P		–	–	1.8	ns	1)2)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) PLL lock at 144 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 72 and P = 1.

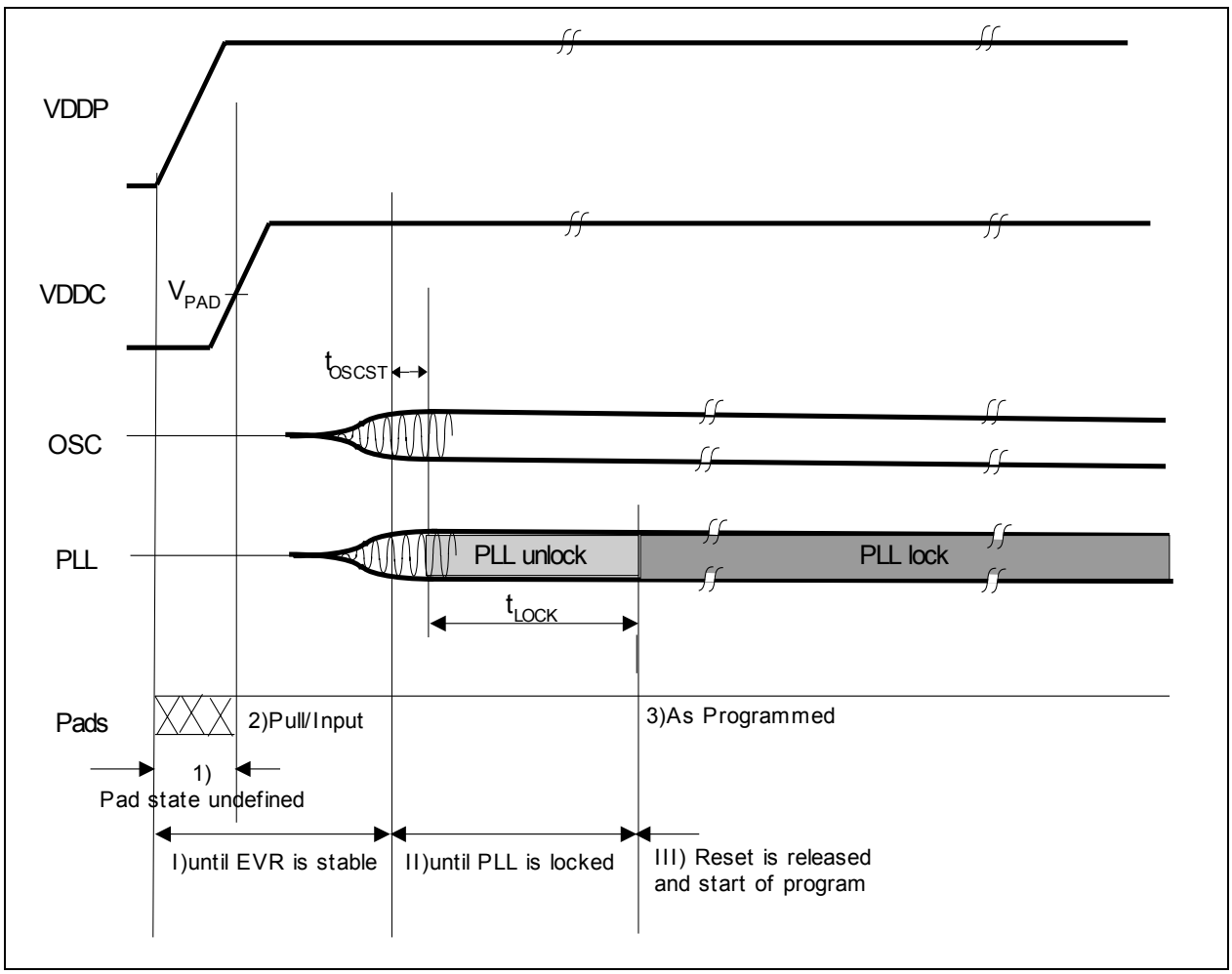

Figure 40 Power-on Reset Timing

5.3 Quality Declaration

Table 57 shows the characteristics of the quality parameters in the XC87x.

Table 57 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the two stated T_J 1)	t_{OP1}	-	15000	hours	T_J = 110°C
		-	2000	hours	T_J = -40°C
Operation Lifetime when the device is used at the five stated T_J 1)	t_{OP2}	-	120	hours	T_J = 140°C
		-	960	hours	T_J = 135°C
		-	7800	hours	T_J = 91°C
		-	2400	hours	T_J = 38°C
		-	720	hours	T_J = -25°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	750	V	Conforming to JESD22-C101-C

1) This lifetime refers only to the time when device is powered-on.