# Infineon Technologies - XC878CM16FFA5VACXXUMA1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 27MHz |
| Connectivity | CANbus, SPI, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | PG-LQFP-64-4 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc878cm16ffa5vacxxuma1 |

**Table 2 Device Profile** (cont'd)

| Sales Type | Device Type | Program Memory (Kbytes) | Power Supply (V) | Temp-erature (°C) | Quality Profile |
|---|---|---|---|---|---|
| SAF-XC874CM-16FVA 5V | Flash | 64 | 5.0 | -40 to 85 | Automotive |
| SAF-XC874CM-13FVA 5V | Flash | 52 | 5.0 | -40 to 85 | Automotive |
| SAK-XC874LM-16FVA 5V | Flash | 64 | 5.0 | -40 to 125 | Automotive |
| SAK-XC874CM-16FVA 5V | Flash | 64 | 5.0 | -40 to 125 | Automotive |
| SAK-XC874-16FVA 5V | Flash | 64 | 5.0 | -40 to 125 | Automotive |
| SAK-XC874LM-13FVA 5V | Flash | 52 | 5.0 | -40 to 125 | Automotive |
| SAK-XC874CM-13FVA 5V | Flash | 52 | 5.0 | -40 to 125 | Automotive |
| SAK-XC874-13FVA 5V | Flash | 52 | 5.0 | -40 to 125 | Automotive |

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC87x throughout this document.

### Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC87x, please refer to your responsible sales representative or your local distributor.

## 2.2 Logic Symbol

The logic symbols of the XC878 and XC874 are shown in **Figure 3**.

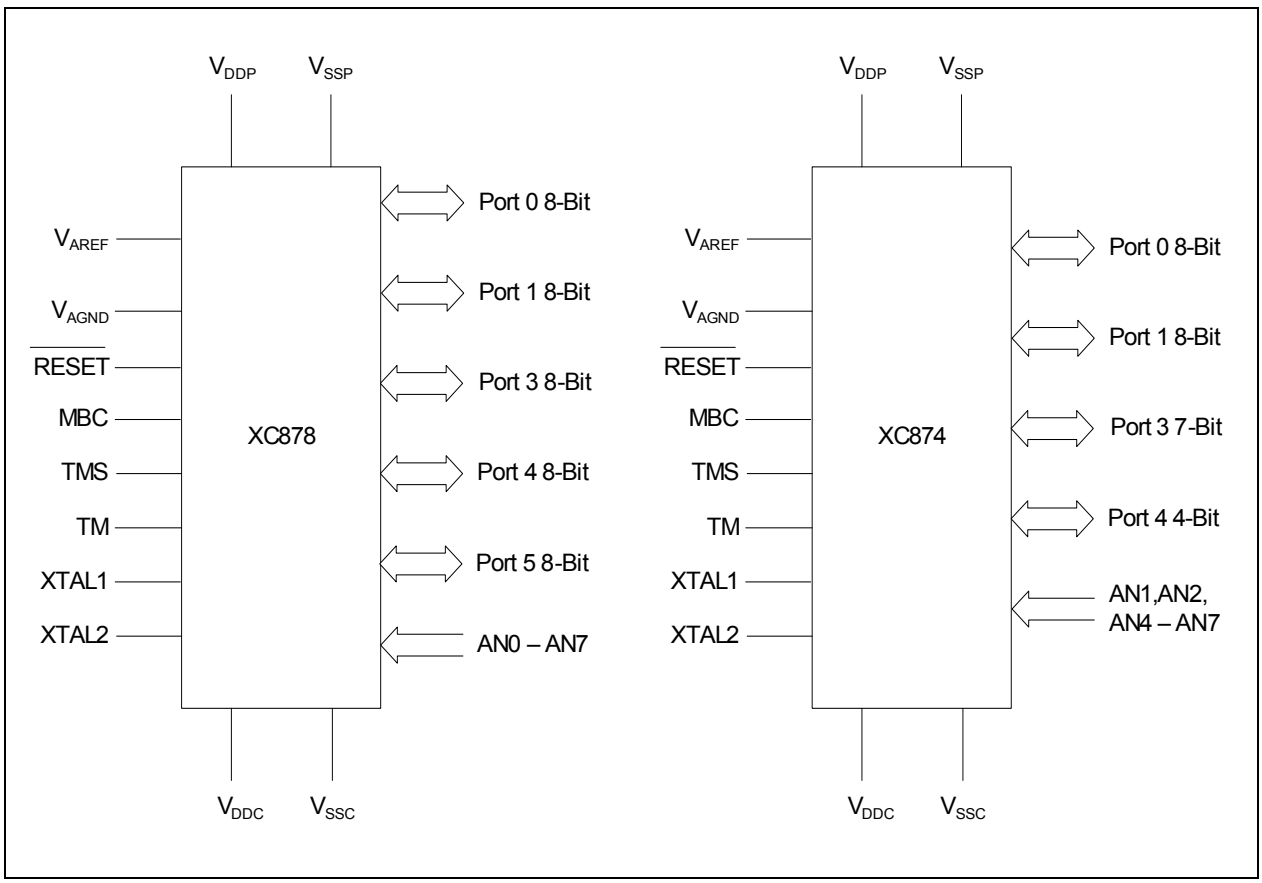



**Figure 3 XC878 and XC874 Logic Symbol**

### 3.2.1 Memory Protection Strategy

The XC87x memory protection strategy includes:

- Basic protection: The user is able to block any external access via the boot option to any memory
- Read-out protection: The user is able to protect the contents in the Flash
- Flash program and erase protection

These protection strategies are enabled by programming a valid password (16-bit non-one value) via Bootstrap Loader (BSL) mode 6.

#### 3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in Table 4.

**Table 4 Flash Protection Modes**

| Flash Protection | Without hardware protection | With hardware protection | |
|---|---|---|---|
| **Hardware Protection Mode** | - | 0 | 1 |
| **Activation** | Program a valid password via BSL mode 6 | | |
| **Selection** | Bit 13 of password = 0 | Bit 13 of password = 1<br>MSB of password = 0 | Bit 13 of password = 1<br>MSB of password = 1 |
| **P-Flash contents can be read by** | Read instructions in any program memory | Read instructions in the P-Flash | Read instructions in the P-Flash or D-Flash |
| **External access to P-Flash** | Not possible | Not possible | Not possible |

**SYSCON0**
**System Control Register 0** **Reset Value: $04_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | **0** | | **IMODE** | **0** | **1** | **0** | **RMAP** |
| | r | | rw | r | r | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RMAP** | 0 | rw | **Interrupt Node XINTR0 Enable**<br>0 The access to the standard SFR area is enabled<br>1 The access to the mapped SFR area is enabled |
| **1** | 2 | r | **Reserved**<br>Returns 1 if read; should be written with 1. |
| **0** | [7:5], 3,1 | r | **Reserved**<br>Returns 0 if read; should be written with 0. |

*Note: The RMAP bit should be cleared/set by ANL or ORL instructions.The rest bits of SYSCON0 should not be modified.*

### 3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC87x has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 10**.

- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

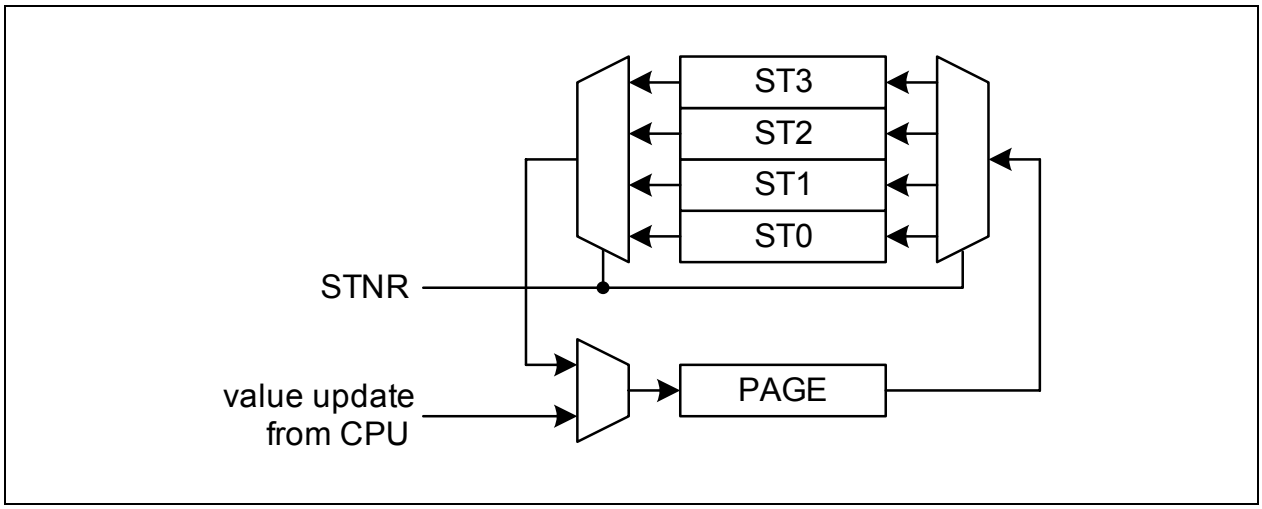



**Figure 11 Storage Elements for Paging**

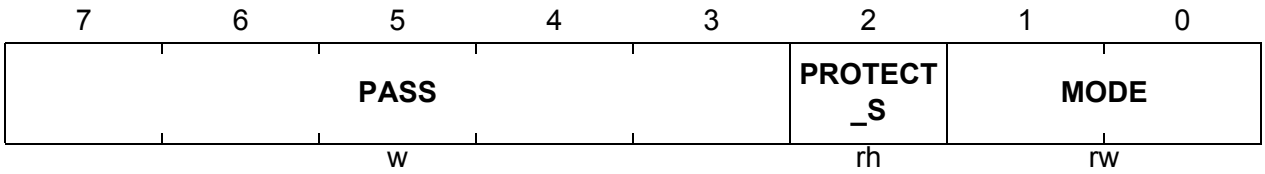
With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC87x supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

### 3.2.3.1 Password Register

**PASSWD**
**Password Register** **Reset Value: $07_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **MODE** | [1:0] | rw | **Bit Protection Scheme Control Bits**<br>00 Scheme disabled - direct access to the protected bits is allowed.<br>11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default)<br>Others:Scheme Enabled.<br>These two bits cannot be written directly. To change the value between $11_B$ and $00_B$, the bit field PASS must be written with $11000_B$; only then, will the MODE[1:0] be registered. |
| **PROTECT_S** | 2 | rh | **Bit Protection Signal Status Bit**<br>This bit shows the status of the protection.<br>0 Software is able to write to all protected bits.<br>1 Software is unable to write to any protected bits. |
| **PASS** | [7:3] | w | **Password Bits**<br>The Bit Protection Scheme only recognizes three patterns.<br>$11000_B$ Enables writing of the bit field MODE.<br>$10011_B$ Opens access to writing of all protected bits.<br>$10101_B$ Closes access to writing of all protected bits |

**Table 5 CPU Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $97_H$ | **MEXSP** **Reset: $7F_H$** Memory Extension Stack Pointer Register | Bit Field | 0 | MXSP | | | | | | |
| | | Type | r | rwh | | | | | | |
| **$98_H$** | **SCON** **Reset: $00_H$** Serial Channel Control Register | Bit Field | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| | | Type | rw | rw | rw | rw | rw | rwh | rwh | rwh |
| $99_H$ | **SBUF** **Reset: $00_H$** Serial Data Buffer Register | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $A2_H$ | **EO** **Reset: $00_H$** Extended Operation Register | Bit Field | 0 | | | TRAP_EN | 0 | | | DPSEL0 |
| | | Type | r | | | rw | r | | | rw |
| **$A8_H$** | **IEN0** **Reset: $00_H$** Interrupt Enable Register 0 | Bit Field | EA | 0 | ET2 | ES | ET1 | EX1 | ET0 | EX0 |
| | | Type | rw | r | rw | rw | rw | rw | rw | rw |
| **$B8_H$** | **IP** **Reset: $00_H$** Interrupt Priority Register | Bit Field | 0 | | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
| | | Type | r | | rw | rw | rw | rw | rw | rw |
| $B9_H$ | **IPH** **Reset: $00_H$** Interrupt Priority High Register | Bit Field | 0 | | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |
| | | Type | r | | rw | rw | rw | rw | rw | rw |
| **$D0_H$** | **PSW** **Reset: $00_H$** Program Status Word Register | Bit Field | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| | | Type | rwh | rwh | rw | rw | rw | rwh | rw | rh |
| **$E0_H$** | **ACC** **Reset: $00_H$** Accumulator Register | Bit Field | ACC7 | ACC6 | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 | ACC0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$E8_H$** | **IEN1** **Reset: $00_H$** Interrupt Enable Register 1 | Bit Field | ECCIP3 | ECCIP2 | ECCIP1 | ECCIP0 | EXM | EX2 | ESSC | EADC |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$F0_H$** | **B** **Reset: $00_H$** B Register | Bit Field | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$F8_H$** | **IP1** **Reset: $00_H$** Interrupt Priority 1 Register | Bit Field | PCCIP3 | PCCIP2 | PCCIP1 | PCCIP0 | PXM | PX2 | PSSC | PADC |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $F9_H$ | **IPH1** **Reset: $00_H$** Interrupt Priority 1 High Register | Bit Field | PCCIP3H | PCCIP2H | PCCIP1H | PCCIP0H | PXMH | PX2H | PSSCH | PADCH |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |

### 3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 6 MDU Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| **$B0_H$** | **MDUSTAT** **Reset: $00_H$** MDU Status Register | Bit Field | 0 | | | | | BSY | IERR | IRDY |
| | | Type | r | | | | | rh | rwh | rwh |

**Table 8 SCU Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $B7_H$ | **EXICON0** **Reset: $F0_H$** External Interrupt Control Register 0 | Bit Field | EXINT3 | | EXINT2 | | EXINT1 | | EXINT0 | |
| | | Type | rw | | rw | | rw | | rw | |
| $BA_H$ | **EXICON1** **Reset: $3F_H$** External Interrupt Control Register 1 | Bit Field | 0 | | EXINT6 | | EXINT5 | | EXINT4 | |
| | | Type | r | | rw | | rw | | rw | |
| $BB_H$ | **NMICON** **Reset: $00_H$** NMI Control Register | Bit Field | 0 | NMI ECC | NMI VDDP | 0 | NMI OCDS | NMI FLASH | NMI PLL | NMI WDT |
| | | Type | r | rw | rw | r | rw | rw | rw | rw |
| $BC_H$ | **NMISR** **Reset: $00_H$** NMI Status Register | Bit Field | 0 | FNMI ECC | FNMI VDDP | 0 | FNMI OCDS | FNMI FLASH | FNMI PLL | FNMI WDT |
| | | Type | r | rwh | rwh | r | rwh | rwh | rwh | rwh |
| $BD_H$ | **BCON** **Reset: $20_H$** Baud Rate Control Register | Bit Field | BGSEL | | NDOV EN | BRDIS | BRPRE | | | R |
| | | Type | rw | | rw | rw | rw | | | rw |
| $BE_H$ | **BG** **Reset: $00_H$** Baud Rate Timer/Reload Register | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rwh | | | | | | | |
| $E9_H$ | **FDCON** **Reset: $00_H$** Fractional Divider Control Register | Bit Field | BGS | SYNE N | ERRS YN | EOFS YN | BRK | NDOV | FDM | FDEN |
| | | Type | rw | rw | rwh | rwh | rwh | rwh | rw | rw |
| $EA_H$ | **FDSTEP** **Reset: $00_H$** Fractional Divider Reload Register | Bit Field | STEP | | | | | | | |
| | | Type | rw | | | | | | | |
| $EB_H$ | **FDRES** **Reset: $00_H$** Fractional Divider Result Register | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |
| RMAP = 0, PAGE 1 | | | | | | | | | | |
| $B3_H$ | **ID** **Reset: $49_H$** Identity Register | Bit Field | PRODID | | | | | VERID | | |
| | | Type | r | | | | | r | | |
| $B4_H$ | **PMCON0** **Reset: $80_H$** Power Mode Control Register 0 | Bit Field | VDDP WARN | WDT RST | WKRS | WK SEL | SD | PD | WS | |
| | | Type | rh | rwh | rwh | rw | rw | rwh | rw | |
| $B5_H$ | **PMCON1** **Reset: $00_H$** Power Mode Control Register 1 | Bit Field | 0 | CDC_ DIS | CAN_ DIS | MDU_ DIS | T2CC U_DIS | CCU_ DIS | SSC_ DIS | ADC_ DIS |
| | | Type | r | rw | rw | rw | rw | rw | rw | rw |
| $B6_H$ | **OSC_CON** **Reset: $XX_H$** OSC Control Register | Bit Field | PLLRD RES | PLLBY P | PLLPD | 0 | XPD | OSC SS | EORD RES | EXTO SCR |
| | | Type | rwh | rwh | rw | r | rw | rwh | rwh | rh |
| $B7_H$ | **PLL_CON** **Reset: $18_H$** PLL Control Register | Bit Field | NDIV | | | | | | PLLR | PLL_L OCK |
| | | Type | rw | | | | | | rh | rh |
| $BA_H$ | **CMCON** **Reset: $10_H$** Clock Control Register | Bit Field | KDIV | | 0 | FCCF G | CLKREL | | | |
| | | Type | rw | | r | rw | rw | | | |

**Table 8 SCU Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $BB_H$ | **PASSWD** **Reset: $07_H$**<br>Password Register | Bit Field | PASS | | | | | PROTECT_S | MODE | |
| | | Type | w | | | | | rh | rw | |
| $BE_H$ | **COCON** **Reset: $00_H$**<br>Clock Output Control Register | Bit Field | COUTS | | TLEN | 0 | COREL | | | |
| | | Type | rw | | rw | r | rw | | | |
| $E9_H$ | **MISC_CON** **Reset: $00_H$**<br>Miscellaneous Control Register | Bit Field | ADCETR0_MUX | ADCETR1_MUX | 0 | | | | | DFLASHEN |
| | | Type | rw | rw | r | | | | | rwh |
| $EA_H$ | **PLL_CON1** **Reset: $20_H$**<br>PLL Control Register 1 | Bit Field | NDIV | | PDIV | | | | | |
| | | Type | rw | | rw | | | | | |
| $EB_H$ | **CR_MISC** **Reset: $00_H$ or $01_H$**<br>Reset Status Register | Bit Field | CCCFG | MDUCCFG | CCUCCFG | T2CCFG | 0 | | | HDRST |
| | | Type | rw | rw | rw | rw | r | | | rwh |
| RMAP = 0, PAGE 3 | | | | | | | | | | |
| $B3_H$ | **XADDRH** **Reset: $F0_H$**<br>On-chip XRAM Address Higher Order | Bit Field | ADDRH | | | | | | | |
| | | Type | rw | | | | | | | |
| $B4_H$ | **IRCON3** **Reset: $00_H$**<br>Interrupt Request Register 3 | Bit Field | 0 | | CANSRC5 | CCU6SR1 | 0 | | CANSRC4 | CCU6SR0 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B5_H$ | **IRCON4** **Reset: $00_H$**<br>Interrupt Request Register 4 | Bit Field | 0 | | CANSRC7 | CCU6SR3 | 0 | | CANSRC6 | CCU6SR2 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B6_H$ | **MODIEN** **Reset: $07_H$**<br>Peripheral Interrupt Enable Register | Bit Field | 0 | | | CM5EN | CM4EN | RIREN | TIREN | EIREN |
| | | Type | r | | | rw | rw | rw | rw | rw |
| $B7_H$ | **MODPISEL1** **Reset: $00_H$**<br>Peripheral Input Select Register 1 | Bit Field | EXINT6IS | | | UR1RIS | | T21EXIS | 0 | |
| | | Type | rw | | | rw | | rw | r | |
| $BA_H$ | **MODPISEL2** **Reset: $00_H$**<br>Peripheral Input Select Register 2 | Bit Field | 0 | | | T2EXIS | T21IS | T2IS | T1IS | T0IS |
| | | Type | r | | | rw | rw | rw | rw | rw |
| $BB_H$ | **PMCON2** **Reset: $00_H$**<br>Power Mode Control Register 2 | Bit Field | 0 | | | | | | UART1_DIS | T21_DIS |
| | | Type | r | | | | | | rw | rw |
| $BD_H$ | **MODSUSP** **Reset: $01_H$**<br>Module Suspend Control Register | Bit Field | 0 | | CCTSUSP | T21SUSP | T2SUSP | T13SUSP | T12SUSP | WDTSUSP |
| | | Type | r | | rw | rw | rw | rw | rw | rw |
| $BE_H$ | **MODPISEL3** **Reset: $00_H$**<br>Peripheral Input Select Register 3 | Bit Field | 0 | | CIS | | SIS | | MIS | |
| | | Type | r | | rw | | rw | | rw | |
| $EA_H$ | **MODPISEL4** **Reset: $00_H$**<br>Peripheral Input Select Register 4 | Bit Field | 0 | | EXINT5IS | | EXINT4IS | | EXINT3IS | |
| | | Type | r | | rw | | rw | | rw | |

### 3.2.4.8 Timer 2 Compare/Capture Unit Registers

The Timer 2 Compare/Capture Unit SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 12 T2CCU Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 | | | | | | | | | | |
| $C7_H$ | **T2_PAGE** **Reset: $00_H$** Page Register | Bit Field | OP | | STNR | | 0 | PAGE | | |
| | | Type | w | | w | | r | rwh | | |
| RMAP = 0, PAGE 0 | | | | | | | | | | |
| **$C0_H$** | **T2_T2CON** **Reset: $00_H$** Timer 2 Control Register | Bit Field | TF2 | EXF2 | 0 | | EXEN2 | TR2 | C/$\overline{T2}$ | $\underline{CP/RL2}$ |
| | | Type | rwh | rwh | r | | rw | rwh | rw | rw |
| $C1_H$ | **T2_T2MOD** **Reset: $00_H$** Timer 2 Mode Register | Bit Field | T2REGS | T2RHEN | EDGESEL | PREN | T2PRE | | | DCEN |
| | | Type | rw | rw | rw | rw | rw | | | rw |
| $C2_H$ | **T2_RC2L** **Reset: $00_H$** Timer 2 Reload/Capture Register Low | Bit Field | RC2 | | | | | | | |
| | | Type | rwh | | | | | | | |
| $C3_H$ | **T2_RC2H** **Reset: $00_H$** Timer 2 Reload/Capture Register High | Bit Field | RC2 | | | | | | | |
| | | Type | rwh | | | | | | | |
| $C4_H$ | **T2_T2L** **Reset: $00_H$** Timer 2 Register Low | Bit Field | THL2 | | | | | | | |
| | | Type | rwh | | | | | | | |
| $C5_H$ | **T2_T2H** **Reset: $00_H$** Timer 2 Register High | Bit Field | THL2 | | | | | | | |
| | | Type | rwh | | | | | | | |
| $C6_H$ | **T2_T2CON1** **Reset: $03_H$** Timer 2 Control Register 1 | Bit Field | 0 | | | | | | TF2EN | EXF2EN |
| | | Type | r | | | | | | rw | rw |
| RMAP = 0, PAGE 1 | | | | | | | | | | |
| $C0_H$ | **T2CCU_CCEN** **Reset: $00_H$** T2CCU Capture/Compare Enable Register | Bit Field | CCM3 | | CCM2 | | CCM1 | | CCM0 | |
| | | Type | rw | | rw | | rw | | rw | |
| $C1_H$ | **T2CCU_CCTBSELReset: $00_H$** T2CCU Capture/Compare Time Base Select Register | Bit Field | CASC | CCTTOV | CCTB5 | CCTB4 | CCTB3 | CCTB2 | CCTB1 | CCTB0 |
| | | Type | rw | rwh | rw | rw | rw | rw | rw | rw |
| $C2_H$ | **T2CCU_CCTRELLReset: $00_H$** T2CCU Capture/Compare Timer Reload Register Low | Bit Field | CCTREL | | | | | | | |
| | | Type | rw | | | | | | | |
| $C3_H$ | **T2CCU_CCTRELHReset: $00_H$** T2CCU Capture/Compare Timer Reload Register High | Bit Field | CCTREL | | | | | | | |
| | | Type | rw | | | | | | | |
| $C4_H$ | **T2CCU_CCTL** **Reset: $00_H$** T2CCU Capture/Compare Timer Register Low | Bit Field | CCT | | | | | | | |
| | | Type | rwh | | | | | | | |

**Table 14 CCU6 Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $FD_H$ | **CCU6_MODCTRH Reset: $00_H$** Modulation Control Register High | Bit Field | ECT13O | 0 | T13MODEN | | | | | |
| | | Type | rw | r | rw | | | | | |
| $FE_H$ | **CCU6_TRPCTRL Reset: $00_H$** Trap Control Register Low | Bit Field | 0 | | | | | TRPM2 | TRPM1 | TRPM0 |
| | | Type | r | | | | | rw | rw | rw |
| $FF_H$ | **CCU6_TRPCTRH Reset: $00_H$** Trap Control Register High | Bit Field | TRPPEN | TRPEN13 | TRPEN | | | | | |
| | | Type | rw | rw | rw | | | | | |
| RMAP = 0, PAGE 3 | | | | | | | | | | |
| $9A_H$ | **CCU6_MCMOUTL Reset: $00_H$** Multi-Channel Mode Output Register Low | Bit Field | 0 | R | MCMP | | | | | |
| | | Type | r | rh | rh | | | | | |
| $9B_H$ | **CCU6_MCMOUTH Reset: $00_H$** Multi-Channel Mode Output Register High | Bit Field | 0 | | CURH | | | EXPH | | |
| | | Type | r | | rh | | | rh | | |
| $9C_H$ | **CCU6_ISL Reset: $00_H$** Capture/Compare Interrupt Status Register Low | Bit Field | T12PM | T12OM | ICC62F | ICC62R | ICC61F | ICC61R | ICC60F | ICC60R |
| | | Type | rh | rh | rh | rh | rh | rh | rh | rh |
| $9D_H$ | **CCU6_ISH Reset: $00_H$** Capture/Compare Interrupt Status Register High | Bit Field | STR | IDLE | WHE | CHE | TRPS | TRPF | T13PM | T13CM |
| | | Type | rh | rh | rh | rh | rh | rh | rh | rh |
| $9E_H$ | **CCU6_PISEL0L Reset: $00_H$** Port Input Select Register 0 Low | Bit Field | ISTRP | | ISCC62 | | ISCC61 | | ISCC60 | |
| | | Type | rw | | rw | | rw | | rw | |
| $9F_H$ | **CCU6_PISEL0H Reset: $00_H$** Port Input Select Register 0 High | Bit Field | IST12HR | | ISPOS2 | | ISPOS1 | | ISPOS0 | |
| | | Type | rw | | rw | | rw | | rw | |
| $A4_H$ | **CCU6_PISEL2 Reset: $00_H$** Port Input Select Register 2 | Bit Field | 0 | | | | | | IST13HR | |
| | | Type | r | | | | | | rw | |
| $FA_H$ | **CCU6_T12L Reset: $00_H$** Timer T12 Counter Register Low | Bit Field | T12CVL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $FB_H$ | **CCU6_T12H Reset: $00_H$** Timer T12 Counter Register High | Bit Field | T12CVH | | | | | | | |
| | | Type | rwh | | | | | | | |
| $FC_H$ | **CCU6_T13L Reset: $00_H$** Timer T13 Counter Register Low | Bit Field | T13CVL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $FD_H$ | **CCU6_T13H Reset: $00_H$** Timer T13 Counter Register High | Bit Field | T13CVH | | | | | | | |
| | | Type | rwh | | | | | | | |
| $FE_H$ | **CCU6_CMPSTATL Reset: $00_H$** Compare State Register Low | Bit Field | 0 | CC63ST | CCPOS2 | CCPOS1 | CCPOS0 | CC62ST | CC61ST | CC60ST |
| | | Type | r | rh | rh | rh | rh | rh | rh | rh |
| $FF_H$ | **CCU6_CMPSTATH Reset: $00_H$** Compare State Register High | Bit Field | T13IM | COUT63PS | COUT62PS | CC62PS | COUT61PS | CC61PS | COUT60PS | CC60PS |
| | | Type | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

### 3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC87x interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in **Table 22**.

**Table 22 Interrupt Vector Addresses**

| Interrupt Source | Vector Address | Assignment for XC87x | Enable Bit | SFR |
|---|---|---|---|---|
| NMI | $0073_H$ | Watchdog Timer NMI | NMIWDT | NMICON |
| | | PLL NMI | NMIPLL | |
| | | Flash Timer NMI | NMIFLASH | |
| | | $V_{DDP}$ Prewarning NMI | NMIVDDP | |
| | | Flash ECC NMI | NMIECC | |
| XINTR0 | $0003_H$ | External Interrupt 0 | EX0 | IEN0 |
| XINTR1 | $000B_H$ | Timer 0 | ET0 | |
| XINTR2 | $0013_H$ | External Interrupt 1 | EX1 | |
| XINTR3 | $001B_H$ | Timer 1 | ET1 | |
| XINTR4 | $0023_H$ | UART | ES | |
| XINTR5 | $002B_H$ | T2CCU | ET2 | |
| | | UART Fractional Divider (Normal Divider Overflow) | | |
| | | MultiCAN Node 0 | | |
| | | LIN | | |

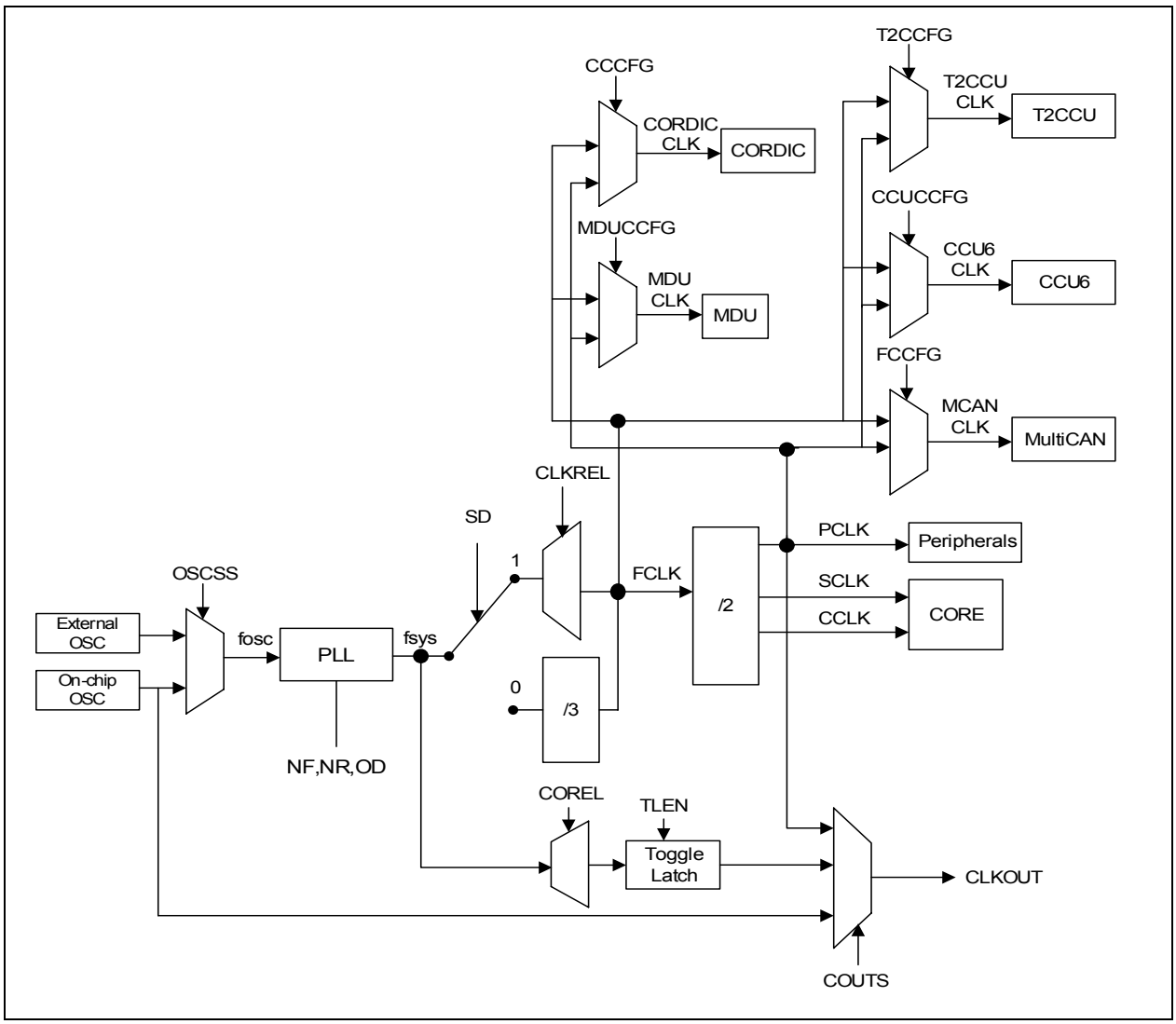



**Figure 22 Clock Generation from $f_{sys}$**

## 3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits.The clock frequency of T2CCU, $f_{T2CCU}$, could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

### T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be ‘reset’ immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
  – Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
  – Active level can be defined by register bit for channel groups A and B.
  – Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

**Table 40 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | 6) |
| Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$) | $I_M$ SR | SR | – | 8 | mA | |
| Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$) | $\Sigma\|I_M\|$ | SR | – | 150 | mA | |
| Maximum current into $V_{DDP}$ | $I_{MVDDP}$ | SR | – | 200 | mA | 5) |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 200 | mA | 5) |

1) DS = 0 refers to the pin having a weak drive strength which is programmable via Px_DS register.

2) DS = 1 refers to the pin having a strong drive strength which is programmable via Px_DS register.

3) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

4) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

5) Not subjected to production test, verified by design/characterization.

6) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when $V_{DDP}$ is powered off.

7) P0.1 has a minimum input hysteresis of 0.25V.

### 4.2.2 Supply Threshold Characteristics

**Table 41** provides the characteristics of the supply threshold in the XC87x.

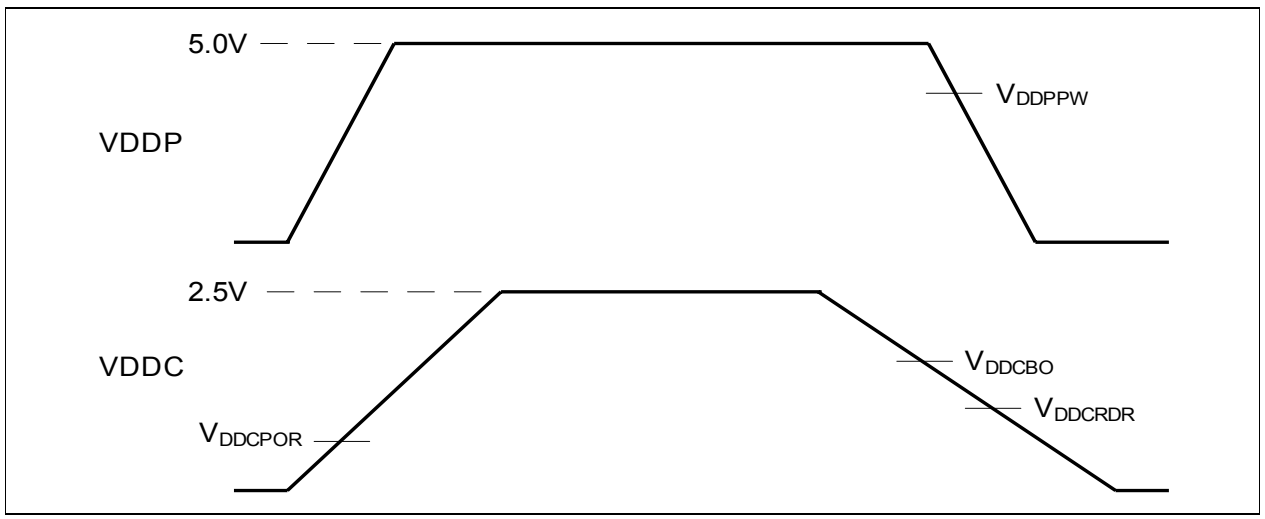



**Figure 34 Supply Threshold Parameters**

**Table 41 Supply Threshold Parameters (Operating Conditions apply)**

| Parameters | Symbol | | Limit Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| $V_{DDC}$ brownout voltage[1)] | $V_{DDCBO}$ | CC | 1.7 | 1.9 | 2.2 | V |
| RAM data retention voltage | $V_{DDCRDR}$ | CC | 1.2 | – | – | V |
| $V_{DDP}$ prewarning voltage[2)] | $V_{DDPPW}$ | CC | 3.8 | 4.2 | 4.5 | V |
| Power-on reset voltage[1)3)] | $V_{DDCPOR}$ | CC | 1.7 | 1.9 | 2.2 | V |

1) Detection is enabled in both active and power-down mode.

2) Detection is enabled for 5.0V power supply variant.
Detection is disabled for 3.3V power supply variant.

3) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

**Table 54 JTAG Timing (Operating Conditions apply; CL = 50 pF)** (cont'd)

| Parameter | Symbol | | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min | max | | |
| TDO high impedance to valid output from TCK | $t_4$ | CC | - | 18 | ns | 5V Device[1)] |
| | | | - | 21 | ns | 3.3V Device[1)] |
| TDO valid output to high impedance from TCK | $t_5$ | CC | - | 21 | ns | 5V Device[1)] |
| | | | - | 20 | ns | 3.3V Device[1)] |

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

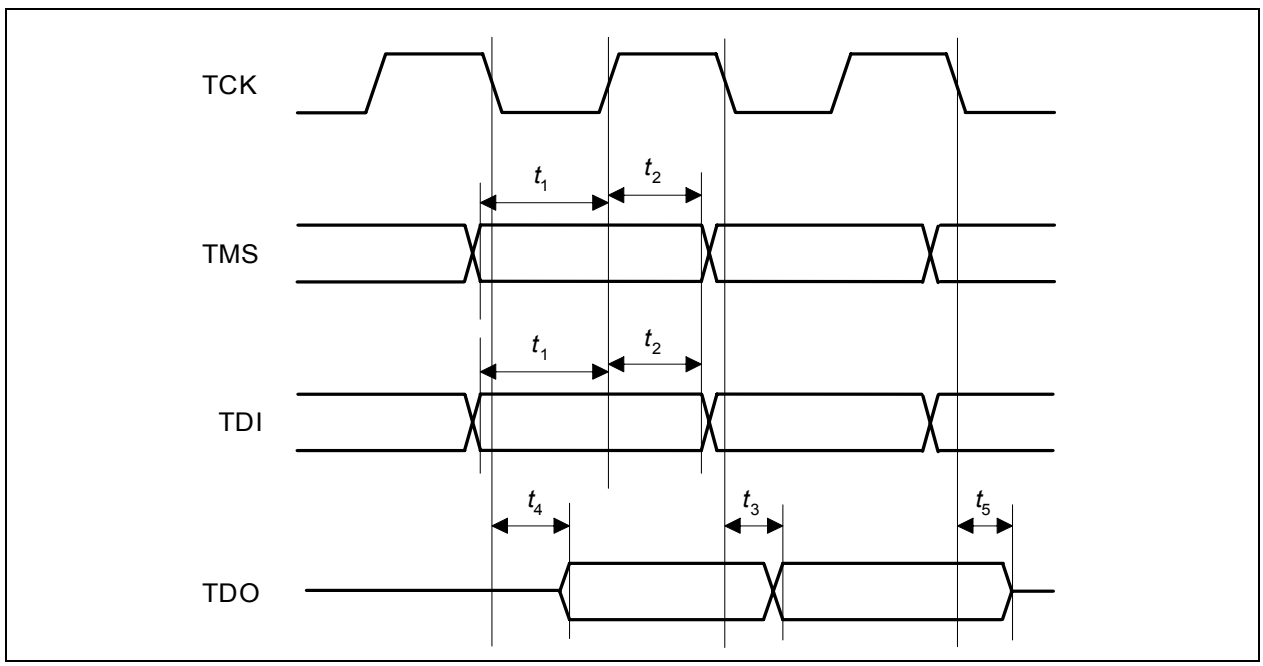
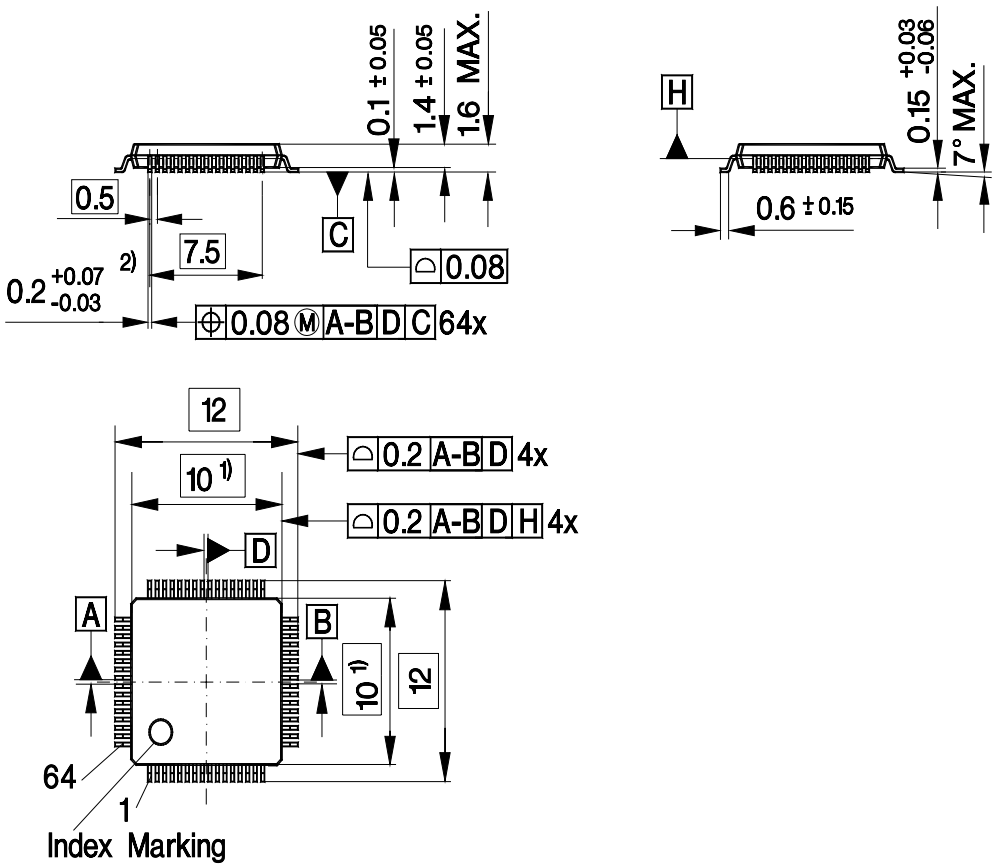



**Figure 45 JTAG Timing**

## 5.2 Package Outline

**Figure 47** shows the package outlines of the XC878.




1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

**Figure 47 PG-LQFP-64-4 Package Outline**