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Details

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc878m16ffi3v3acfxuma1

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General Device Information

2.4 Pin Definitions and Functions

The functions and default states of the XC87x external pins are provided in [Table 3](#).

Table 3 Pin Definitions and Functions

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P0		I/O		Port 0 Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface. <i>Note: External Bus Interface is not available in XC874.</i>
P0.0	17/12		Hi-Z	TCK_0 JTAG Clock Input T12HR_1 CCU6 Timer 12 Hardware Run Input CC61_1 Input/Output of Capture/Compare channel 1 CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	21/14		Hi-Z	TDI_0 JTAG Serial Data Input T13HR_1 CCU6 Timer 13 Hardware Run Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input COUT61_1 Output of Capture/Compare channel 1 EXF2_1 Timer 2 External Flag Output
P0.2	18/13		PU	CTRAP_2 CCU6 Trap Input TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P4		I/O		Port 4 Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Bus Interface. <i>Note: External Bus Interface is not available in XC874.</i>
P4.0	59/45		Hi-Z	RXDC0_3 MultiCAN Node 0 Receiver Input CC60_1 Output of Capture/Compare channel 0 T2CC0_0/ External Interrupt Input 3/T2CCU EXINT3_1 Capture/Compare Channel 0 D0 Data Line 0 Input/Output
P4.1	60/46		Hi-Z	TXDC0_3 MultiCAN Node 0 Transmitter Output COUT60_1 Output of Capture/Compare channel 0 T2CC1_0/ External Interrupt Input 4/T2CCU EXINT4_1 Capture/Compare Channel 1 D1 Data Line 1 Input/Output
P4.2	61/47		PU	EXINT6_1 External Interrupt Input 6 T21_0 Timer 21 Input D2 Data Line 2 Input/Output
P4.3	40/31		Hi-Z	T2EX_1 Timer 2 External Trigger Input EXF21_1 Timer 21 External Flag Output COUT63_2 Output of Capture/Compare channel 3 D3 Data Line 3 Input/Output
P4.4	45/-		Hi-Z	CCPOS0_3 CCU6 Hall Input 0 T0_0 Timer 0 Input CC61_4 Output of Capture/Compare channel 1 T2CC2_0/ External Interrupt Input 5/T2CCU EXINT5_1 Capture/Compare Channel 2 D4 Data Line 4 Input/Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P5		I/O		Port 5 Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External Interface.
P5.0	8/-		PU	EXINT1_1 External Interrupt Input 1 A0 Address Line 0 Output
P5.1	9/-		PU	EXINT2_1 External Interrupt Input 2 A1 Address Line 1 Output
P5.2	12/-		PU	RXD_2 UART Receive Data Input T2CC2_2/ External Interrupt Input 5/T2CCU EXINT5_3 Capture/Compare Channel 2 A2 Address Line 2 Output
P5.3	13/-		PU	CCPOS0_0 CCU6 Hall Input 0 EXINT1_0 External Interrupt Input 1 T12HR_2 CCU6 Timer 12 Hardware Run Input CC61_3 Input of Capture/Compare channel 1 TXD_2 UART Transmit Data Output/Clock Output T2CC5_2 Compare Output Channel 5 A3 Address Line 3 Output
P5.4	14/-		PU	CCPOS1_0 CCU6 Hall Input 1 EXINT2_0 External Interrupt Input 2 T13HR_2 CCU6 Timer 13 Hardware Run Input CC62_3 Input of Capture/Compare channel 2 RXDO_2 UART Transmit Data Output T2CC4_2 Compare Output Channel 4 A4 Address Line 4 Output

Functional Description

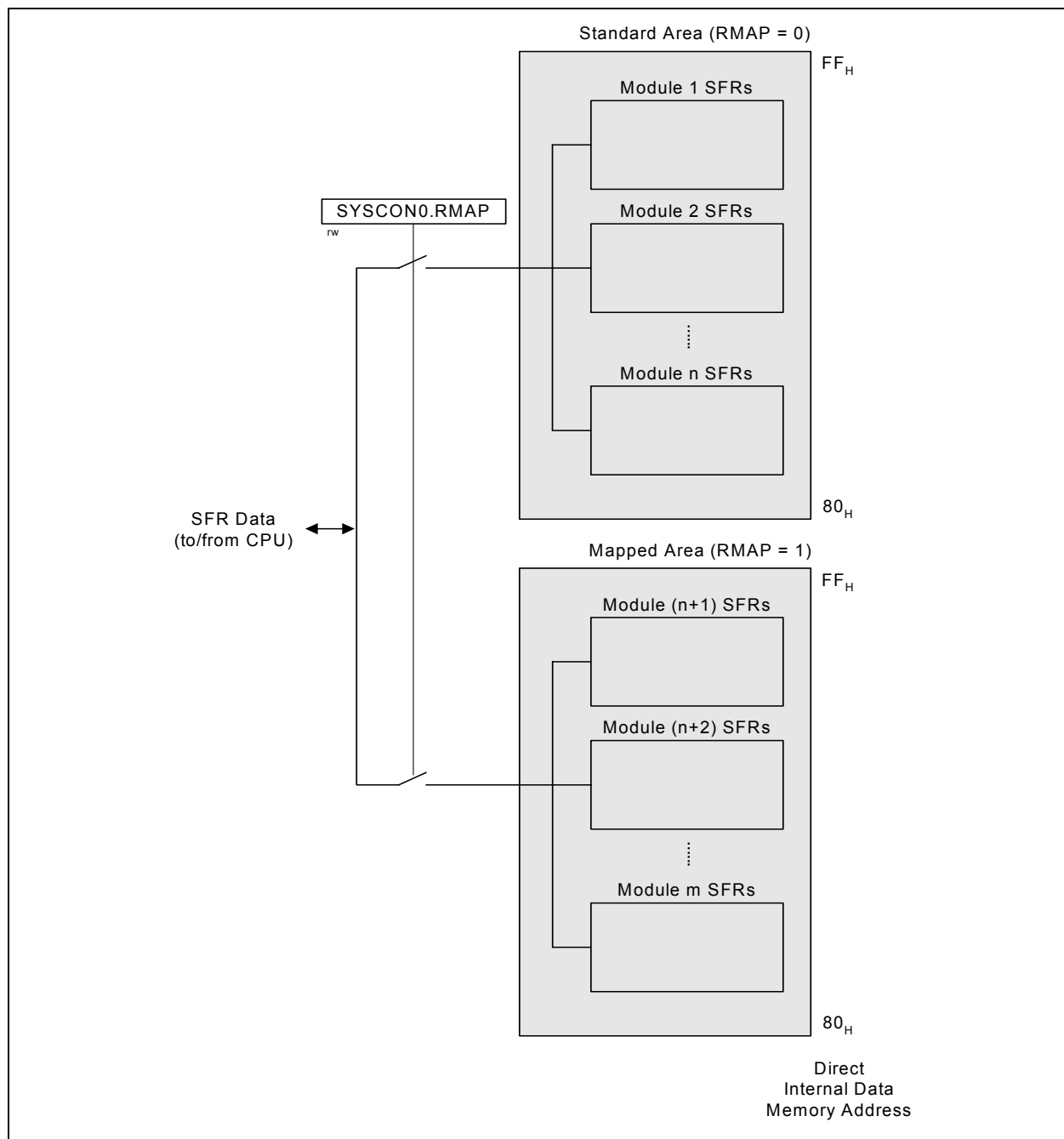


Figure 9 Address Extension by Mapping

Functional Description

- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
(this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

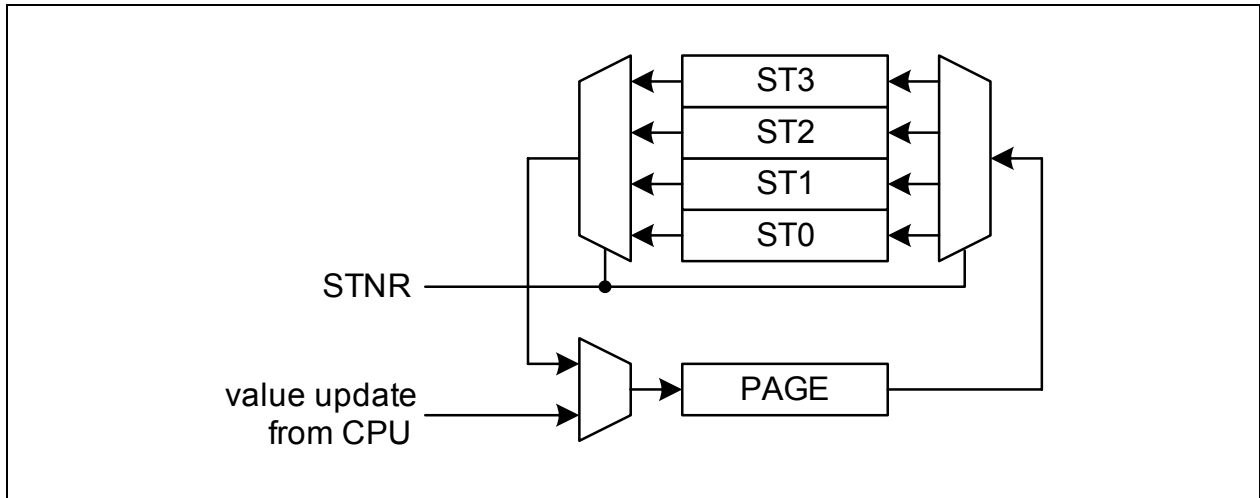


Figure 11 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC87x supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

Functional Description

3.2.4 XC87x Register Overview

The SFRs of the XC87x are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in [Chapter 3.2.4.1](#) to [Chapter 3.2.4.15](#).

Note: The addresses of the bitaddressable SFRs appear in bold typeface.

3.2.4.1 CPU Registers

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Table 5 CPU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0 or 1										
81 _H	SP Stack Pointer Register Reset: 07_H	Bit Field	SP							
		Type	rw							
82 _H	DPL Data Pointer Register Low Reset: 00_H	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
83 _H	DPH Data Pointer Register High Reset: 00_H	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
87 _H	PCON Power Control Register Reset: 00_H	Bit Field	SMOD	0			GF1	GF0	0	IDLE
		Type	rw	r			rw	rw	r	rw
88 _H	TCON Timer Control Register Reset: 00_H	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Type	rwh	rw	rwh	rw	rwh	rw	rwh	rw
89 _H	TMOD Timer Mode Register Reset: 00_H	Bit Field	GATE 1	T1S	T1M		GATE 0	T0S	T0M	
		Type	rw	rw	rw		rw	rw	rw	
8A _H	TL0 Timer 0 Register Low Reset: 00_H	Bit Field	VAL							
		Type	rwh							
8B _H	TL1 Timer 1 Register Low Reset: 00_H	Bit Field	VAL							
		Type	rwh							
8C _H	TH0 Timer 0 Register High Reset: 00_H	Bit Field	VAL							
		Type	rwh							
8D _H	TH1 Timer 1 Register High Reset: 00_H	Bit Field	VAL							
		Type	rwh							
94 _H	MEX1 Memory Extension Register 1 Reset: 00_H	Bit Field	CB				NB			
		Type	r				rw			
95 _H	MEX2 Memory Extension Register 2 Reset: 00_H	Bit Field	MCM	MCB			IB			
		Type	rw	rw			rw			
96 _H	MEX3 Memory Extension Register 3 Reset: 00_H	Bit Field	MCB1 9	0		MXB1 9	MXM	MXB		
		Type	rw	r		rw	rw	rw		

Functional Description
3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
A3 _H	CCU6_PAGE Page Register Reset: 00 _H	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
9A _H	CCU6_CC63SRL Capture/Compare Shadow Register for Channel CC63 Low Reset: 00 _H	Bit Field	CC63SL							
		Type	rw							
9B _H	CCU6_CC63SRH Capture/Compare Shadow Register for Channel CC63 High Reset: 00 _H	Bit Field	CC63SH							
		Type	rw							
9C _H	CCU6_TCTR4L Timer Control Register 4 Low Reset: 00 _H	Bit Field	T12 STD	T12 STR	0		DT RES	T12 RES	T12R S	T12R R
		Type	w	w	r		w	w	w	w
9D _H	CCU6_TCTR4H Timer Control Register 4 High Reset: 00 _H	Bit Field	T13 STD	T13 STR	0			T13 RES	T13R S	T13R R
		Type	w	w	r			w	w	w
9E _H	CCU6_MCMOUTSL Multi-Channel Mode Output Shadow Register Low Reset: 00 _H	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
9F _H	CCU6_MCMOUTSH Multi-Channel Mode Output Shadow Register High Reset: 00 _H	Bit Field	STRH P	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
A4 _H	CCU6_ISRL Capture/Compare Interrupt Status Reset Register Low Reset: 00 _H	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
		Type	w	w	w	w	w	w	w	w
A5 _H	CCU6_ISRH Capture/Compare Interrupt Status Reset Register High Reset: 00 _H	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
A6 _H	CCU6_CMPMODIFL Compare State Modification Register Low Reset: 00 _H	Bit Field	0	MCC6 3S	0			MCC6 2S	MCC6 1S	MCC6 0S
		Type	r	w	r			w	w	w
A7 _H	CCU6_CMPMODIFH Compare State Modification Register High Reset: 00 _H	Bit Field	0	MCC6 3R	0			MCC6 2R	MCC6 1R	MCC6 0R
		Type	r	w	r			w	w	w
FA _H	CCU6_CC60SRL Capture/Compare Shadow Register for Channel CC60 Low Reset: 00 _H	Bit Field	CC60SL							
		Type	rwh							
FB _H	CCU6_CC60SRH Capture/Compare Shadow Register for Channel CC60 High Reset: 00 _H	Bit Field	CC60SH							
		Type	rwh							

Functional Description
Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FC _H	CCU6_CC61SRL Reset: 00_H Capture/Compare Shadow Register for Channel CC61 Low	Bit Field	CC61SL							
		Type	rwh							
FD _H	CCU6_CC61SRH Reset: 00_H Capture/Compare Shadow Register for Channel CC61 High	Bit Field	CC61SH							
		Type	rwh							
FE _H	CCU6_CC62SRL Reset: 00_H Capture/Compare Shadow Register for Channel CC62 Low	Bit Field	CC62SL							
		Type	rwh							
FF _H	CCU6_CC62SRH Reset: 00_H Capture/Compare Shadow Register for Channel CC62 High	Bit Field	CC62SH							
		Type	rwh							
RMAP = 0, PAGE 1										
9A _H	CCU6_CC63RL Reset: 00_H Capture/Compare Register for Channel CC63 Low	Bit Field	CC63VL							
		Type	rh							
9B _H	CCU6_CC63RH Reset: 00_H Capture/Compare Register for Channel CC63 High	Bit Field	CC63VH							
		Type	rh							
9C _H	CCU6_T12PRL Reset: 00_H Timer T12 Period Register Low	Bit Field	T12PVL							
		Type	rwh							
9D _H	CCU6_T12PRH Reset: 00_H Timer T12 Period Register High	Bit Field	T12PVH							
		Type	rwh							
9E _H	CCU6_T13PRL Reset: 00_H Timer T13 Period Register Low	Bit Field	T13PVL							
		Type	rwh							
9F _H	CCU6_T13PRH Reset: 00_H Timer T13 Period Register High	Bit Field	T13PVH							
		Type	rwh							
A4 _H	CCU6_T12DTCL Reset: 00_H Dead-Time Control Register for Timer T12 Low	Bit Field	DTM							
		Type	rw							
A5 _H	CCU6_T12DTCH Reset: 00_H Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0
		Type	r	rh	rh	rh	r	rw	rw	rw
A6 _H	CCU6_TCTR0L Reset: 00_H Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE1 2	T12R	T12 PRE	T12CLK		
		Type	rw	rh	rh	rh	rw	rw		
A7 _H	CCU6_TCTR0H Reset: 00_H Timer Control Register 0 High	Bit Field	0		STE1 3	T13R	T13 PRE	T13CLK		
		Type	r		rh	rh	rw	rw		
FA _H	CCU6_CC60RL Reset: 00_H Capture/Compare Register for Channel CC60 Low	Bit Field	CC60VL							
		Type	rh							
FB _H	CCU6_CC60RH Reset: 00_H Capture/Compare Register for Channel CC60 High	Bit Field	CC60VH							
		Type	rh							
FC _H	CCU6_CC61RL Reset: 00_H Capture/Compare Register for Channel CC61 Low	Bit Field	CC61VL							
		Type	rh							

Functional Description
3.2.4.15 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 19 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
D1 _H	FCON Reset: 10_H P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D2 _H	EECON Reset: 10_H D-Flash Control Register	Bit Field	0	EEBS Y	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D3 _H	FCS Reset: 80_H Flash Control and Status Register	Bit Field	1	SBEIE	FTEN	0	EEDE RR	EESE RR	FDER R	FSER R
		Type	r	rw	rwh	r	rwh	rwh	rwh	rwh
D4 _H	FEAL Reset: 00_H Flash Error Address Register, Low Byte	Bit Field	ECCEADDR							
		Type	rh							
D5 _H	FEAH Reset: 00_H Flash Error Address Register, High Byte	Bit Field	ECCEADDR							
		Type	rh							
D6 _H	FTVAL Reset: 78_H Flash Timer Value Register	Bit Field	MODE	OFVAL						
		Type	rw	rw						
DD _H	FCS1 Reset: 00_H Flash Control and Status Register 1	Bit Field	0							EEAB ORT
		Type	r							rwh

Functional Description

Table 20 and **Table 21** shows the Flash data retention and endurance targets for Industrial profile and Automotive profile respectively.

**Table 20 Flash Data Retention and Endurance for Industrial Profile
(Operating Conditions apply)**

Retention	Endurance ¹⁾²⁾	Size	Remarks
Program Flash			
15 years	1000 cycles	up to 60 Kbytes	
Data Flash			
15 years	1000 cycles	4 Kbytes	
10 years	10,000 cycles	4 Kbytes	
5 years	30,000 cycles	4 Kbytes	
1 year	100,000 cycles	4 Kbytes	SAF and SAX variant
	80,000 cycles		SAK variant

1) In Program Flash, one cycle refers to the programming of all pages in the flash bank and a mass erase.

2) In Data Flash, one cycle refers to the programming of all wordlines in a page and a page erase.

**Table 21 Flash Data Retention and Endurance for Automotive Profile
(Operating Conditions apply)**

Retention	Endurance ¹⁾²⁾	Size	Remarks
Program Flash			
15 years	1000 cycles	up to 60 Kbytes	
Data Flash			
15 years	1000 cycles	4 Kbytes	
5 years	10,000 cycles	1 Kbytes	
2 years	15,000 cycles	512 Bytes	
2 years	30,000 cycles	256 Bytes	
1 year	100,000 cycles	128 Bytes	

1) In Program Flash, one cycle refers to the programming of all pages in the flash bank and a mass erase.

2) In Data Flash, one cycle refers to the programming of all wordlines in a page and a page erase.

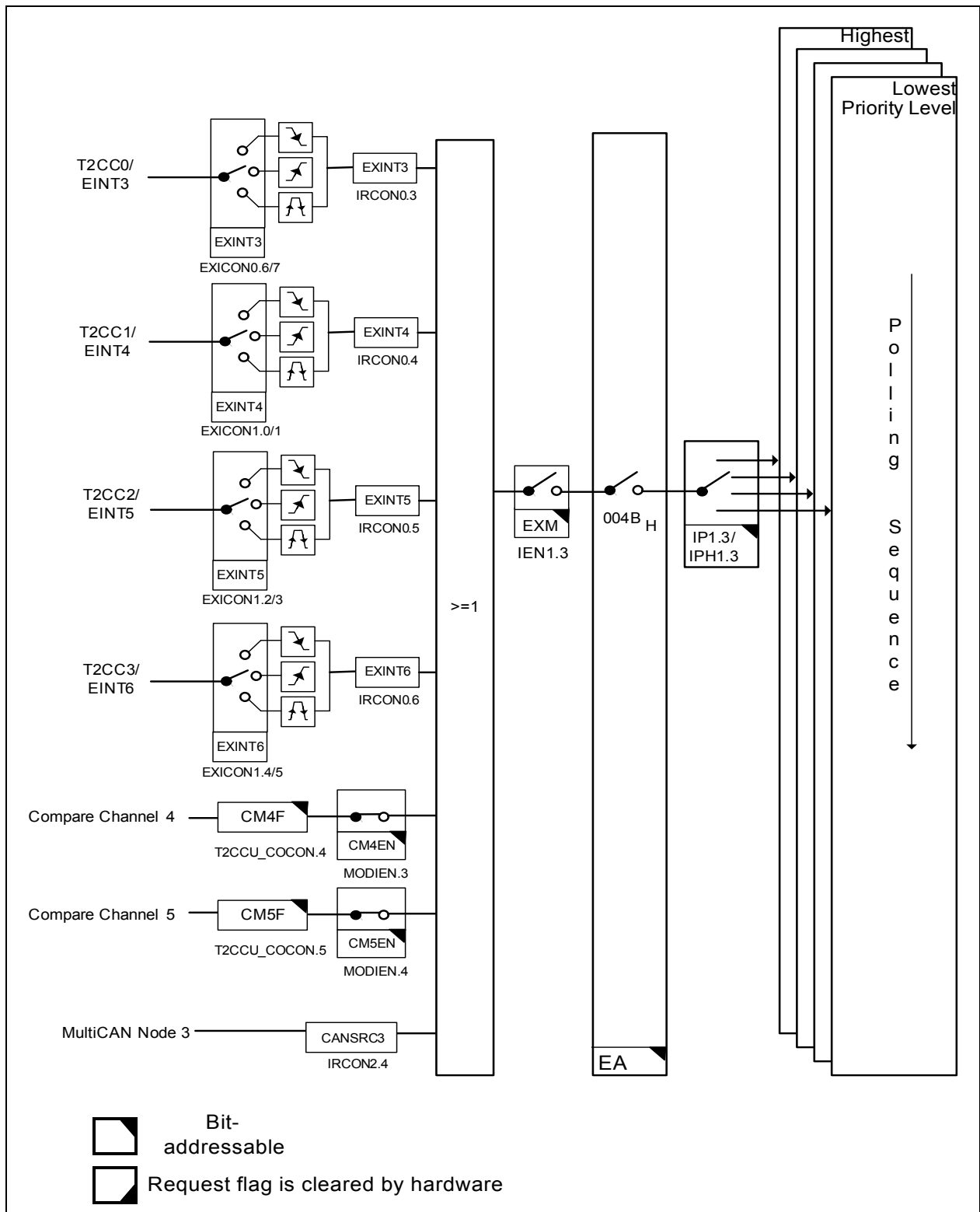


Figure 16 Interrupt Request Sources (Part 4)

3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC87x interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in [Table 22](#).

Table 22 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
NMI	0073 _H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash Timer NMI	NMIFLASH	
		V _{DDP} Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 _H	External Interrupt 0	EX0	IEN0
XINTR1	000B _H	Timer 0	ET0	
XINTR2	0013 _H	External Interrupt 1	EX1	
XINTR3	001B _H	Timer 1	ET1	
XINTR4	0023 _H	UART	ES	
XINTR5	002B _H	T2CCU	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		
		LIN		

Functional Description

resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor. **Figure 21** shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

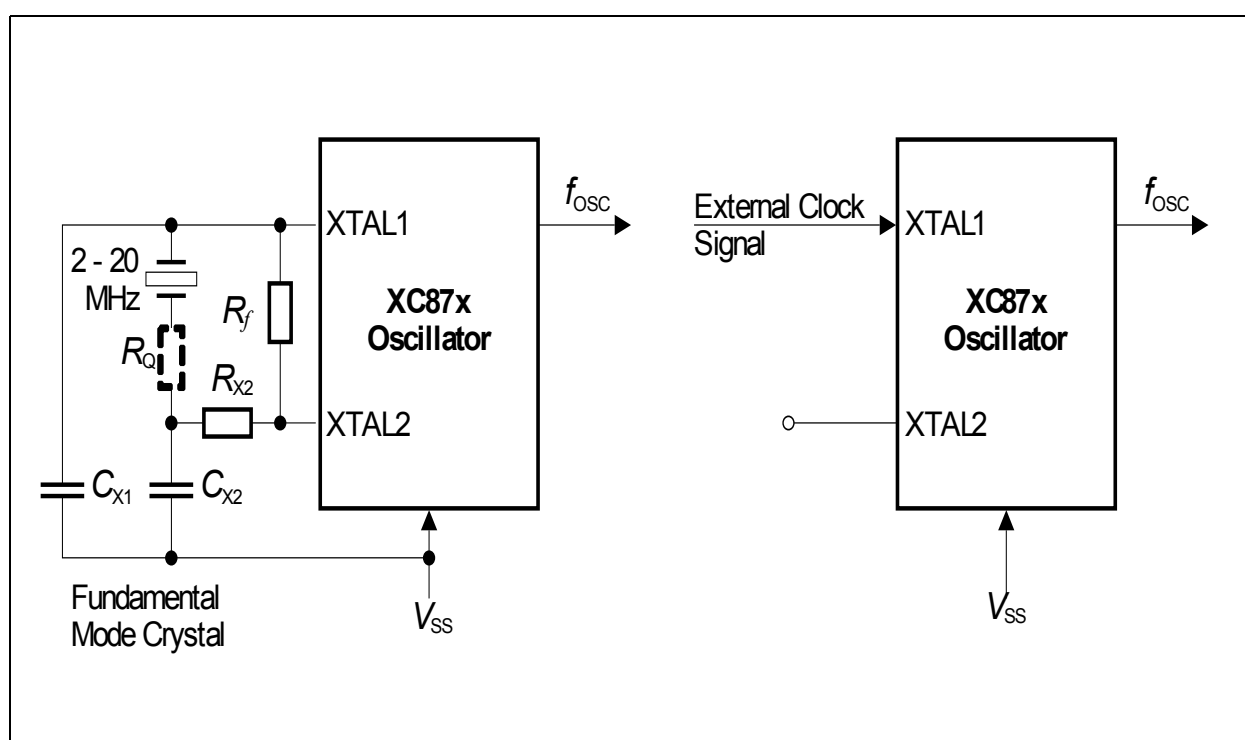


Figure 21 External Oscillator Circuitry

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

Functional Description

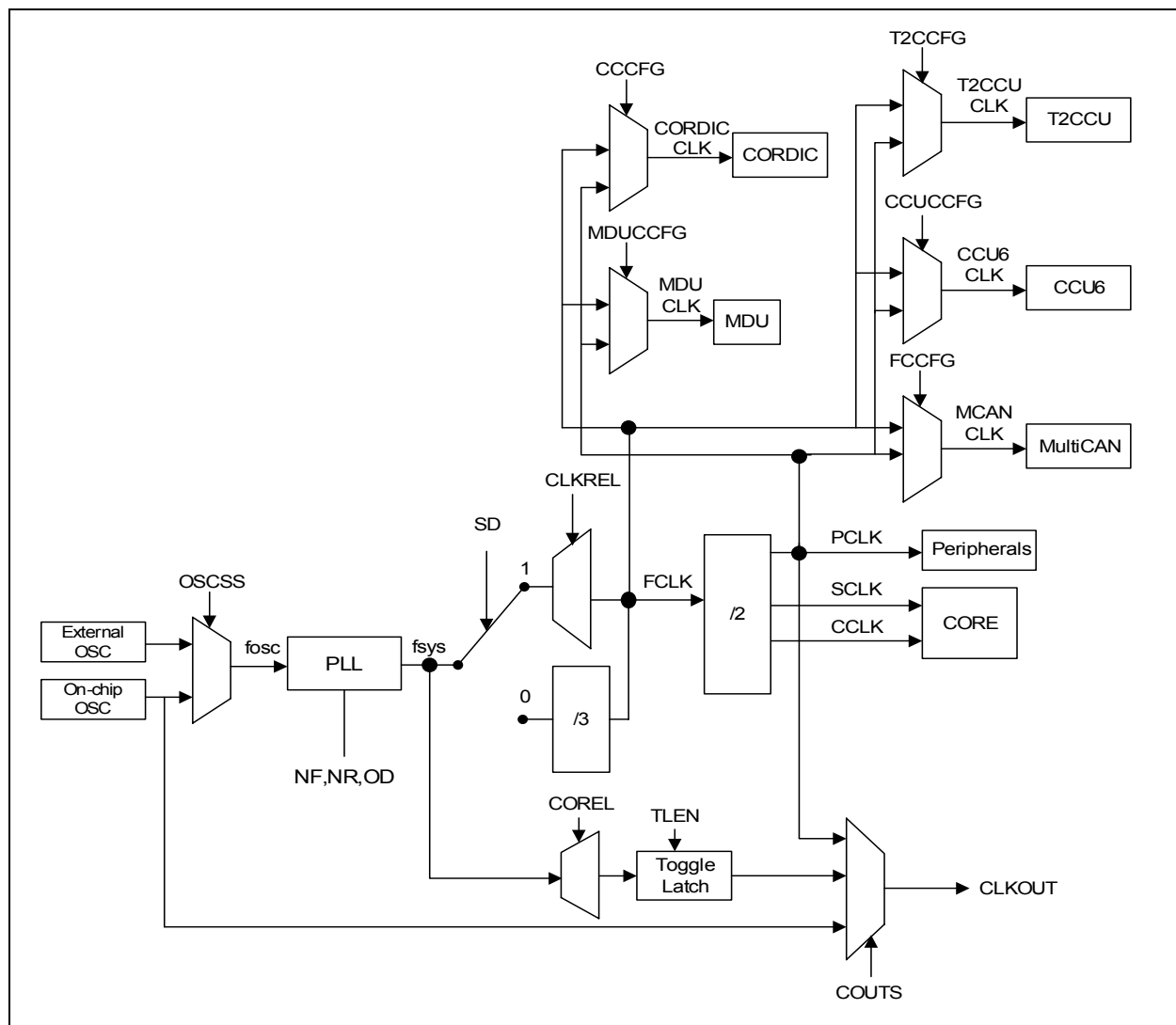


Figure 22 Clock Generation from f_{sys}

Functional Description

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC87x system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC87x will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access.

Figure 24 shows the block diagram of the WDT unit.

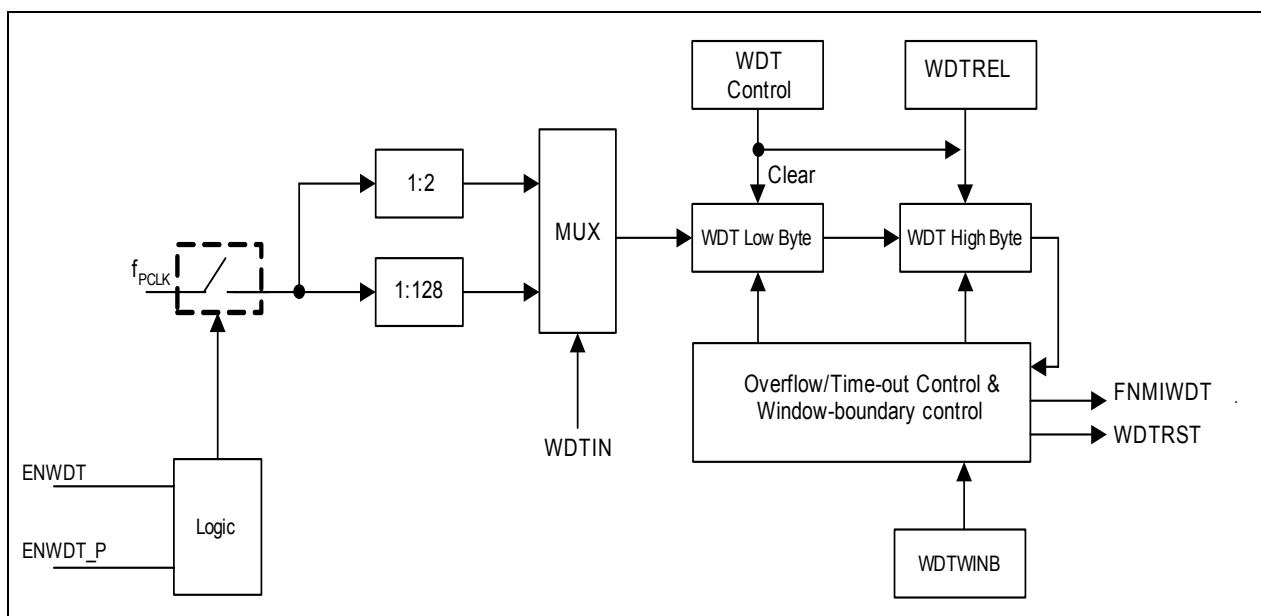


Figure 24 WDT Block Diagram

Functional Description

3.21 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 Mbaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

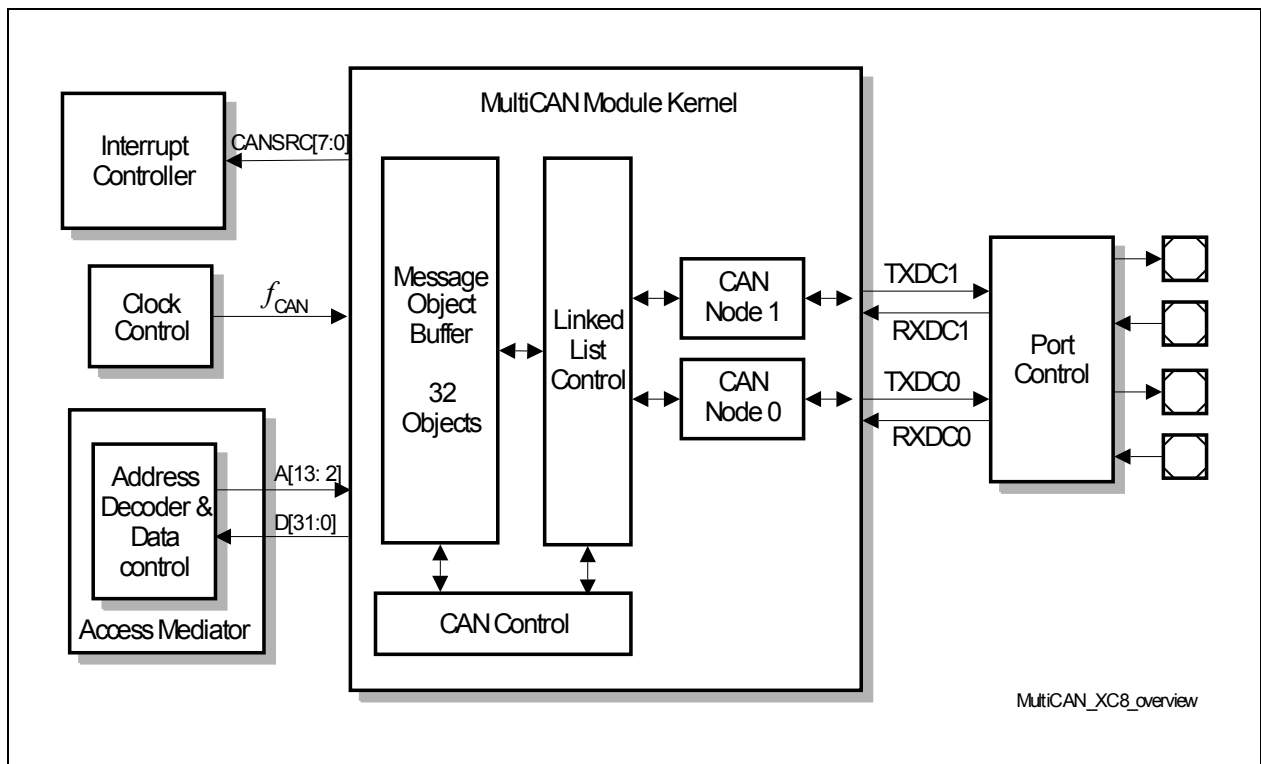


Figure 30 Overview of the MultiCAN

Features

- Compliant to ISO 11898.

Electrical Parameters

4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 42 ADC Characteristics (Operating Conditions apply; $V_{DDP} = 5V$ Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	V_{AREF}	SR	$V_{AGND} + 1$	V_{DDP}	$V_{DDP} + 0.05$	V	¹⁾
Analog reference ground	V_{AGND}	SR	$V_{SS} - 0.05$	V_{SS}	$V_{AREF} - 1$	V	¹⁾
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}		–	24	–	MHz	module clock ¹⁾
	f_{ADCI}		–	–	14 ²⁾	MHz	internal analog clock ¹⁾ See Figure 31
Sample time	t_S	CC	$(2 + INPCR0.STC) \times t_{ADCI}$			μs	¹⁾
Conversion time	t_C	CC	See Section 4.2.3.1			μs	¹⁾
Differential Nonlinearity	$ EA_{DNL} $	CC	–	–	1.5	LSB	10-bit conversion
Integral Nonlinearity	$ EA_{INL} $	CC	–	–	2	LSB	10-bit conversion
Offset	$ EA_{OFF} $	CC	–	–	3	LSB	10-bit conversion
Gain	$ EA_{GAIN} $	CC	–	–	2.5	LSB	10-bit conversion
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	14	pF	¹⁾³⁾
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	4	5	pF	¹⁾⁴⁾

Electrical Parameters

Table 44 Power Down Current¹⁾(Operating Conditions apply; $V_{DDP} = 5V$ range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. ²⁾	max. ³⁾		
V_{DDP} = 5V Range					
Power-Down Mode	I_{PDP}	20	80	μA	T_A = + 25 °C ⁴⁾⁵⁾
		-	250	μA	T_A = + 85 °C ⁵⁾⁶⁾

- 1) The table is only applicable to SAF and SAX variants. SAK variant does not support power-down mode
- 2) The typical I_{PDP} values are based on preliminary measurements and are to be used as reference only. These values are measured at $V_{DDP} = 5.0\text{ V}$.
- 3) The maximum I_{PDP} values are measured at $V_{DDP} = 5.5\text{ V}$.
- 4) I_{PDP} has a maximum value of $450\text{ }\mu A$ at $T_A = + 105\text{ }^{\circ}C$.
- 5) I_{PDP} is measured with: $\overline{RESET} = V_{DDP}$, $V_{AGND} = V_{SS}$, $RXD/INT0 = V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.
- 6) Not subjected to production test, verified by design/characterization.

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