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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	27MHz
Connectivity	SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc878m16ffi5vacfxuma1

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface. *Note: External Bus Interface is not available in XC874.*
P1.0	34/25		PU	RXD_0 UART Receive Data Input T2EX_0 Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input A8 Address Line 8 Output
P1.1	35/26		PU	EXINT3_0 External Interrupt Input 3 T0_1 Timer 0 Input TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output A9 Address Line 9 Output
P1.2	36/27		PU	SCK_0 SSC Clock Input/Output A10 Address Line 10 Output
P1.3	37/28		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input SCK_2 SSC Clock Input/Output TXDC1_3 MultiCAN Node 1 Transmitter Output A11 Address Line 11 Output
P1.4	38/29		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input MTSR_2 SSC Master Transmit Output/Slave Receive Input A12 Address Line 12 Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Type	Reset State	Function	
P5.5	15/-		PU	CCPOS2_0	CCU6 Hall Input 2
				CTRAP_1	CCU6 Trap Input
				CC60_3	Input of Capture/Compare channel 0
				TDO_1	JTAG Serial Data Output
				TXD1_2	UART1 Transmit Data Output/ Clock Output
				T2CC0_2/ EXINT3_3	External Interrupt Input 3/T2CCU Capture/Compare Channel 0
				A5	Address Line 5 Output
P5.6	19/-		PU	TCK_1	JTAG Clock Input
				RXDO1_2	UART1 Transmit Data Output
				T2CC1_2/ EXINT4_3	External Interrupt Input 4/T2CCU Capture/Compare Channel 1
				A6	Address Line 6 Output
P5.7	20/-		PU	TDI_1	JTAG Serial Data Input
				RXD1_2	UART1 Receive Data Input
				T2CC3_2/ EXINT6_4	External Interrupt Input 6/T2CCU Capture/Compare Channel 3
				A7	Address Line 7 Output

3 Functional Description

Chapter 3 provides an overview of the XC87x functional description.

3.1 Processor Architecture

The XC87x is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC87x CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC87x CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 6 shows the CPU functional blocks.

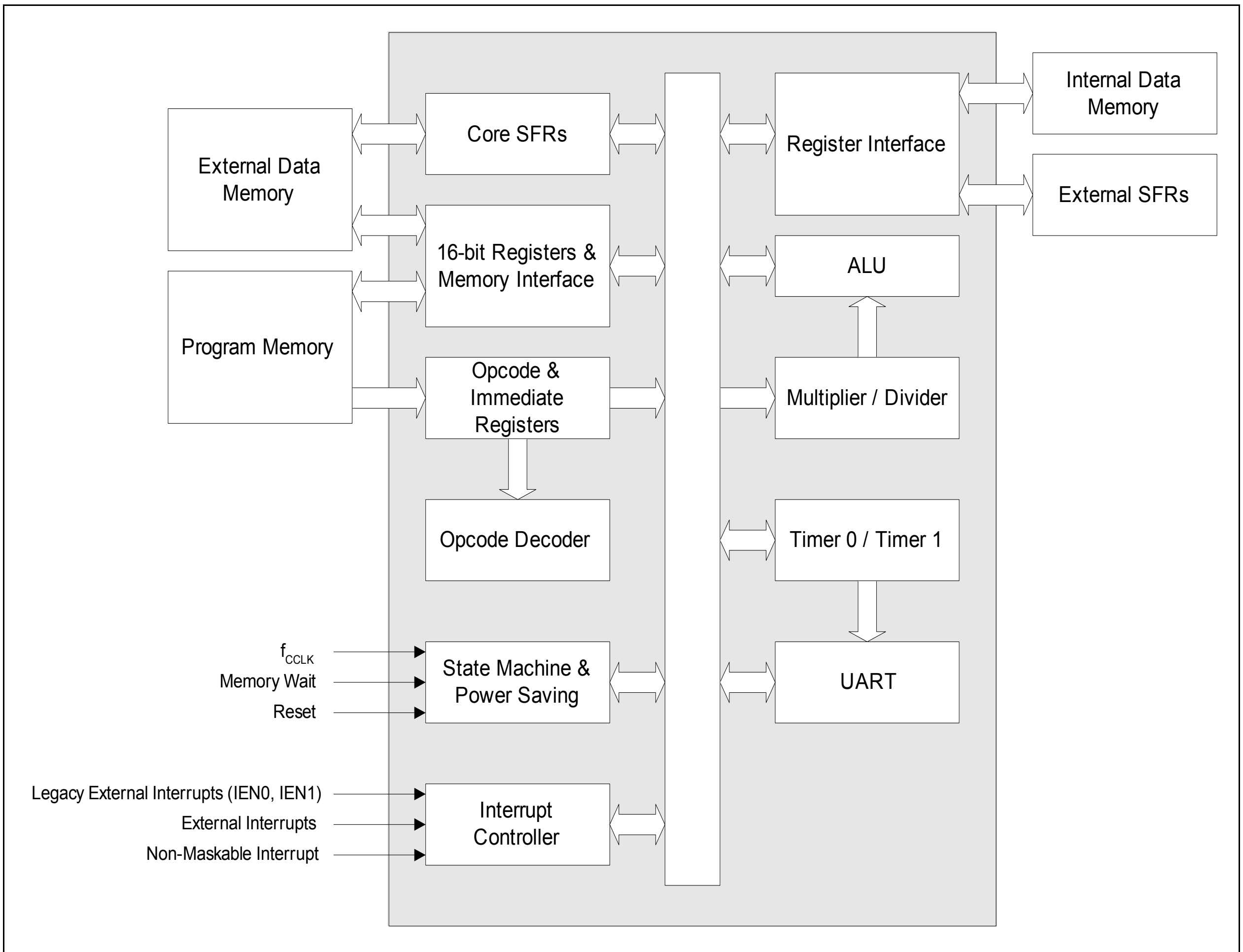

Figure 6 CPU Block Diagram

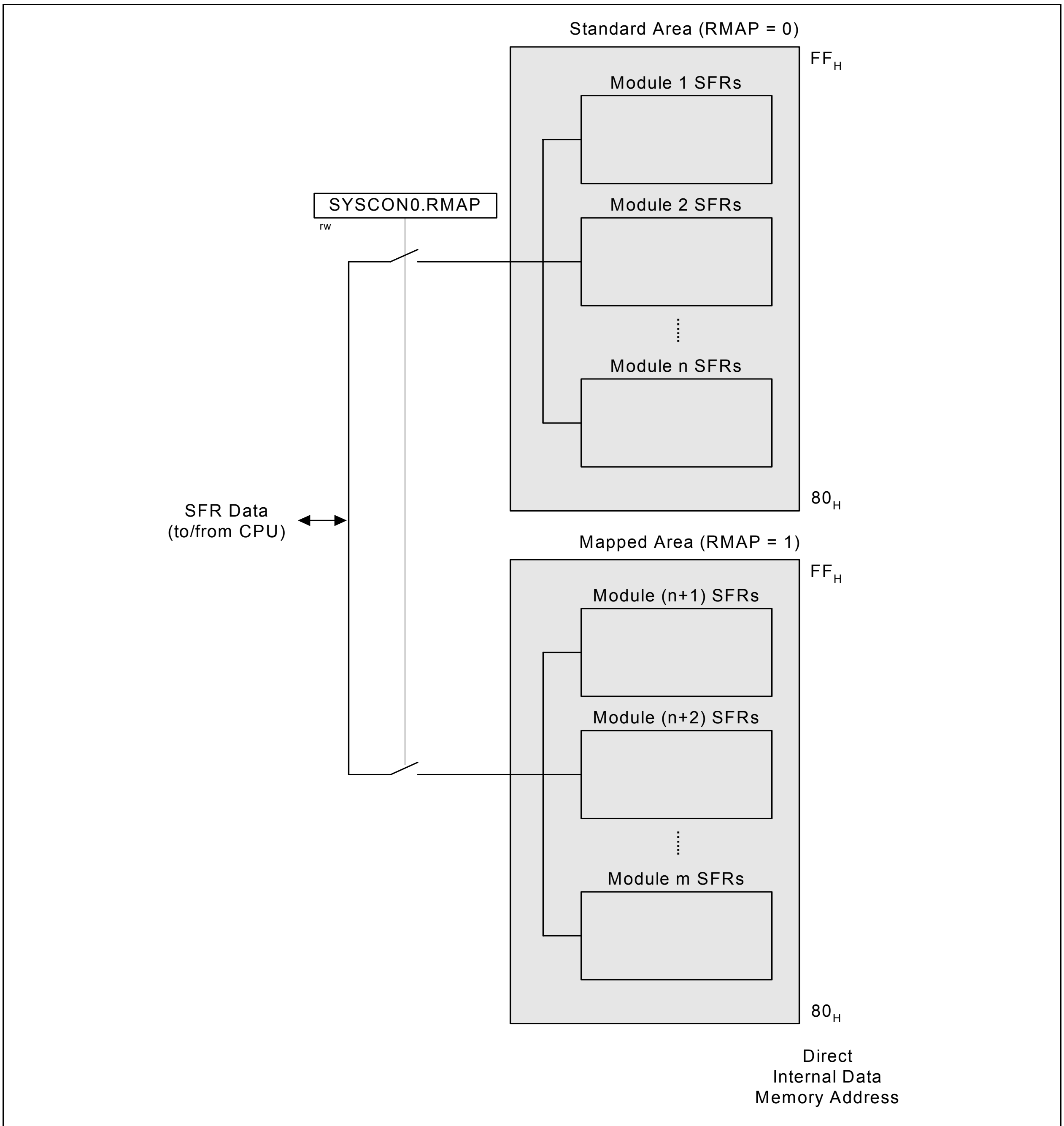

Figure 9 Address Extension by Mapping

SYSCON0
System Control Register 0 **Reset Value: 04_H**

7	6	5	4	3	2	1	0
	0		IMODE	0	1	0	RMAP
	r		rw	r	r	r	rw

Field	Bits	Type	Description
RMAP	0	rw	**Interrupt Node XINTR0 Enable** 0 The access to the standard SFR area is enabled 1 The access to the mapped SFR area is enabled
1	2	r	**Reserved** Returns 1 if read; should be written with 1.
0	[7:5], 3,1	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The RMAP bit should be cleared/set by ANL or ORL instructions.The rest bits of SYSCON0 should not be modified.

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC87x has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 10**.

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 2										
CA$_H$	**ADC_RESR0L** **Reset: 00$_H$** Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB$_H$	**ADC_RESR0H** **Reset: 00$_H$** Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC$_H$	**ADC_RESR1L** **Reset: 00$_H$** Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD$_H$	**ADC_RESR1H** **Reset: 00$_H$** Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE$_H$	**ADC_RESR2L** **Reset: 00$_H$** Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF$_H$	**ADC_RESR2H** **Reset: 00$_H$** Result Register 2 High	Bit Field	RESULT							
		Type	rh							
D2$_H$	**ADC_RESR3L** **Reset: 00$_H$** Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
D3$_H$	**ADC_RESR3H** **Reset: 00$_H$** Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										
CA$_H$	**ADC_RESRA0L** **Reset: 00$_H$** Result Register 0, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB$_H$	**ADC_RESRA0H** **Reset: 00$_H$** Result Register 0, View A High	Bit Field	RESULT							
		Type	rh							
CC$_H$	**ADC_RESRA1L** **Reset: 00$_H$** Result Register 1, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD$_H$	**ADC_RESRA1H** **Reset: 00$_H$** Result Register 1, View A High	Bit Field	RESULT							
		Type	rh							
CE$_H$	**ADC_RESRA2L** **Reset: 00$_H$** Result Register 2, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF$_H$	**ADC_RESRA2H** **Reset: 00$_H$** Result Register 2, View A High	Bit Field	RESULT							
		Type	rh							
D2$_H$	**ADC_RESRA3L** **Reset: 00$_H$** Result Register 3, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
D3$_H$	**ADC_RESRA3H** **Reset: 00$_H$** Result Register 3, View A High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 4										
CA$_H$	**ADC_RCR0** **Reset: 00$_H$** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw

3.7 Reset Control

The XC87x has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC87x is first powered up, the status of certain pins (see **Table 25**) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

The second type of reset in XC87x is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin $\overline{\text{RESET}}$ is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.

3.7.1 Module Reset Behavior

Table 24 lists the functions of the XC87x and the various reset types that affect these functions. The symbol "■" signifies that the particular function is reset to its default state.

Table 24 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core	■	■	■	■	■
Peripherals	■	■	■	■	■
On-Chip Static RAM	Not affected, Reliable	Not affected, Reliable	Not affected, Reliable	Affected, un-reliable	Affected, un-reliable
Oscillator, PLL	■	Not affected	■	■	■
Port Pins	■	■	■	■	■
EVR	The voltage regulator is switched on	Not affected	Not affected	■	■
FLASH	■	■	■	■	■
NMI	Disabled	Disabled	■	■	■

3.7.2 Booting Scheme

When the XC87x is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. **Table 25** shows the available boot options in the XC87x.

Table 25 XC87x Boot Selection [1)]

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	X	User Mode[2)]; on-chip OSC/PLL non-bypassed	0000_H
0	0	X	BSL Mode; (LIN Mode[3)], UART/ MultiCAN Mode[4)5)] and Alternate BSL Mode[6)]); on-chip OSC/PLL non-bypassed	0000_H
0	1	0	OCDS Mode; on-chip OSC/PLL non-bypassed	0000_H
1	1	0	User (JTAG) Mode[7)]; on-chip OSC/PLL non-bypassed (normal)	0000_H

1) In addition to the pins MBC, TMS and P0.0, TM pin also requires an external pull down for all the boot options.
2) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
3) If a device is programmed as LIN, LIN BSL is always used instead of UART/MultiCAN.
4) UART or MultiCAN BSL is decoded by firmware based on the protocol for product variant with MultiCAN. If no MultiCAN and LIN variant, UART BSL is used.
5) In MultiCAN BSL mode, the clock source is switched to XTAL by firmware, bypassing the on-chip oscillator. This avoids any frequency invariance with the on-chip oscillator and allows other frequency clock input, thus ensuring accurate baud rate detection (especially at high bit rates).
6) Alternate BSL Mode is a user defined BSL code programmed in Flash. It is entered if the AltBSLPassword is valid.
7) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

not be bypassed for this PLL mode. The PLL mode is used during normal system operation.

(3.2)

$$f_{SYS} = f_{OSC} \times \frac{NF}{NR \times OD}$$

System Frequency Selection

For the XC87x, the value of NF, NR and OD can be selected by bits NDIV, PDIV and KDIV respectively for different oscillator inputs inorder to obtain the required fsys. But the combination of these factors must fulfill the following condition:

- 100 MHz < f_{VCO} < 175 MHz
- 800 KHz < f_{OSC} / (2 * NR) < 8 MHz

Table 26 provides examples on how the typical system frequency of fsys = 144 MHz and maximum frequency of 160 MHz (CPU clock = 26.67 MHz)can be obtained for the different oscillator sources.

Table 26 System frequency (f_{sys} = 144 MHz)

Oscillator	fosc	N	P	K	fsys
On-chip	4 MHz	72	2	1	144 MHz
	4 MHz	80	2	1	160 MHz
External	8 MHz	72	4	1	144 MHz
	6 MHz	72	3	1	144 MHz
	4 MHz	72	2	1	144 MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 2 MHz to 20 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. An external feedback resistor R_f is also required in the external oscillator circuitry. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative

3.9 Power Saving Modes

The power saving modes of the XC87x provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 23**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

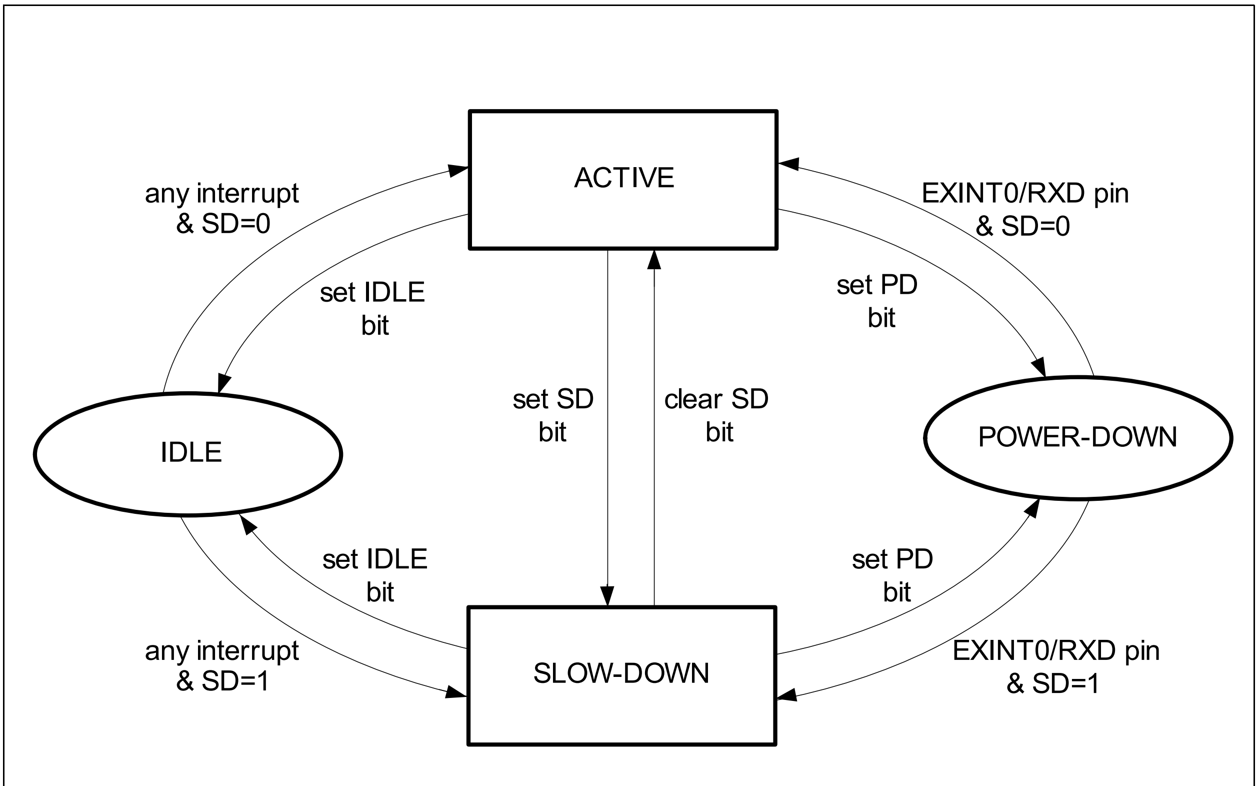

Figure 23 Transition between Power Saving Modes

Note: SAK product variant does not support power-down mode.

3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits.The clock frequency of T2CCU, f_{T2CCU}, could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be ‘reset’ immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
  – Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
  – Active level can be defined by register bit for channel groups A and B.
  – Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

3.21 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

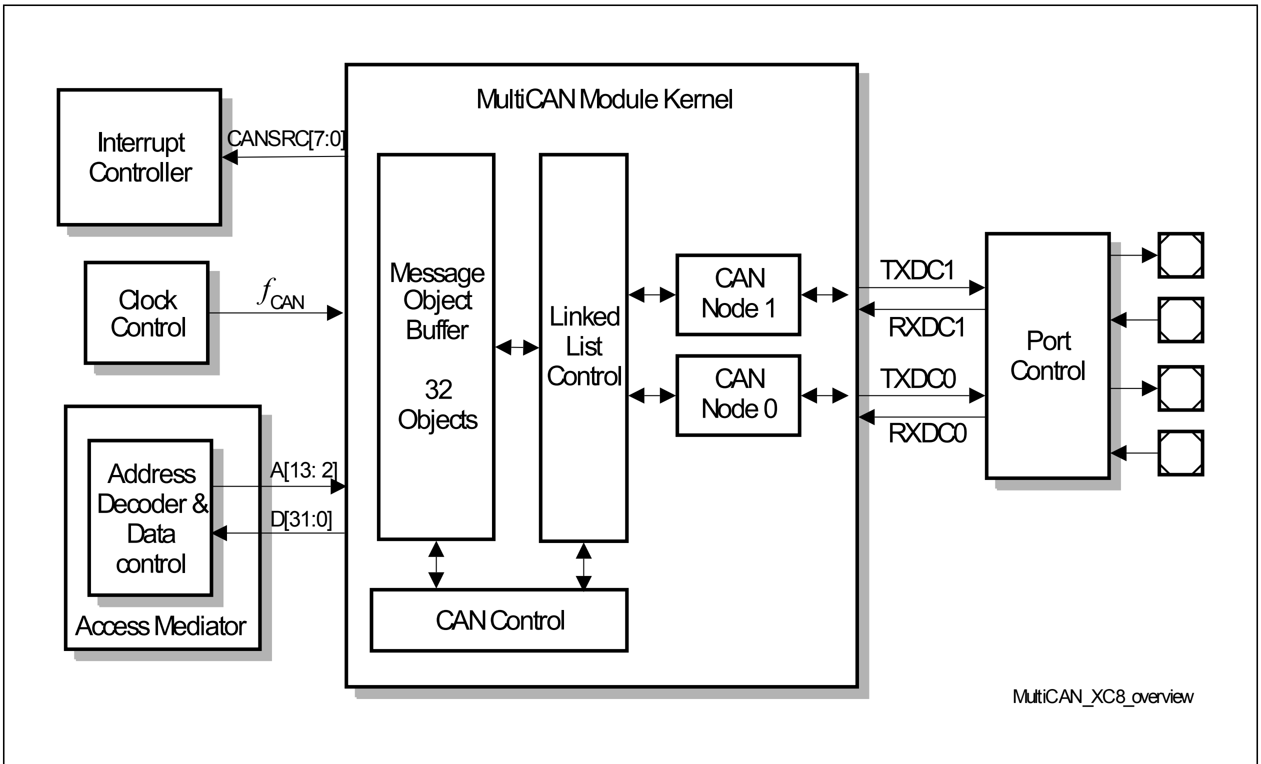

Figure 30 Overview of the MultiCAN

Features

- Compliant to ISO 11898.

3.22 Analog-to-Digital Converter

The XC87x includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at AN0 - AN7.

Features

- Successive approximation
- 8-bit or 10-bit resolution
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.22.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

Figure 31 shows the clocking scheme of the ADC module. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

3.24 Chip Identification Number

The XC87x identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 49_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

Table 37 lists the chip identification numbers of available XC87x Flash device variants.

Table 37 Chip Identification Number

Product Variant	Chip Identification Number
	AC-step
Flash Devices	
XC878-16FF 5V	$4B580063_H$
XC878M-16FF 5V	$4B580023_H$
XC878CM-16FF 5V	$4B580003_H$
XC878LM-16FF 5V	$4B500023_H$
XC878CLM-16FF 5V	$4B500003_H$
XC878-13FF 5V	$4B590463_H$
XC878M-13FF 5V	$4B590423_H$
XC878CM-13FF 5V	$4B590403_H$
XC878LM-13FF 5V	$4B510423_H$
XC878CLM-13FF 5V	$4B510403_H$
XC878-16FF 3V3	$4B180063_H$
XC878M-16FF 3V3	$4B180023_H$
XC878CM-16FF 3V3	$4B180003_H$
XC878-13FF 3V3	$4B190463_H$
XC878M-13FF 3V3	$4B190423_H$
XC878CM-13FF 3V3	$4B190403_H$
XC874CM-16FV 5V	$4B580002_H$
XC874LM-16FV 5V	$4B500022_H$
XC874-16FV 5V	$4B580062_H$

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC87x.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC87x and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC87x and must be regarded for a system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC87x is designed in.

4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC87x. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 39 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
CPU Clock Frequency[1]	f_{CCLK}		26.67[2]	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC878/874...
		-40	105	°C	SAX-XC878...
		-40	125	°C	SAK-XC878/874...

1) f_{CCLK} is the input frequency to the XC800 core. Please refer to **Figure 22** for detailed description.

2) Default setting of f_{CCLK} upon reset is 24 MHz.

4.2.2 Supply Threshold Characteristics

Table 41 provides the characteristics of the supply threshold in the XC87x.

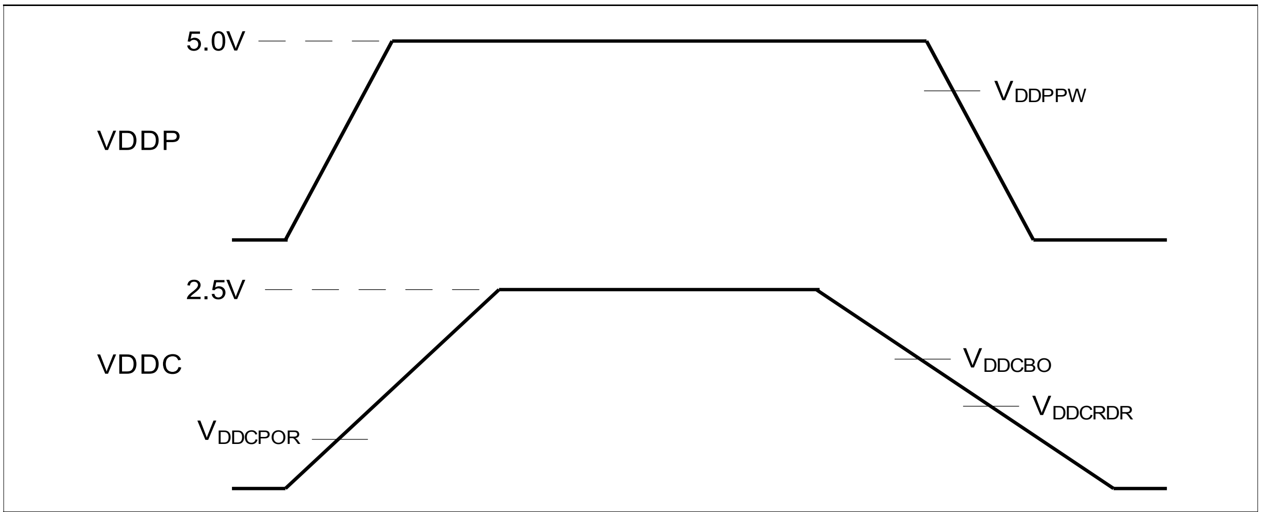

Figure 34 Supply Threshold Parameters

Table 41 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} brownout voltage[1]	V_{DDCBO}	CC	1.7	1.9	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	1.2	–	–	V
V_{DDP} prewarning voltage[2]	V_{DDPPW}	CC	3.8	4.2	4.5	V
Power-on reset voltage[1][3]	V_{DDCPOR}	CC	1.7	1.9	2.2	V

1) Detection is enabled in both active and power-down mode.

2) Detection is enabled for 5.0V power supply variant.
Detection is disabled for 3.3V power supply variant.

3) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

Table 42 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	[1)]
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	3	kΩ	[1)]

1) Not subjected to production test, verified by design/characterization.

2) This value includes the maximum oscillator deviation.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

4) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

4.3.6 External Clock Drive XTAL1

Table 52 shows the parameters that define the external clock supply for XC87x. These timing parameters are based on the direct XTAL1 drive of clock input signals. They are not applicable if an external crystal or ceramic resonator is considered.

Table 52 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Oscillator period	t_{osc}	SR	50	500	ns	1)2)
High time	t_1	SR	15	-	ns	2)3)
Low time	t_2	SR	15	-	ns	2)3)
Rise time	t_3	SR	-	10	ns	2)3)
Fall time	t_4	SR	-	10	ns	2)3)

1) The clock input signals with 45-55% duty cycle are used.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) The clock input signal must reach the defined levels V_{ILX} and V_{IHX}.

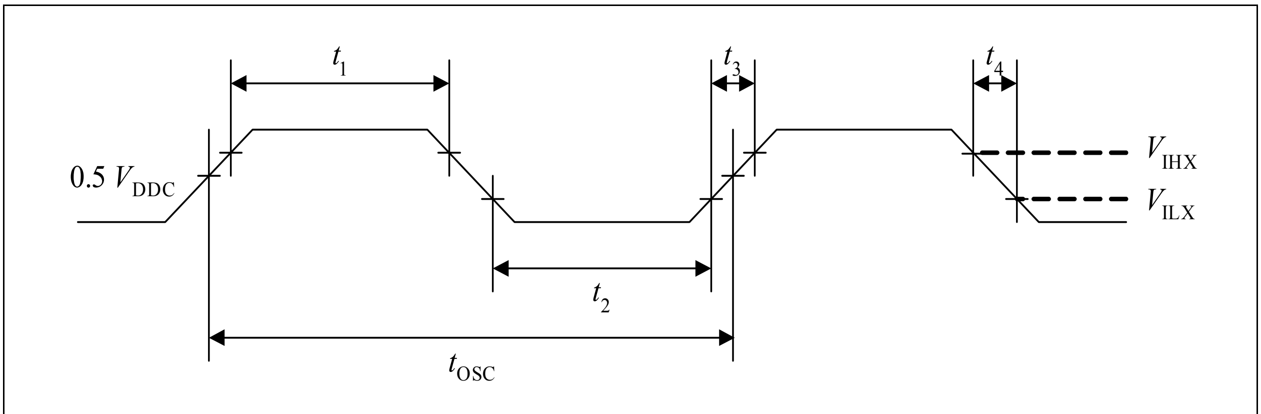

Figure 43 External Clock Drive XTAL1

5.3 Quality Declaration

Table 57 shows the characteristics of the quality parameters in the XC87x.

Table 57 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the two stated T_J[1]	t_{OP1}	-	15000	hours	T_J = 110°C
		-	2000	hours	T_J = -40°C
Operation Lifetime when the device is used at the five stated T_J[1]	t_{OP2}	-	120	hours	T_J = 140°C
		-	960	hours	T_J = 135°C
		-	7800	hours	T_J = 91°C
		-	2400	hours	T_J = 38°C
		-	720	hours	T_J = -25°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	750	V	Conforming to JESD22-C101-C

1) This lifetime refers only to the time when device is powered-on.