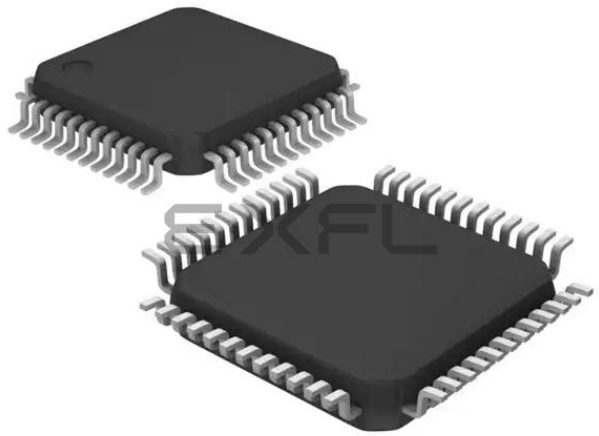


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	33
Program Memory Size	17.5KB (17.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini55lde

Table of Contents

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

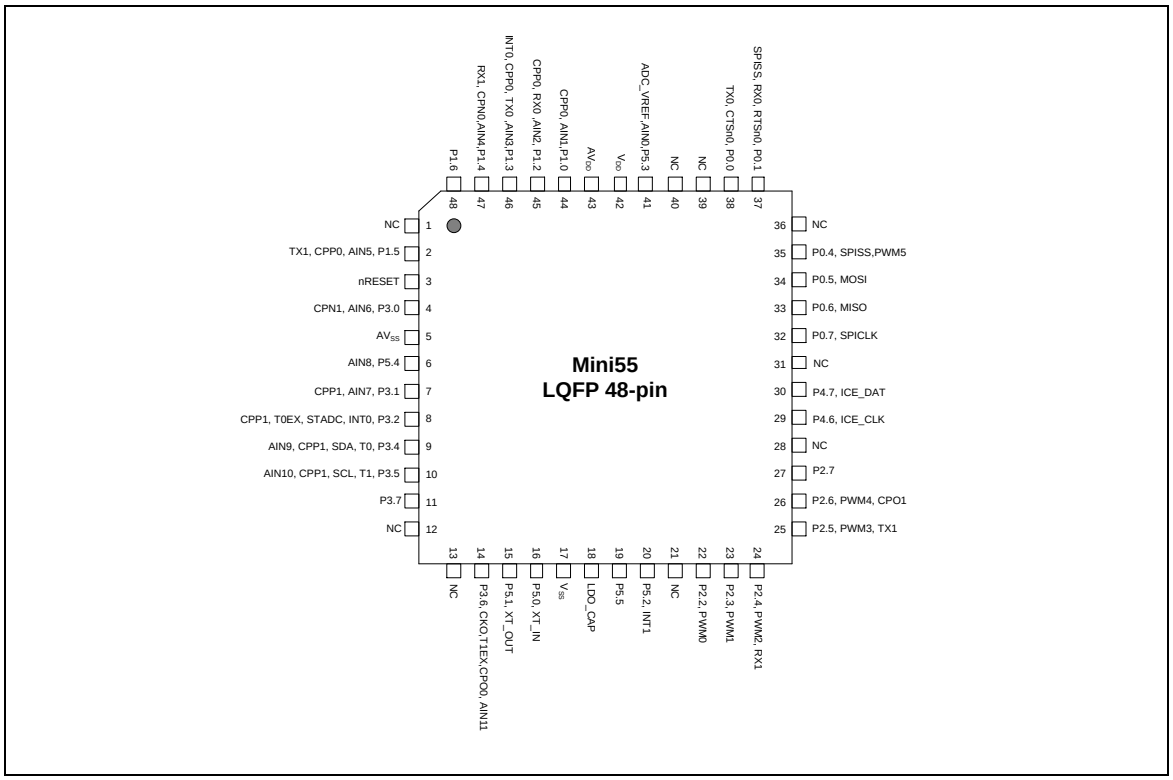


Figure 4.3-1 NuMicro® Mini55 Series LQFP 48-pin Diagram

- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

(CLK_CLKSEL1[1:0])								
XLTSTB **(CLK_STATUS[0])**	0x0	-	-	-	-	-	-	-
LIRCSTB **(CLK_STATUS[3])**	0x0							
HIRCSTB **(CLK_STATUS[4])**	0x0	-	-	-	-	-	-	-
CLKSFAIL **(CLK_STATUS[7])**	0x0	0x0	-	-	-	-	-	-
WDT_CTL	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
BS **(FMC_ISPCTL[1])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
ISPEN **(FMC_ISPCTL[16])**								
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS **(FMC_ISPSTS[2:1])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP **(FMC_ISPSTS[20:9])**	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

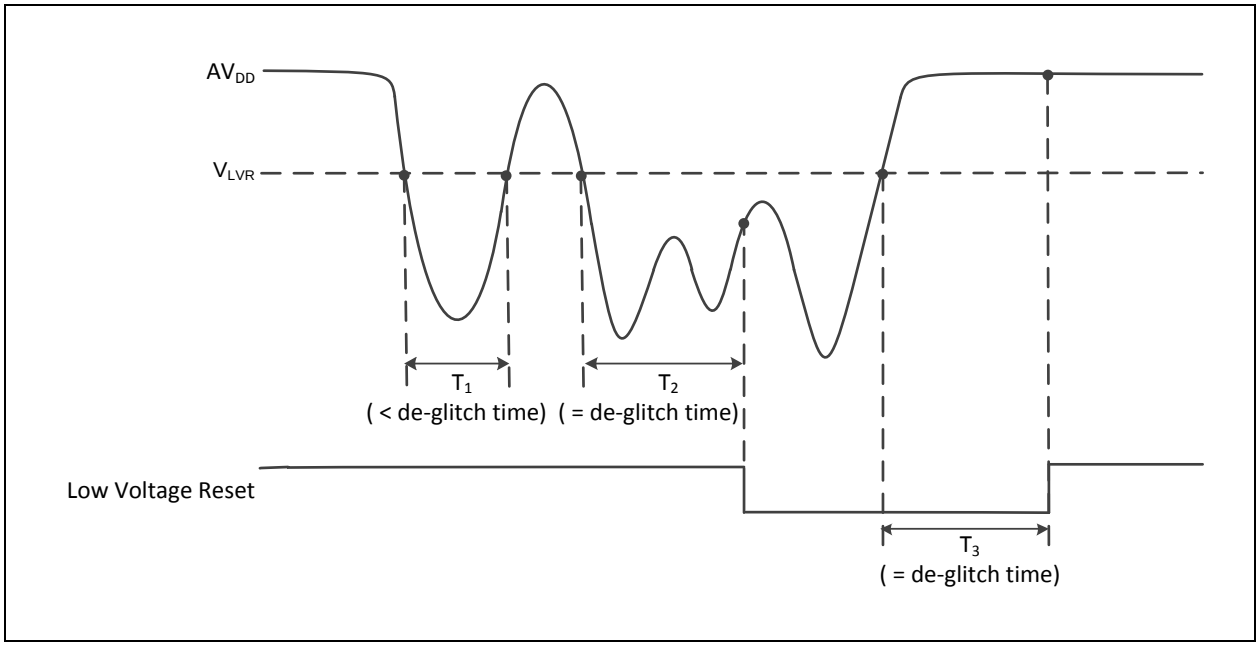


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Threshold Voltage Selection BODVL[1:0] (SYS_BODCTL[2:1]), BODVL[2] (SYS_BODCTL[7]) and Brown-Out Detector Selection Extension BODVLEXT (SYS_BODCTL[0]). Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset if BODRSTEN (SYS_BODCTL[3]) is enabled. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BODVL[1:0] (SYS_BODCTL[2:1]), BODVL[2] (SYS_BODCTL[7]), BODVLEXT (SYS_BODCTL[0]) and BODRSTEN (SYS_BODCTL[3]) is set by flash controller user configuration register CBOVEXT (CONFIG0 [23]), CBOV[1:0] (CONFIG0 [22:21]), CBOV[2] (CONFIG0 [19]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-Out Detector waveform.

	Normal Mode	Idle Mode	Power-down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
UART	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD and GPIO

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN (CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-up Source	Wake-up condition	System can enter Power-down mode again condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear SYS_BODCTL[BODIF].
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).

6.2.5 System Memory Mapping

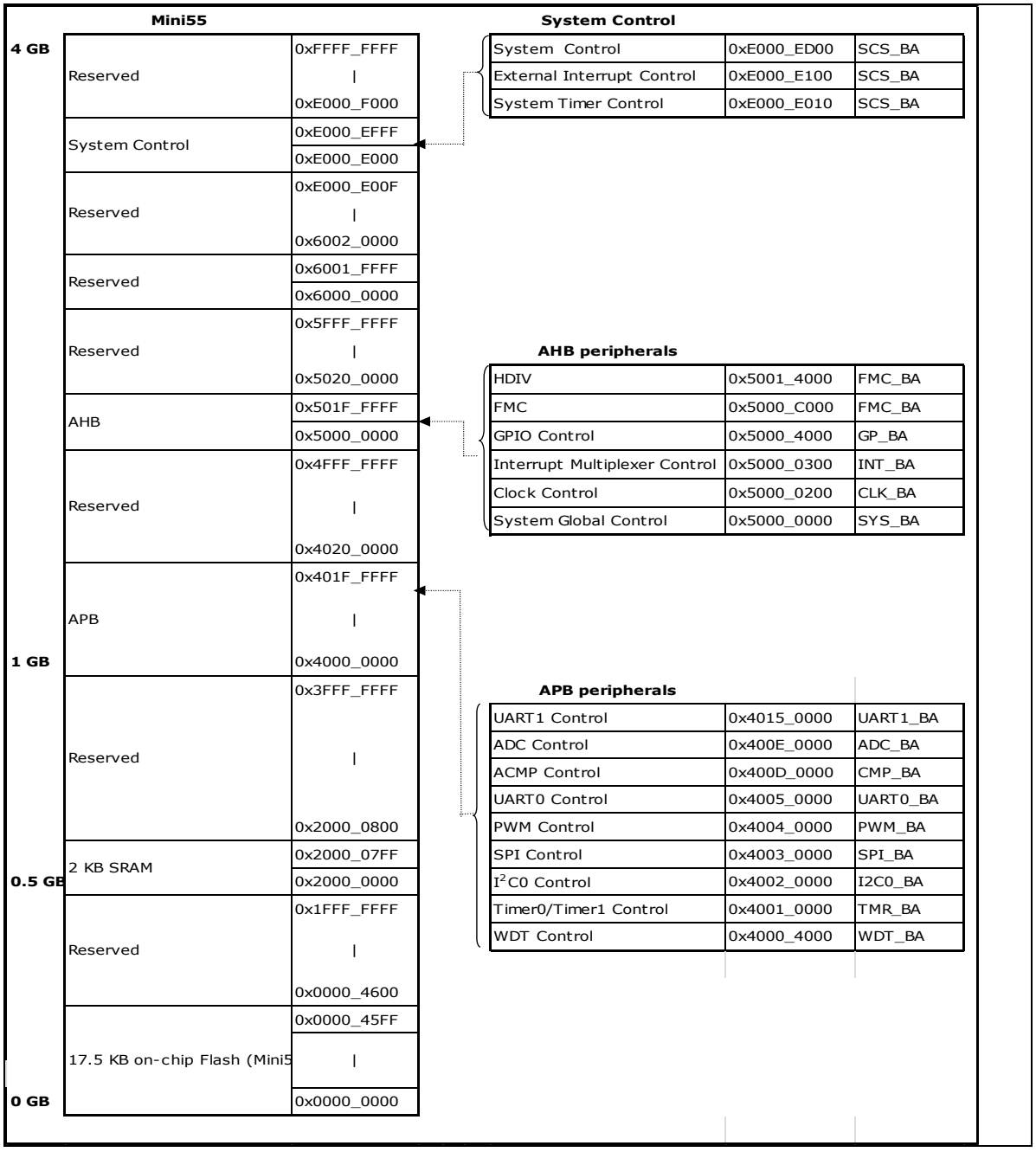


Table 6.2-5 Memory Mapping Table

6.2.6 Memory Organization

6.2.6.1 Overview

The NuMicro® Mini55 series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown in Table 6.2-6. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The Mini55 series only supports little-endian data format.

6.2.9 System Control Registers (SCB)

The Cortex®-M0 status and operating mode control are managed System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3.2 Auto-trim

This chip supports auto-trim function: the HIRC trim (48 MHz internal RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 1 % deviation within all temperature ranges. For instance, the system needs an accurate 48 MHz clock. In such case, if users do not want to use 48 MHz HXT as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL[0] trim frequency selection) to “1”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) high indicates the HIRC output frequency is accurate within 1% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

6.3.3 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

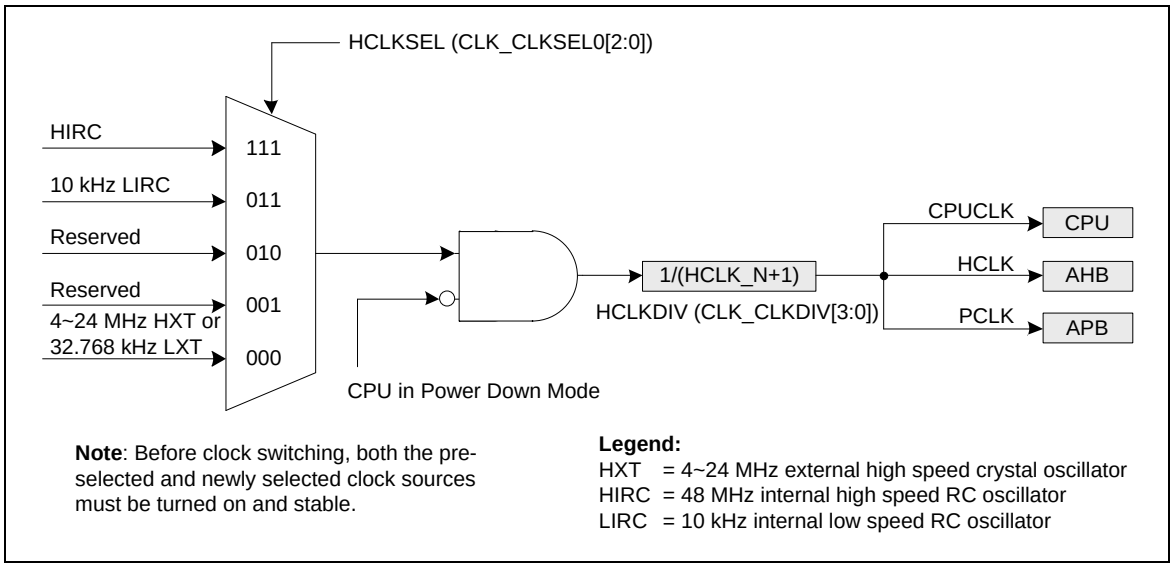


Figure 6.3-3 System Clock Block Diagram

The source of PCLK is equal to HCLK in system clock architecture.

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock CLKSRC(SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

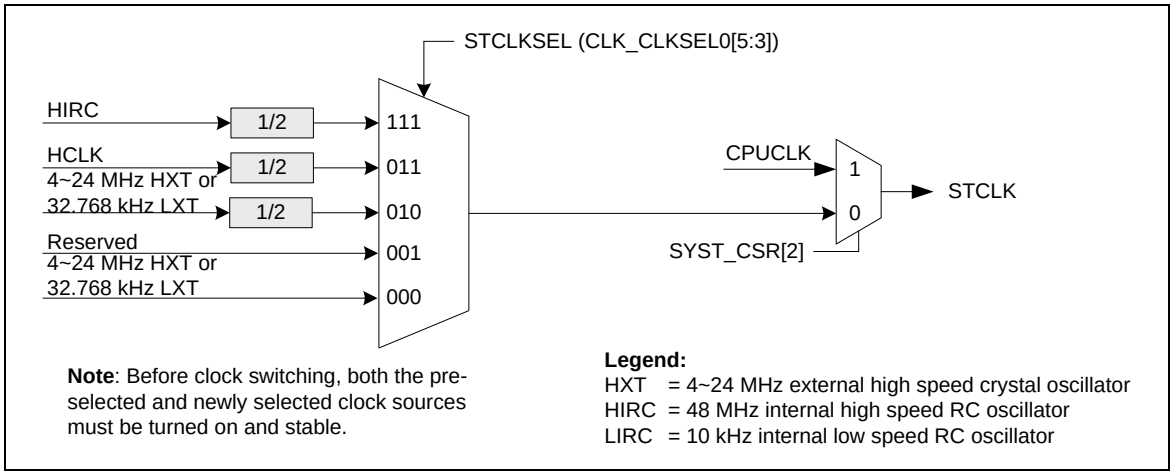


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLK_CLKSEL1 and CLK_APBCLK register description in NuMicro® Mini55 Series Technical Reference Manual section 6.3.8. Please to note that, while switching clock source from one to another, user must wait until both clock sources are running stabled.

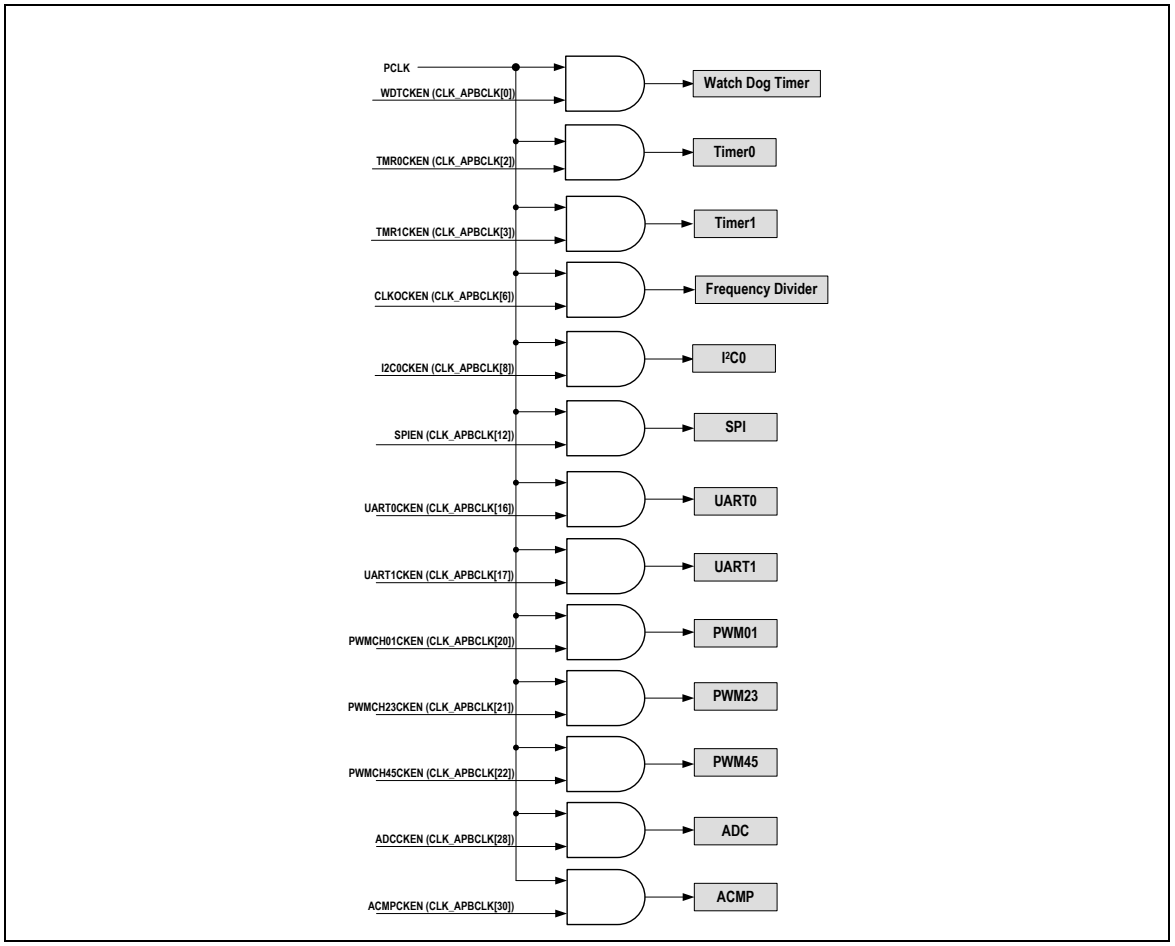


Figure 6.3-5 Peripherals Bus Clock Source Selection for PCLK

	Peripheral Clok Selectable	Ext. CLK (HXT Or LXT)	HIRC	LIRC	HCLK
WDT	Yes	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes	Yes
I^2C0	No	-	-	-	-
SPI	Yes	Yes	No	No	Yes
UART0	Yes	Yes	Yes	No	No
UART1	Yes	Yes	Yes	No	No
PWM	No	-	-	-	-
ADC	Yes	Yes	Yes	No	Yes
ACMP	No	-	-	-	-

Table 6.3-1 Peripheral Clock Source Selection Table

Note: For the peripherals those peripheral clock are not selectable, its clock source is fixed to PCLK.

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CLKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

6.6 Timer Controller (TMR)

6.6.1 Overview

The Timer Controller includes two 32-bit timers, TMR0 and TMR1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Two sets of 32-bit timer with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMRTx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports internal capture triggered while internal ACMP output signal transition

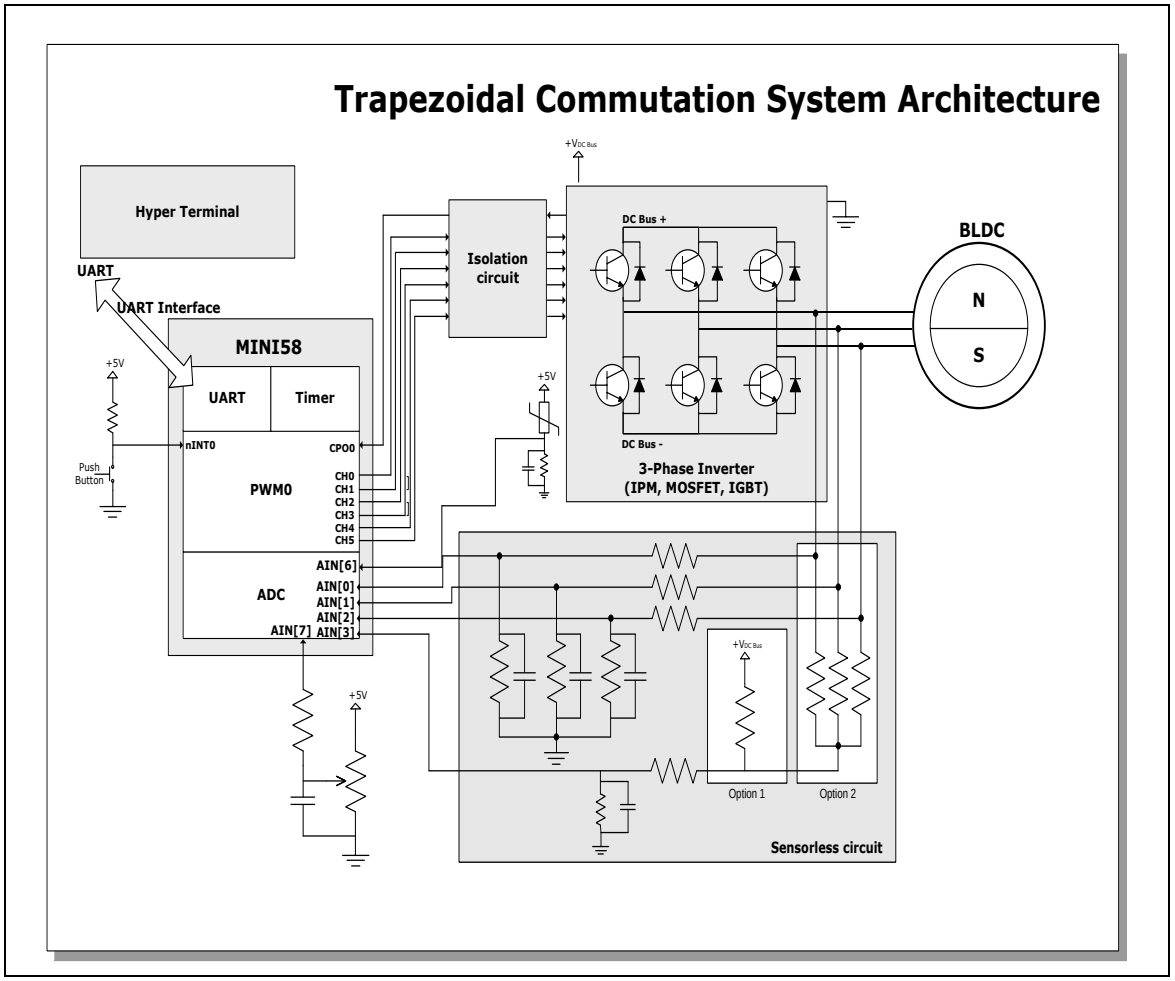


Figure 6.7-1 Application Circuit Diagram

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycles and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.10 I²C Serial Interface Controller (I²C)

6.10.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method for data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There are two sets of I²C controller and only I²C0 supports Power-down wake-up function.

6.10.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function
- Supports two-level buffer function

6.13 Analog Comparator (ACMP)

6.13.1 Overview

The NuMicro® Mini55 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input is greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.13.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input
- ACMP0 supports:
  - Four positive sources
    - P1.5, P1.0, P1.2, or P1.3
  - Three negative sources
    - P1.4
    - Internal Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
- ACMP1 supports:
  - Four positive sources
    - P3.1, P3.2, P3.4, or P3.5
  - Three negative sources
    - P3.0
    - Internal Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

I_{DD16}		-	6.9	-	mA	3.3V	X	V	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 22.1184 MHz while(1){} Executed from Flash	-	9.3	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{DD18}		-	6.7	-	mA	5.5V	X	V	X	X
I_{DD19}		-	9.0	-	mA	3.3V	X	V	X	V
I_{DD20}		-	6.5	-	mA	3.3V	X	V	X	X
I_{DD21}	Operating Current Normal Run Mode HCLK = 12MHz while(1){} Executed from Flash	-	4.5	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	12 MHz	X	X	V
I_{DD22}		-	3.5	-	mA	5.5V	12 MHz	X	X	X
I_{DD23}		-	4.5	-	mA	3.3V	12 MHz	X	X	V
I_{DD24}		-	3.5	-	mA	3.3V	12 MHz	X	X	X
I_{DD25}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	2.0	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	4 MHz	X	X	V
I_{DD26}		-	1.6	-	mA	5.5V	4 MHz	X	X	X
I_{DD27}		-	2.0	-	mA	3.3V	4 MHz	X	X	V
I_{DD28}		-	1.6	-	mA	3.3V	4 MHz	X	X	X
I_{DD29}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	100	-	µA	V_{DD}	HXT	LIRC	PLL	All Digital Modules
						5.5V	X	V	X	V[4]
I_{DD30}		-	100	-	µA	5.5V	X	V	X	X
I_{DD31}		-	90	-	µA	3.3V	X	V	X	V[4]
I_{DD32}		-	90	-	µA	3.3V	X	V	X	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 48 MHz	-	10.0	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{IDLE2}		-	4.6	-	mA	5.5V	X	V	X	X
I_{IDLE3}		-	9.6	-	mA	3.3V	X	V	X	V
I_{IDLE4}		-	4.5	-	mA	3.3V	X	V	X	X
I_{IDLE5}	Operating Current	-	9.3	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules

8.5 Flash DC Electrical Characteristics

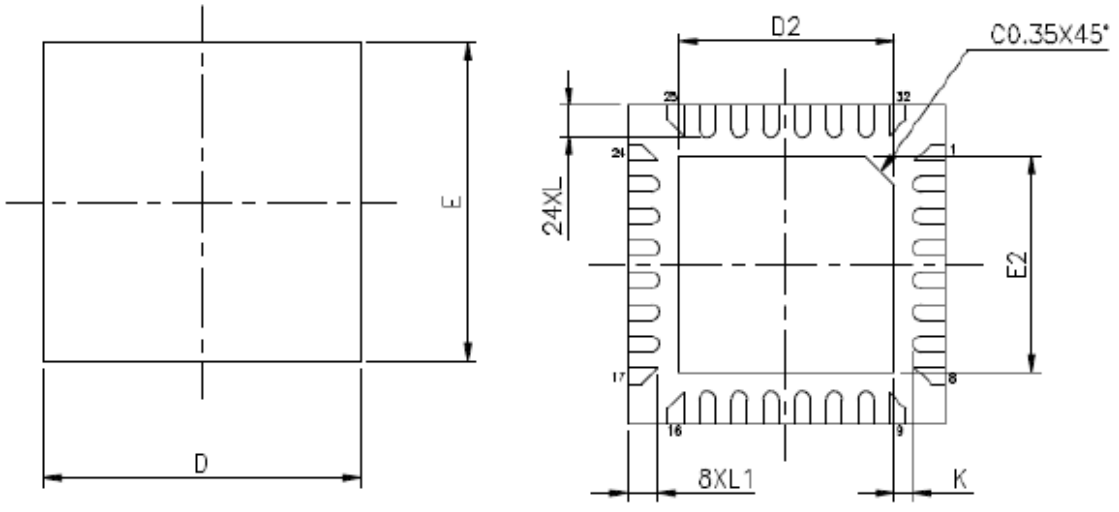
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-	6	-	ms	
T_{PROG}	Program Time	-	7.5	-	us	
I_{DD1}	Read Current	-	4	-	mA	
I_{DD2}	Program Current	-	3.5	-	mA	
I_{DD3}	Erase Current	-	2	-	mA	

Note1: Number of program/erase cycles.

Note2: V_{FLA} is source from chip LDO output voltage.

Note3: Guaranteed by design, not test in production.

9.3 33-pin QFN (4 mm x 4 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.35	0.40	0.45
K	0.20	—	—

Symbol	Dimension in mm		
	MIN.	NOR.	MAX.
D2	2.6	2.7	2.8
E2	2.6	2.7	2.8