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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini55zde

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2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage: 2.1V to 5.5V
- Memory
  - 17.5 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - Support 4 ~ 24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Support 32.768 kHz external low speed crystal oscillator (LXT) for idle wake-up and system operation clock
  - Built-in 48 MHz internal high speed RC oscillator (HIRC) for system operation (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±2% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
- I/O Port
  - Up to 33 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional Schmitt trigger input
- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer
    - Supports Event Counter mode

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition (four slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 500 kSPS
  - Up to 12-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger or external pin trigger
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.4V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V/1.7V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 3KV, ESD HBM pass 6KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (4x4)

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

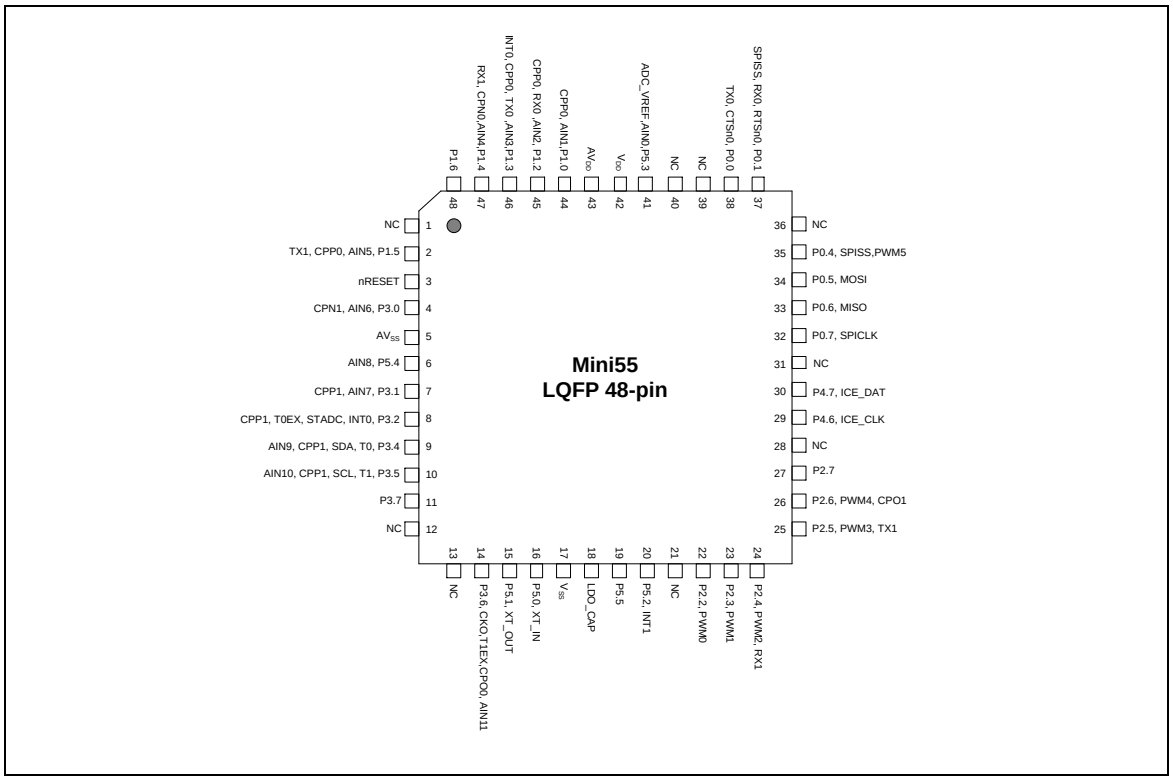


Figure 4.3-1 NuMicro® Mini55 Series LQFP 48-pin Diagram

		PWM0	O	PWM0 output of PWM unit
23	15	P2.3	I/O	General purpose digital I/O pin
		PWM1	O	PWM1 output of PWM unit
24	16	P2.4	I/O	General purpose input/output digital pin
		PWM2	O	PWM2 output of PWM unit
		RX1	I	UART1 data receiver input pin
25	17	P2.5	I/O	General purpose digital I/O pin
		PWM3	O	PWM3 output of PWM unit
		TX1	O	UART1 transmitter output pin
26	18	P2.6	I/O	General purpose digital I/O pin
		PWM4	O	PWM4 output of PWM unit
		ACMP1_O	O	Analog comparator output pin
27		P2.7	I/O	General purpose digital I/O pin
28		NC		Not connected
29	19	P4.6	I/O	General purpose digital I/O pin
		ICE_CLK	I	Serial wired debugger clock pin
30	20	P4.7	I/O	General purpose digital I/O pin
		ICE_DAT	I/O	Serial wired debugger data pin
31		NC		Not connected
32	21	P0.7	I/O	General purpose digital I/O pin
		SPICLK	I/O	SPI serial clock pin
33	22	P0.6	I/O	General purpose digital I/O pin
		MISO	I/O	SPI MISO (master in/slave out) pin
34	23	P0.5	I/O	General purpose digital I/O pin
		MOSI	O	SPI MOSI (master out/slave in) pin
35	24	P0.4	I/O	General purpose digital I/O pin
		SPISS	I/O	SPI slave select pin
		PWM5	O	PWM5 output of PWM unit
36		NC		Not connected
37	25	P0.1	I/O	General purpose digital I/O pin
		RTSn	O	UART0 RTS pin

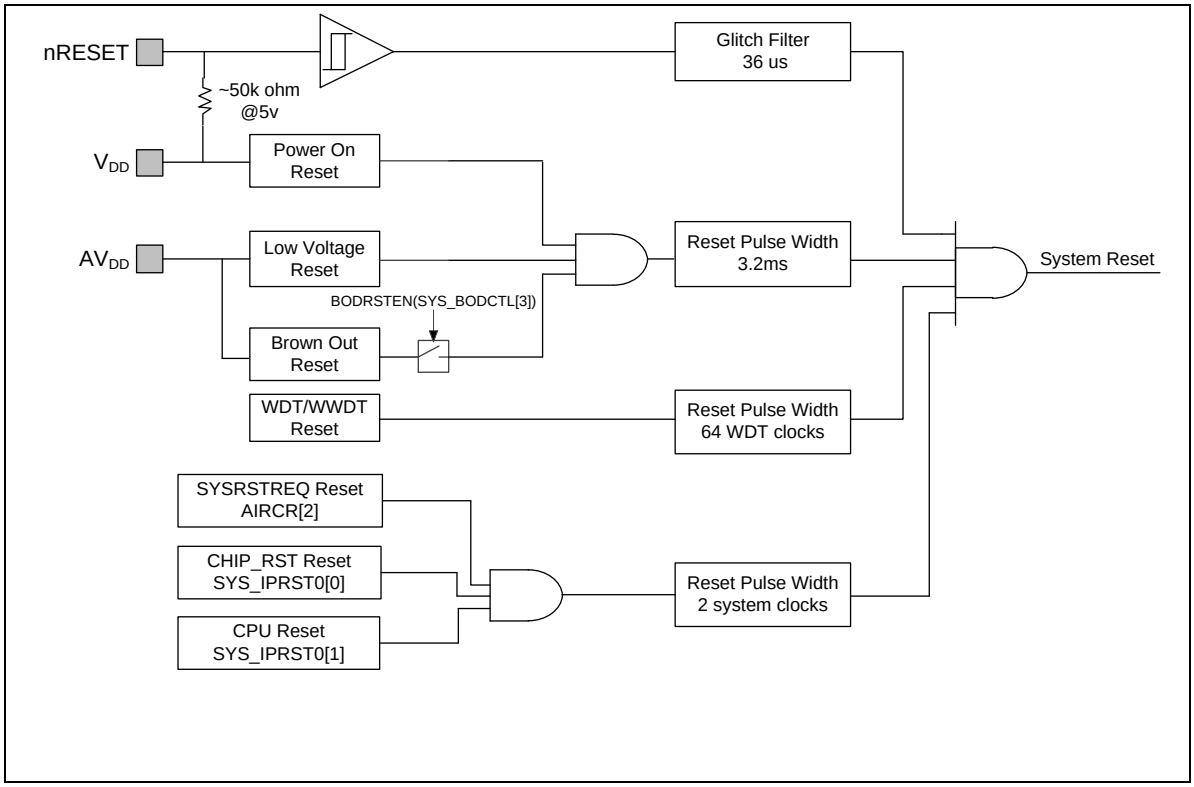


Figure 6.2-1 System Rese Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex-M0 only; the other reset sources will reset Cortex-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	0x001	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])								
BODRSTEN (SYS_BODCTL[3])								
XTLEN (CLK_PWRCTL[1:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x8	0x8	0x8	0x8	0x8	0x8	0x8	-
WDTSEL	0x3	0x3	-	-	-	-	-	-

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-7 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-down Wake-up
1 ~ 15	-	**-**	-	System exceptions	-
16	0	**BODOUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM Brake interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	**-**	-	-	
28	12	**UART0_INT**	UART0	UART0 interrupt	Yes
29	13	**UART1_INT**	UART1	UART1 interrupt	Yes
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	**-**	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt	Yes

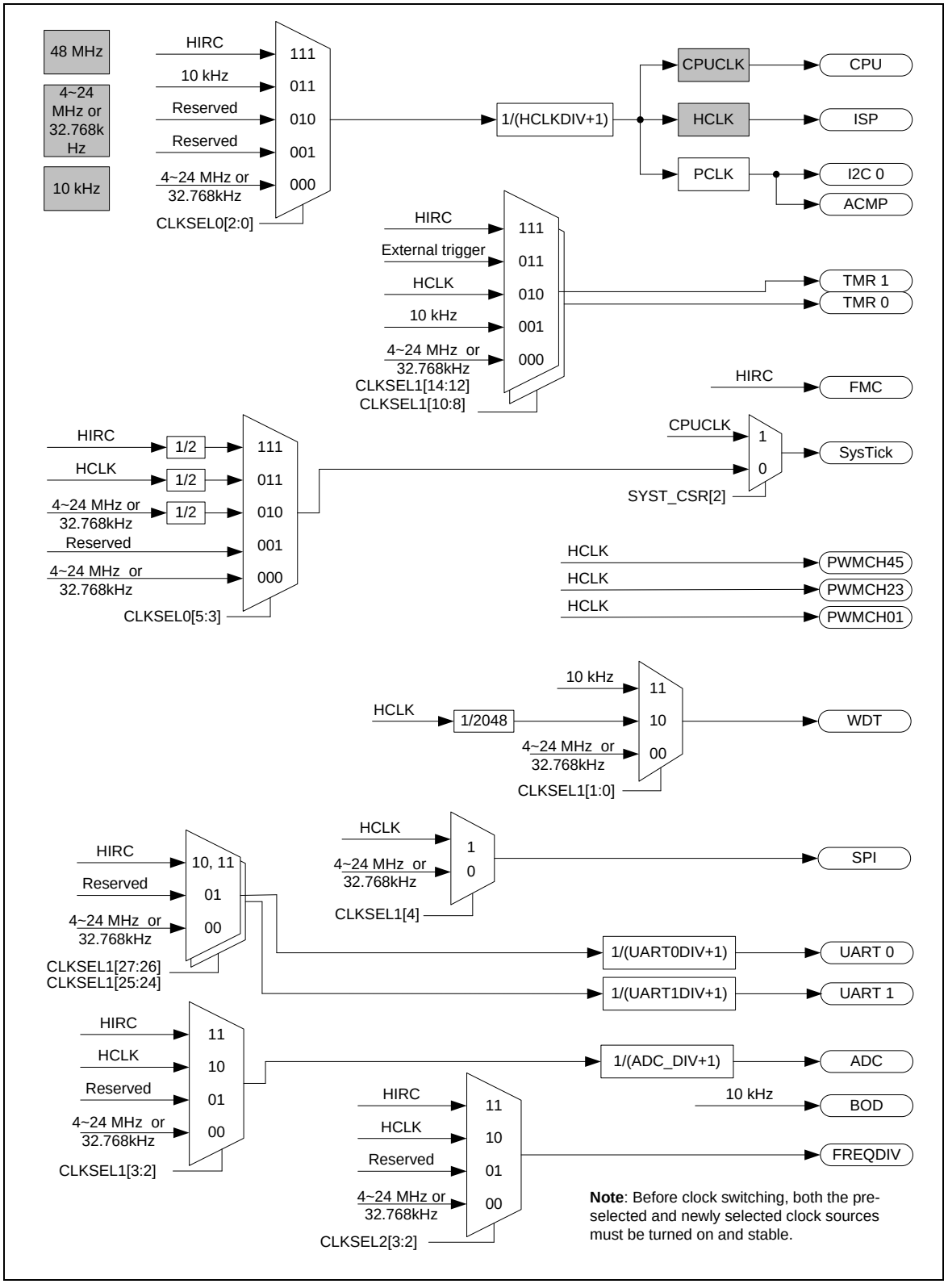


Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 Auto-trim

This chip supports auto-trim function: the HIRC trim (48 MHz internal RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 1 % deviation within all temperature ranges. For instance, the system needs an accurate 48 MHz clock. In such case, if users do not want to use 48 MHz HXT as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL[0] trim frequency selection) to “1”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) high indicates the HIRC output frequency is accurate within 1% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

6.3.3 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

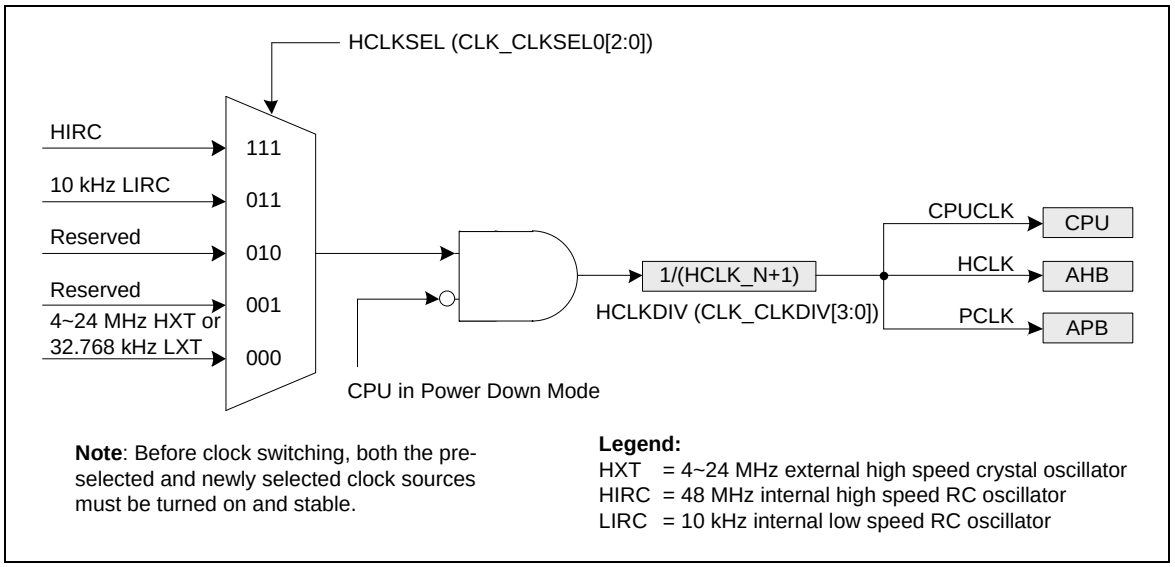


Figure 6.3-3 System Clock Block Diagram

The source of PCLK is equal to HCLK in system clock architecture.

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock CLKSRC(SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

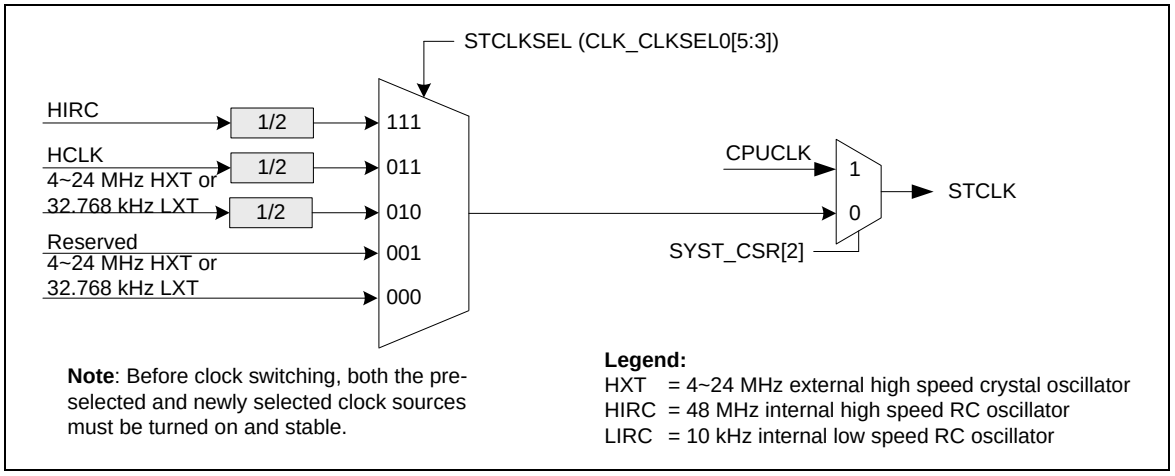


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLK_CLKSEL1 and CLK_APBCLK register description in NuMicro® Mini55 Series Technical Reference Manual section 6.3.8. Please to note that, while switching clock source from one to another, user must wait until both clock sources are running stabled.

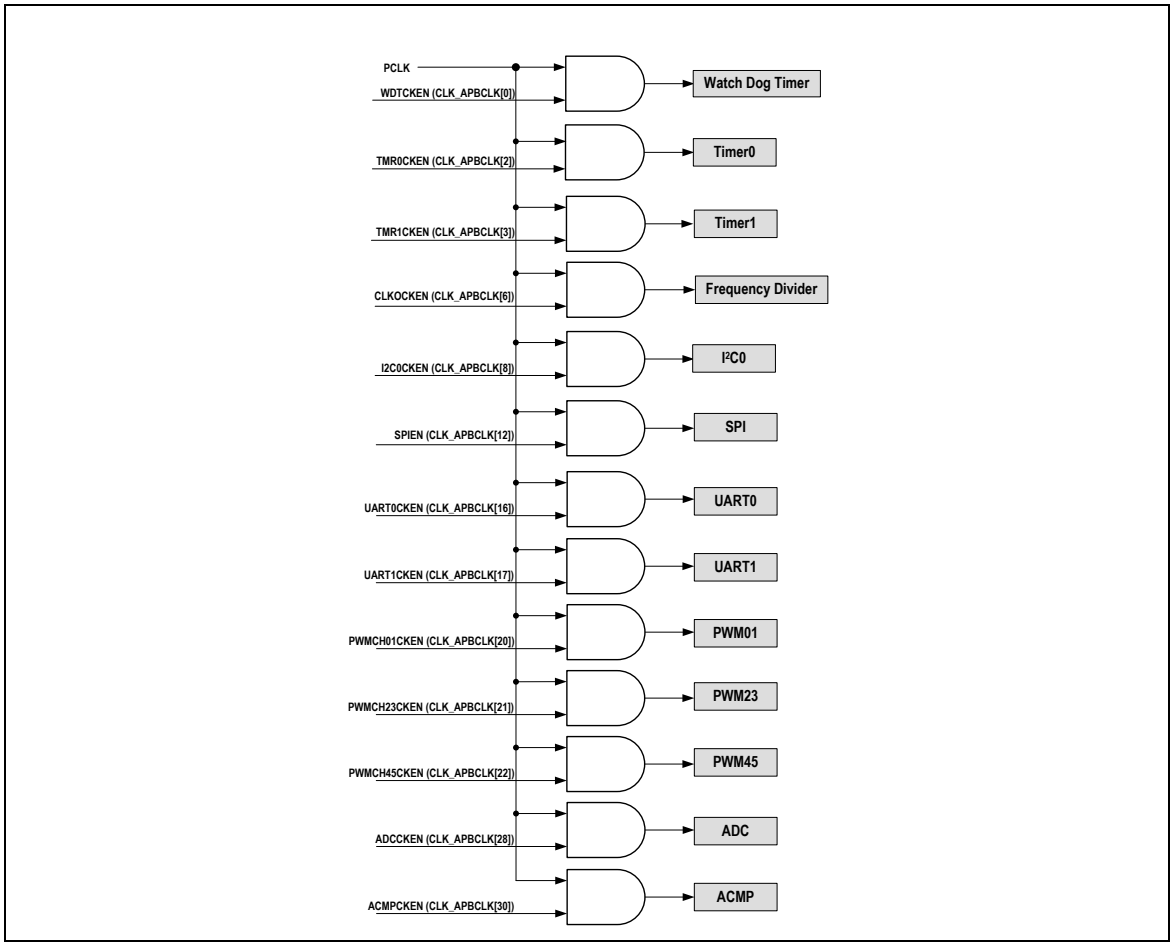


Figure 6.3-5 Peripherals Bus Clock Source Selection for PCLK

	Peripheral Clok Selectable	Ext. CLK (HXT Or LXT)	HIRC	LIRC	HCLK
WDT	Yes	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes	Yes
I^2C0	No	-	-	-	-
SPI	Yes	Yes	No	No	Yes
UART0	Yes	Yes	Yes	No	No
UART1	Yes	Yes	Yes	No	No
PWM	No	-	-	-	-
ADC	Yes	Yes	Yes	No	Yes
ACMP	No	-	-	-	-

Table 6.3-1 Peripheral Clock Source Selection Table

Note: For the peripherals those peripheral clock are not selectable, its clock source is fixed to PCLK.

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CLKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® Mini55 series has up to 33 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 33 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 33 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins is stay in input mode and each port data register Px_DOUT[n] resets to 1. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.1 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-pull output
  - Open-drain output
  - Input-only with high impendence
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by SYS_Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- High driver and high sink I/O mode support
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in Input tri-state mode after chip reset

- Each pin of PWM0_CH0 to PWM0_CH5 has independent polarity setting control
- Hardware fault brake protections
  - Supports software trigger
  - Two Interrupt source types:
    - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned type) or underflow (edge-aligned type)
    - Requested when external fault brake asserted
      - BKP0: EINT0 or CPO1
      - BKP1: EINT1 or CPO0
- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register
- Supports mask aligned function
- Supports independently rising CMP matching, PERIOD matching, falling CMP matching (in Center-aligned type), period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

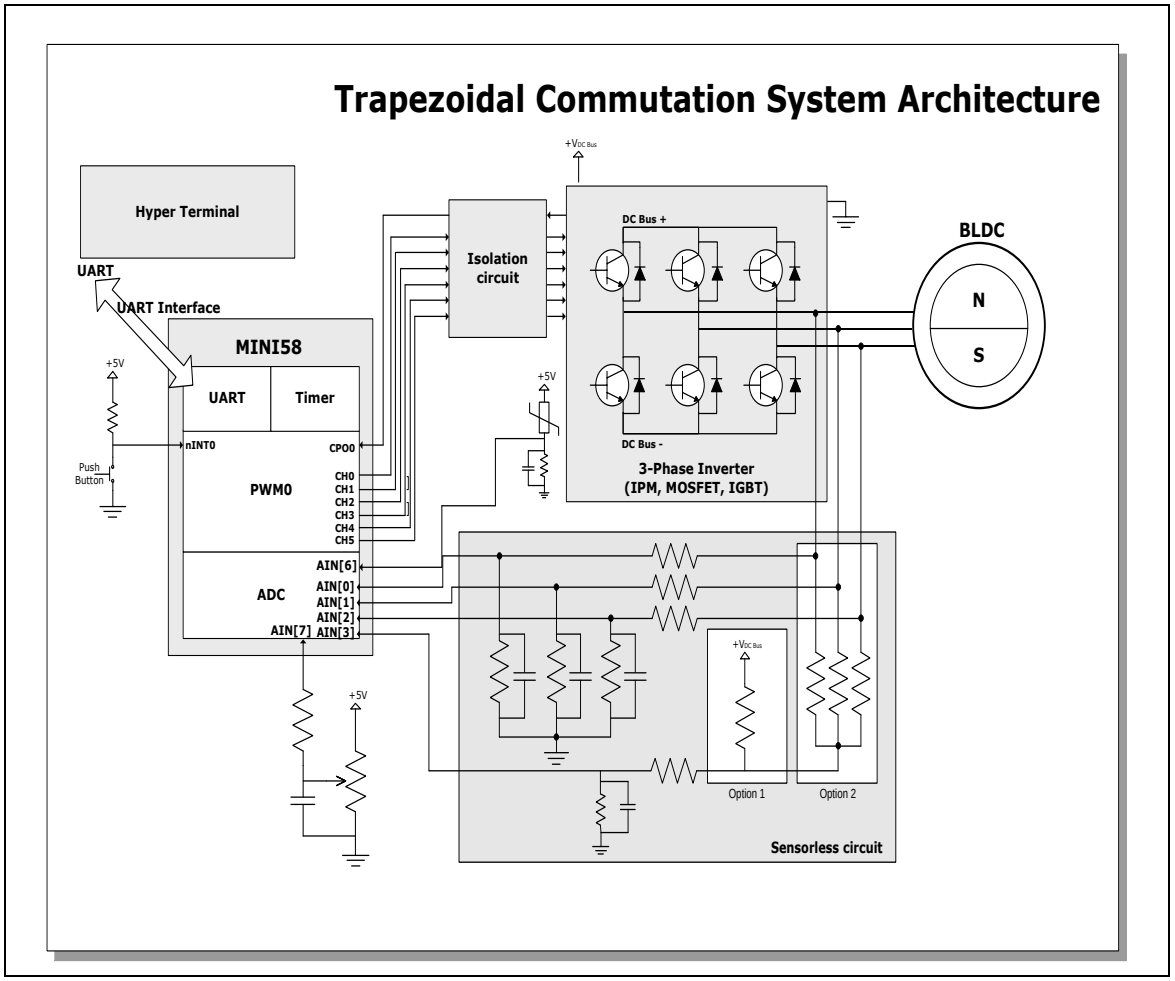


Figure 6.7-1 Application Circuit Diagram

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycles and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

	Idle Mode HCLK = 44.2368 MHz					5.5V	X	V	X	V
I_{IDLE6}		-	4.3	-	mA	5.5V	X	V	X	X
I_{IDLE7}		-	9.0	-	mA	3.3V	X	V	X	V
I_{IDLE8}		-	4.2	-	mA	3.3V	X	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 24MHz	-	4.0	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	24 MHz	X	X	V
I_{IDLE10}		-	2.2	-	mA	5.5V	24 MHz	X	X	X
I_{IDLE11}		-	4.0	-	mA	3.3V	24 MHz	X	X	V
I_{IDLE12}		-	2.0	-	mA	3.3V	24 MHz	X	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 24 MHz	-	6.1	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{IDLE14}		-	3.2	-	mA	5.5V	X	V	X	X
I_{IDLE15}		-	5.9	-	mA	3.3V	X	V	X	V
I_{IDLE16}		-	3.2	-	mA	3.3V	X	V	X	X
I_{IDLE17}	Operating Current Idle Mode HCLK=22.1184 MHz	-	5.7	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{IDLE18}		-	3.0	-	mA	5.5V	X	V	X	X
I_{IDLE19}		-	5.6	-	mA	3.3V	X	V	X	V
I_{IDLE20}		-	3.0	-	mA	3.3V	X	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	2.5	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE10}		-	1.5	-	mA	5.5V	V	X	X	X
I_{IDLE11}		-	2.5	-	mA	3.3V	V	X	X	V
I_{IDLE12}		-	1.5	-	mA	3.3V	V	X	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	1.5	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE14}		-	1.0	-	mA	5.5V	V	X	X	X

V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	μA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR12}		-50	-80	-	μA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR13}		-40	-73	-	μA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-Drain and Push-pull Mode)	10	15	-	mA	V_{DD} = 4.5 V, V_{SS} = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_{SS} = 0.45 V
I_{SK13}		5	8	-	mA	V_{DD} = 2.5 V, V_{SS} = 0.45 V

Note1: nRST pin is a Schmitt trigger input.

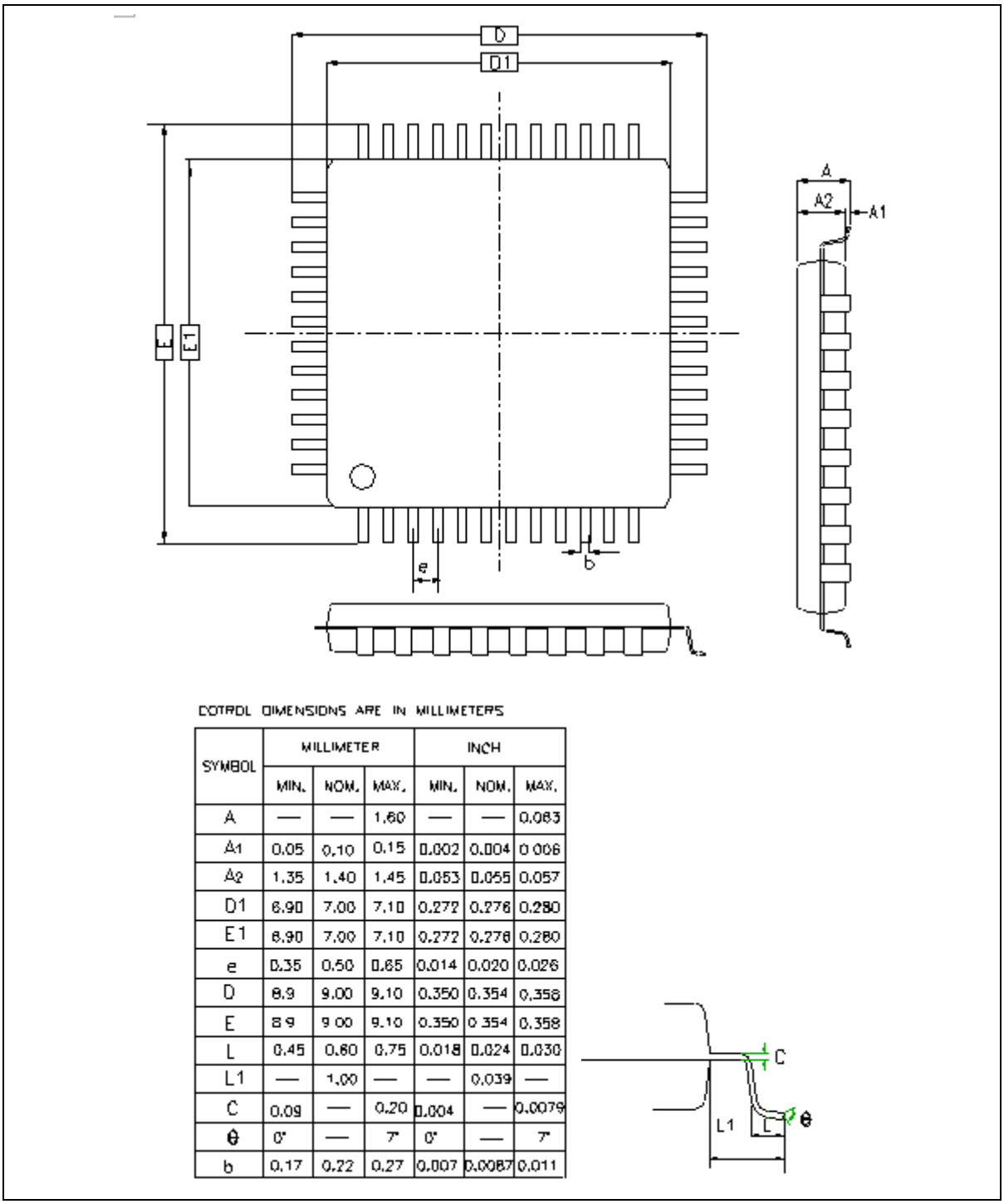
Note2: XT_IN is a CMOS input.

Note3: Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.

Note4: Only enable modules which support 10 kHz LIRC clock source

9 PACKAGE DIMENSIONS

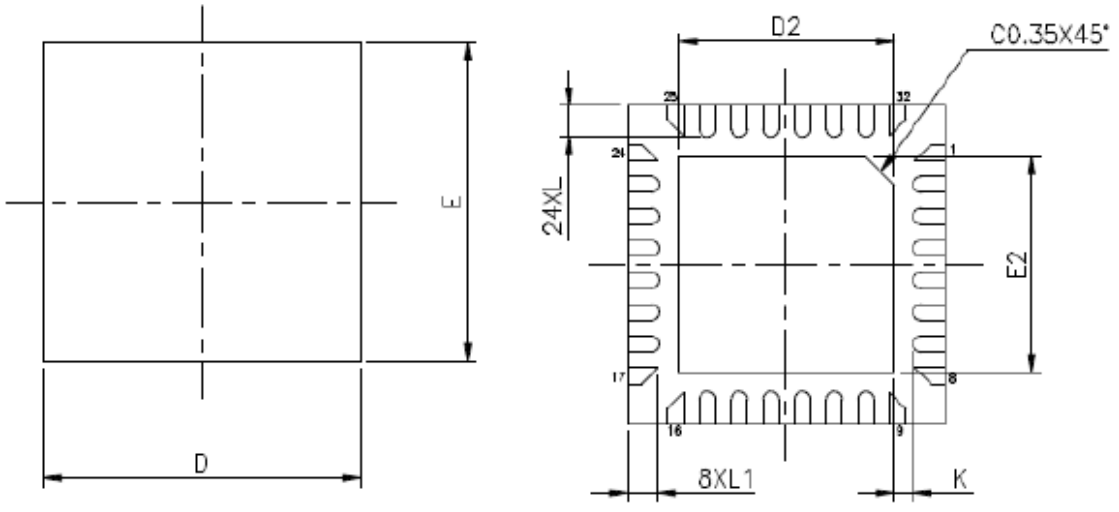
9.1 48-pin LQFP (7 mm x 7 mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

9.3 33-pin QFN (4 mm x 4 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.35	0.40	0.45
K	0.20	—	—

Symbol	Dimension in mm		
	MIN.	NOR.	MAX.
D2	2.6	2.7	2.8
E2	2.6	2.7	2.8