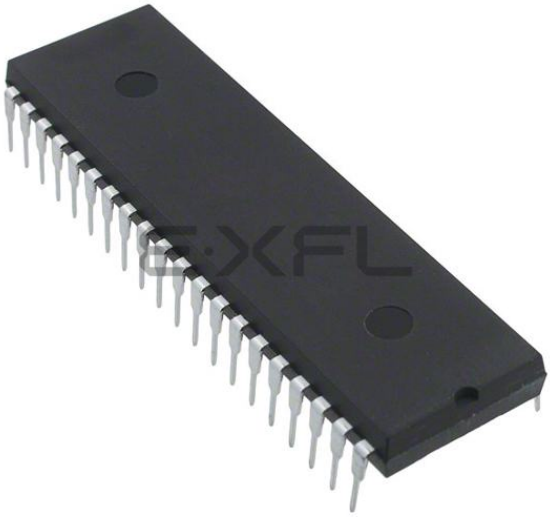

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Understanding Embedded - Microprocessors

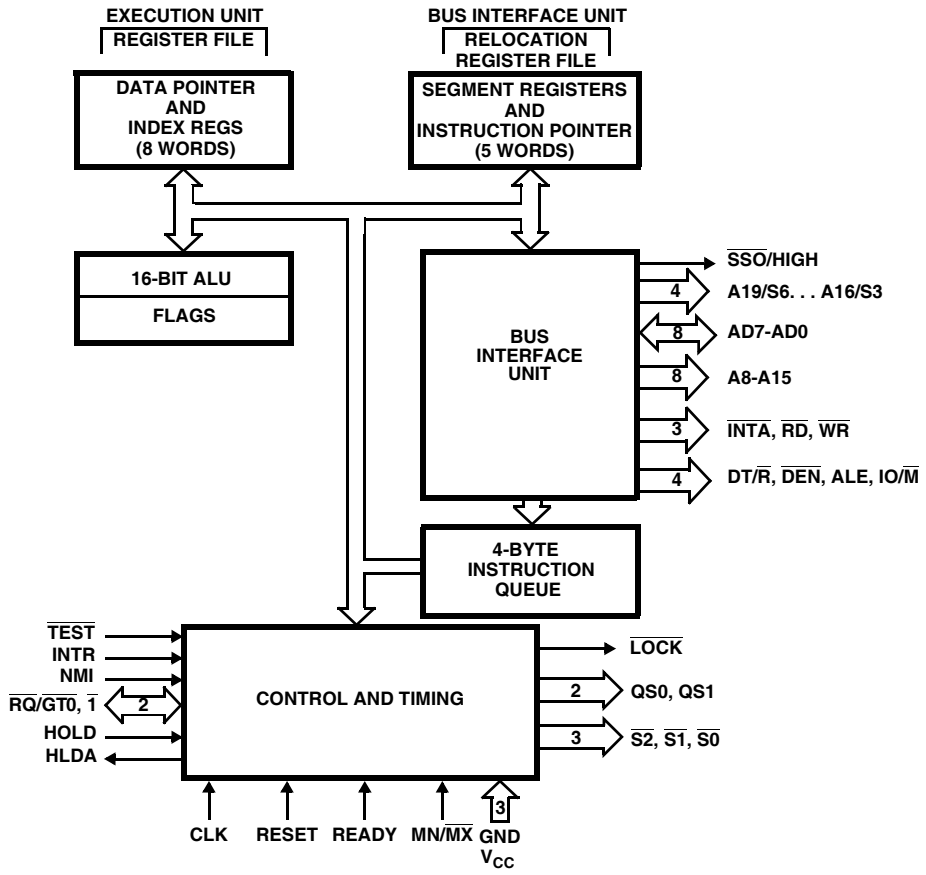
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

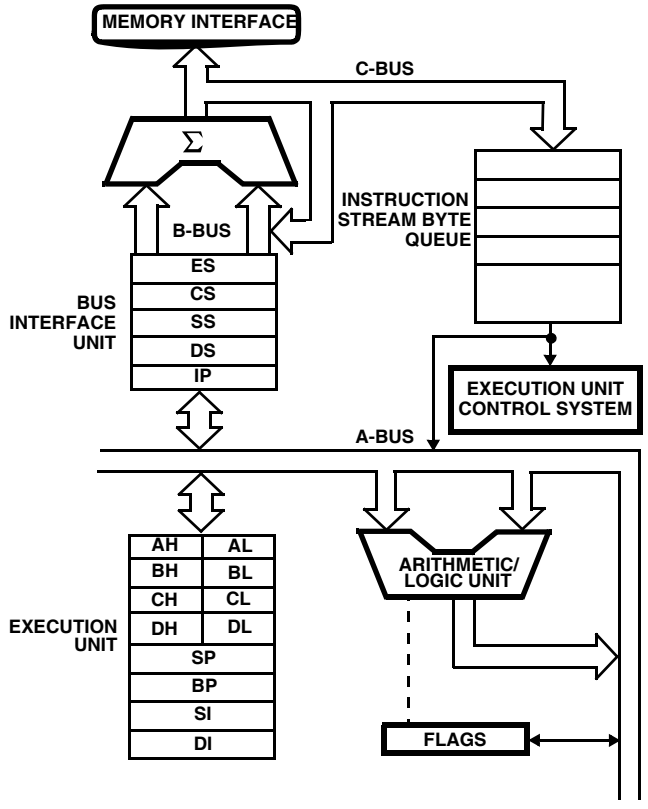
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	80C88
Number of Cores/Bus Width	1 Core, 16-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/cp80c88-2z

Functional Diagram





Pin Description

The following pin function descriptions are for 80C88 system in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to the minimum mode are described; all other pin functions are as described above.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
MINIMUM MODE SYSTEM (i.e., MN/$\overline{MX}$ = V_{CC})			
IO/$\overline{M}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ is held to a high impedance logic one during local bus “hold acknowledge”.
$\overline{WR}$	29	O	Write: strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and is held to high impedance logic one during local bus “hold acknowledge”.
$\overline{INTA}$	24	O	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and Tw of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an 82C86/82C87 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal is held to a high impedance logic one during local bus “hold acknowledge”.
$\overline{DEN}$	26	O	DATA ENABLE: is provided as an output enable for the 82C86/82C87 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to high impedance logic one during local bus “hold acknowledge”.
HOLD, HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus “hold”. To be acknowledged, HOLD must be active HIGH. The processor receiving the “hold” request will issue HLDA (HIGH) as an acknowledgment, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SS0}$	34	O	STATUS LINE: is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SS0}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status. $\overline{SS0}$ is held to high impedance logic one during local bus “hold acknowledge”.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	CHARACTERISTICS
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

Pin Description (Continued)

The following pin function descriptions are for 80C88 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to the maximum mode are described; all other pin functions are as described above.

<table>
<tr><th>SYMBOL</th><th>PIN NUMBER</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td colspan="4">MAXIMUM MODE SYSTEM (i.e., MN/$\overline{MX}$ = GND).</td></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>26
27
28</td><td>O
O
O</td><td>STATUS: is active during clock high of T4, T1 and T2, and is returned to the passive state (1, 1, 1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle.
These signals are held at a high impedance logic one state during “grant sequence”.
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>CHARACTERISTICS</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
</td></tr>
<tr><td>$\overline{RQ}$/$\overline{GT0}$,
RQ/GT1</td><td>31
30</td><td>I/O</td><td>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor’s current bus cycle. Each pin is bidirectional with $\overline{RQ}$/$\overline{GT0}$ having higher priority than $\overline{RQ}$/$\overline{GT1}$. $\overline{RQ}$/$\overline{GT}$ has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}$/$\overline{GT}$ Timing Sequence):
1. A pulse of one CLK wide from another local bus master indicates a local bus request (“hold”) to the 80C88 (pulse 1).
2. During a T4 or T1 clock cycle, a pulse one clock wide from the 80C88 to the requesting master (pulse 2), indicates that the 80C88 has allowed the local bus to float and that it will enter the “grant sequence” state at the next CLK. The CPUs bus interface unit is disconnected logically from the local bus during “grant sequence”.
3. A pulse one CLK wide from the requesting master indicates to the 80C88 (pulse 3) that the “hold” request is about to end and that the 80C88 can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending).
Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conjugations are met:
1. Request occurs on or before T2.
2. Current cycle is not the low bit of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>29</td><td>O</td><td>LOCK: indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the “LOCK” prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during “grant sequence”. In Max Mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.</td></tr>
</table>

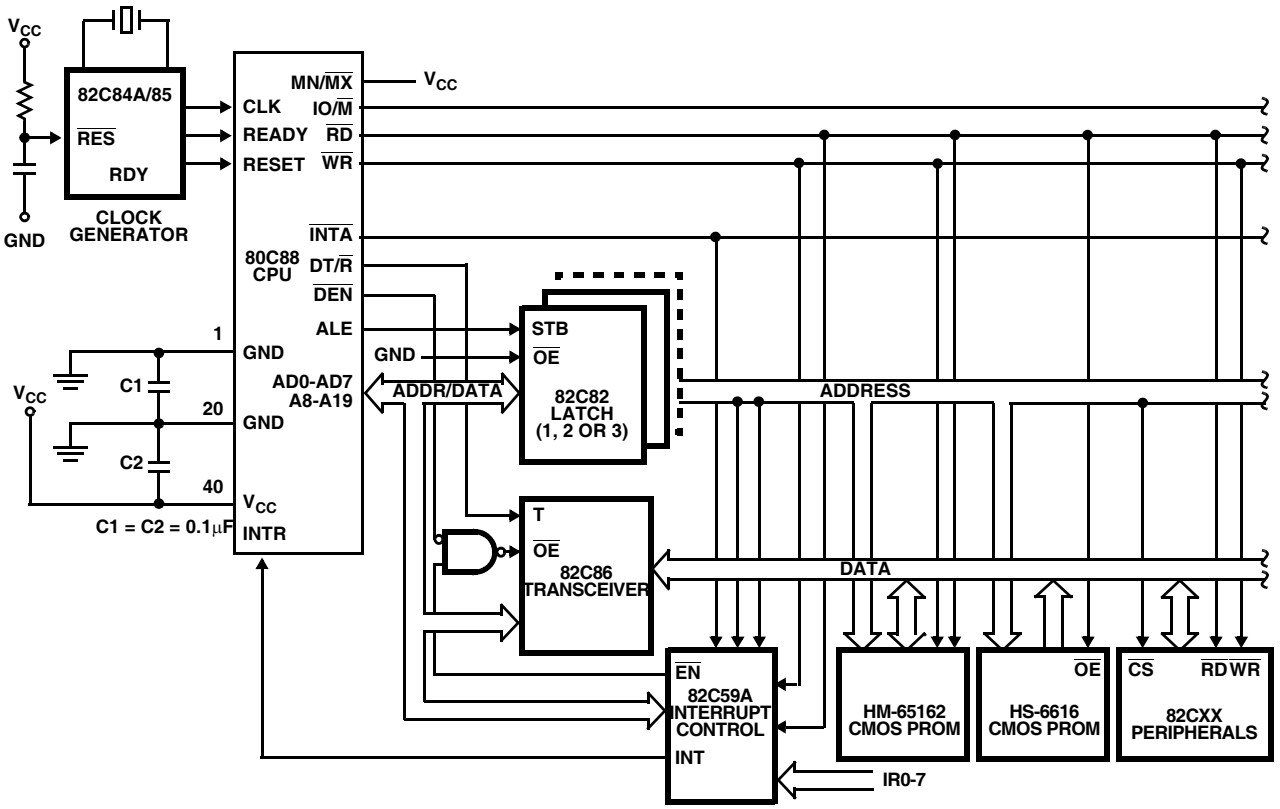


FIGURE 3. DEMULTIPLEXED BUS CONFIGURATION

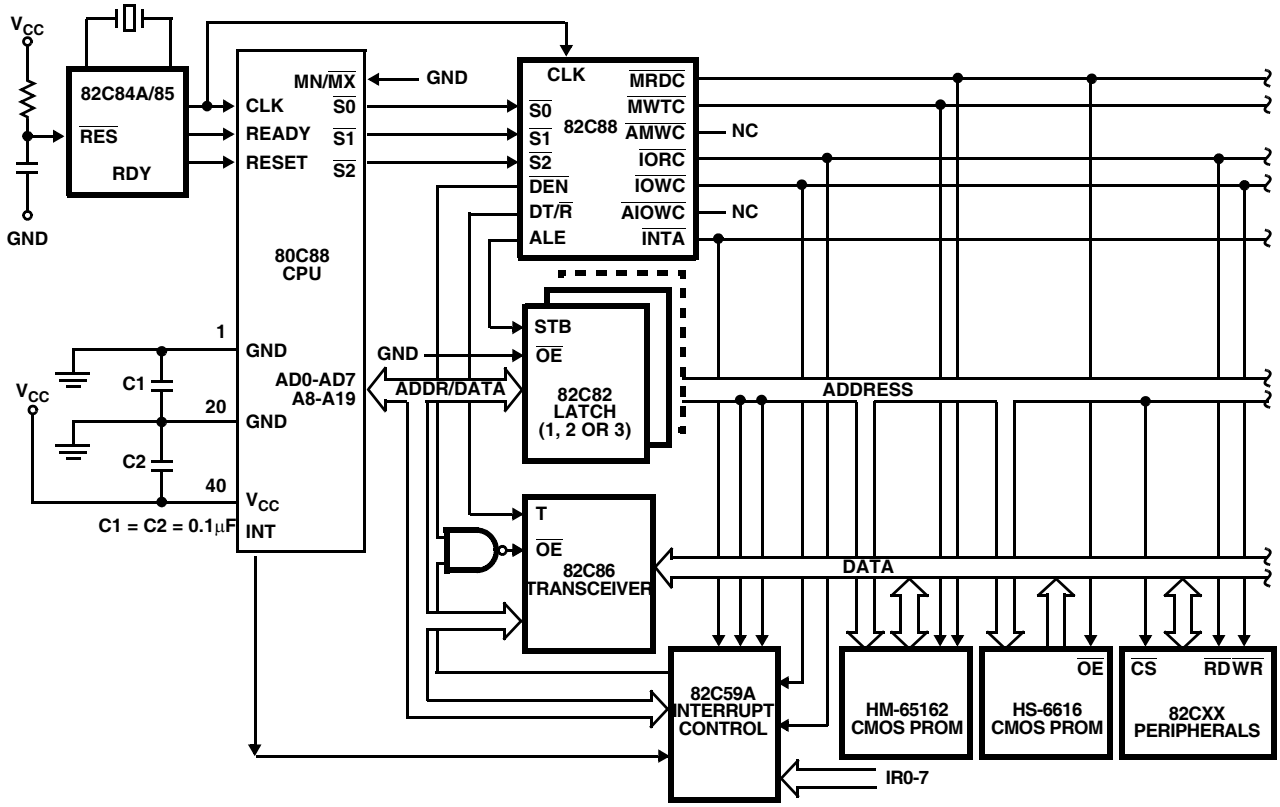


FIGURE 4. FULLY BUFFERED SYSTEM USING BUS CONTROLLER

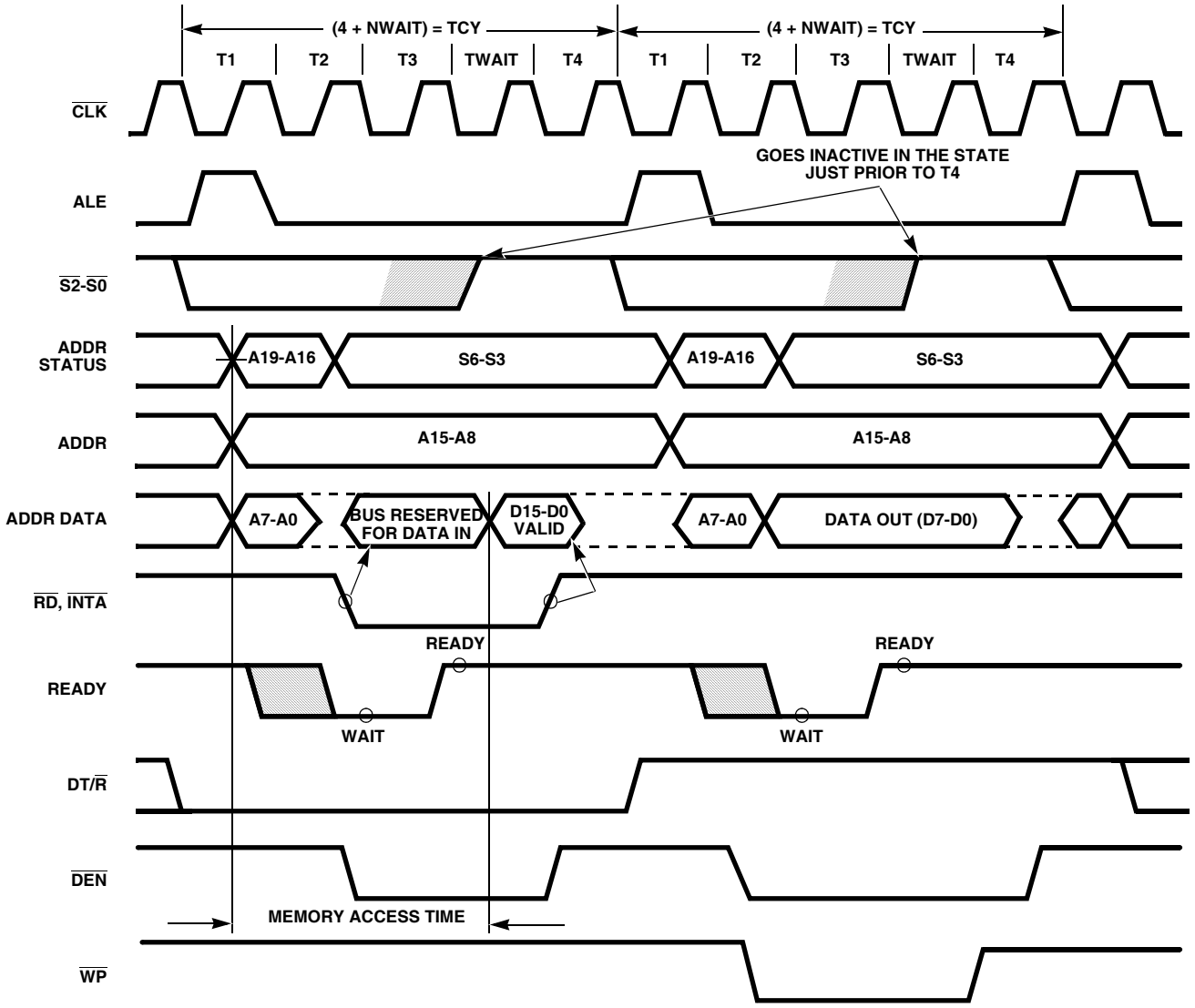


FIGURE 5. BASIC SYSTEM TIMING

TABLE 2.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

TABLE 3.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (Extra Segment)
0	1	Stack
1	0	Code or None
1	1	Data

I/O Addressing

In the 80C88, I/O operations can address up to a maximum of 64k I/O registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 80C88 uses a full 16-bit address on its lower 16 address lines.

External Interface

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C88 RESET is required to be HIGH for greater than four clock cycles. The 80C88 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 80C88 operates normally, beginning with the instruction in absolute location FFFFOH (see Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50μs after power up, to allow complete initialization of the 80C88.

NMI will not be recognized if asserted prior to the second CLK cycle following the end of RESET.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, “bus-hold” circuitry has been used on 80C88 pins 2-16, 26-32 and 34-39 (see Figure 6A and 6B). These circuits maintain a valid logic state if no driving source is present (i.e., an unconnected pin or a driving source which goes to a high impedance state).

To override the “bus hold” circuits, an external driver must be capable of supplying 400μA minimum sink or source current at valid input voltage levels. Since this “bus hold” circuitry is active and not a “resistive” type element, the associated power supply current is negligible. Power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description. Hardware interrupts can be classified as nonmusical or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 2), which are reserved for this purpose. Each element in the table is 4-bytes in size and corresponds to an interrupt “type”. An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

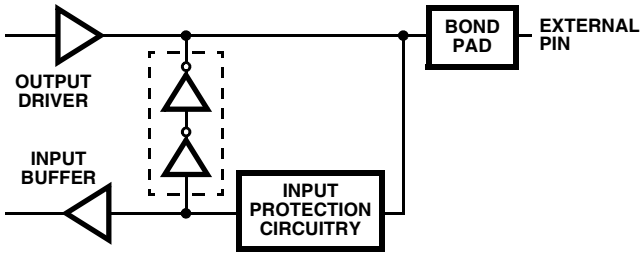


FIGURE 6A. BUS HOLD CIRCUITRY PINS 2-16 AND 35-39

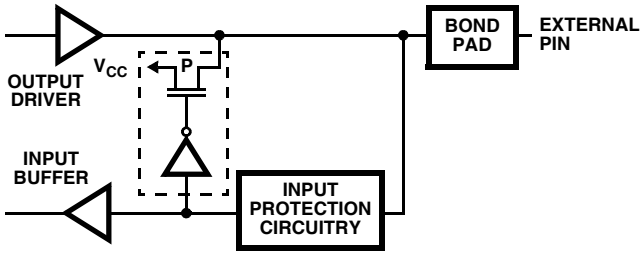


FIGURE 6B. BUS HOLD CIRCUITRY PINS 26-32 AND 34

FIGURE 6.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to High transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. An high going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2-bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure.

The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C88 provides a singe interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK.

To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step). The FLAGS register, which is automatically pushed onto the stack, reflects the state of the processor prior to the interrupt. The enable bit will be zero until the old FLAGS register is restored, unless specifically set by an instruction.

During the response sequence (see Figure 7), the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C88 emits to $\overline{LOCK}$ signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 82C59A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table.

An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

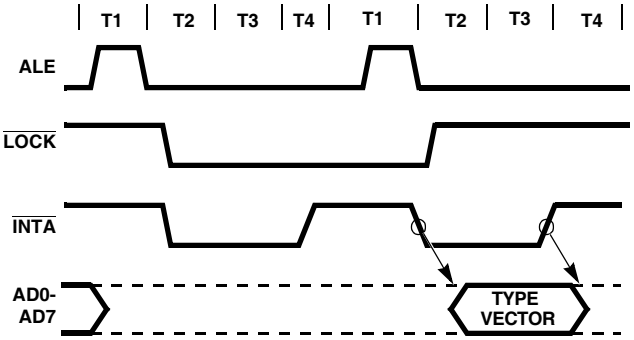


FIGURE 7. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SS0}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$, and the 82C88 bus controller issues one ALE. The 80C88 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 80C88 out of the HALT state.

Read/Modify/Write (Semaphore) Operations Via LOCK

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the $\overline{LOCK}$ prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the $\overline{LOCK}$ prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}$/$\overline{GT}$ pin will be recorded, and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via $\overline{TEST}$

As an alternative to interrupts, the 80C88 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C88 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C88 will recognize interrupts and process them when it regains control of the bus.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals ($\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal (see Figure 5). The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address data bus (ADO-AD7) at this time, into the 82C82/82C83 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address data bus and the bus is held at the last valid logic state by internal bus-hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data

only. DT/$\overline{R}$, IO/$\overline{M}$ and $\overline{SS0}$ provide the complete bus status in minimum mode.

- IO/$\overline{M}$ has been inverted to be compatible with the 8085 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

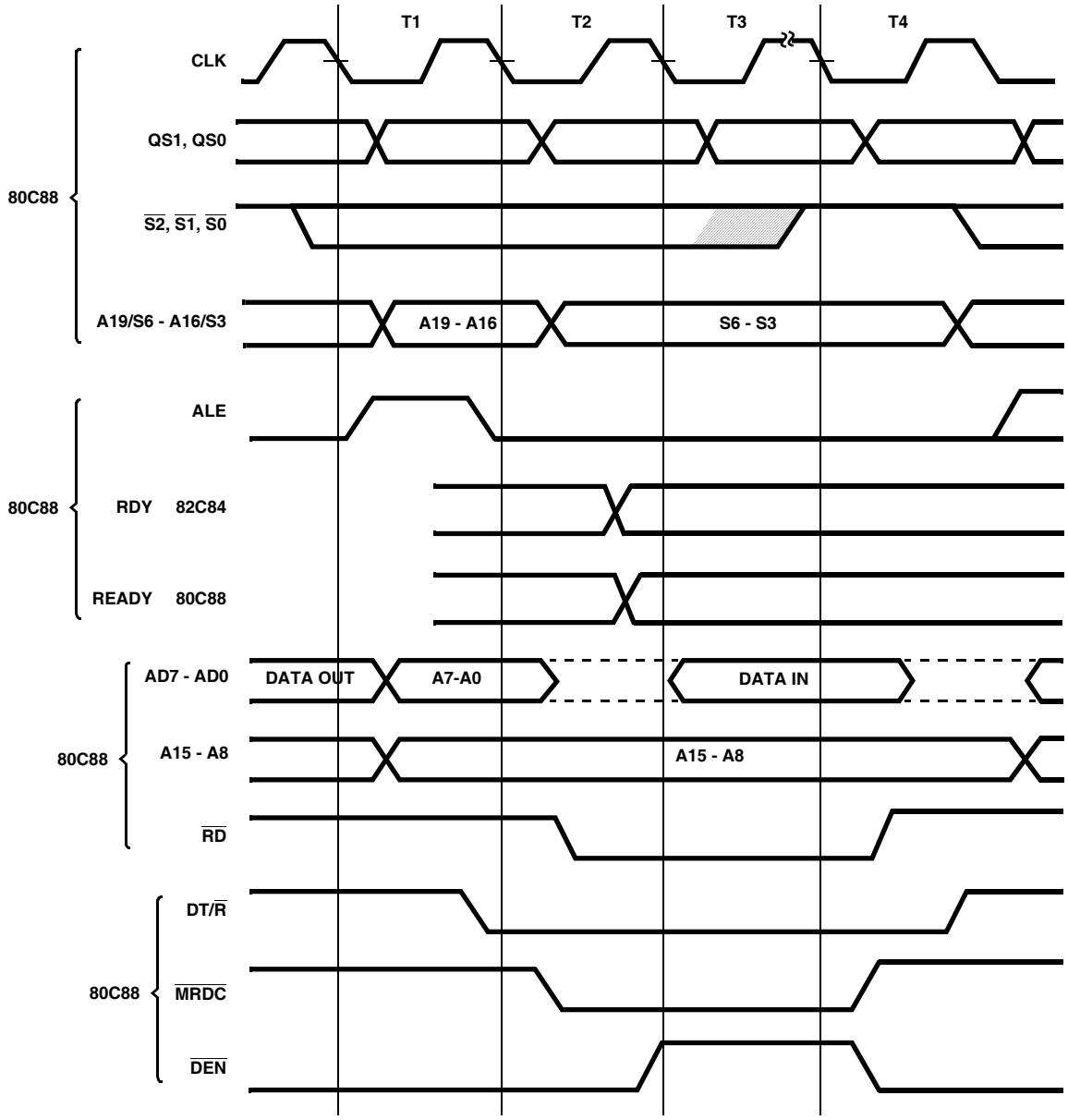


FIGURE 8. MEDIUM COMPLEXITY SYSTEM TIMING

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND - 0.5V to V_{CC} + 0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range. . . . . +4.5V to +5.5V
M80C88-2 Only . . . . . +4.75V to +5.25V
Operating Temperature Range
C80C88/-2 . . . . . 0°C to +70°C
I80C88/-2 . . . . . -40°C to +85°C
M80C88 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical) . . . . . θ_{JA} (°C/W)
PDIP Package* 50
CERDIP Package 30
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package. . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Die Characteristics

Gate Count . . . . . 9750 Gates

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

V_{CC} = 5.0V, ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V, ±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V, ±10%; T_A = -55°C to +125°C (M80C88)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNITS
V_{IH}	Logical One Input Voltage	C80C88, I80C88 (Note 4)	2.0	-	V
		M80C88 (Note 4)	2.2		V
V_{IL}	Logical Zero Input Voltage		-	0.8	V
VIHC	CLK Logical One Input Voltage		V_{CC} - 0.8	-	V
VILC	CLK Logical Zero Input Voltage		-	0.8	V
V_{OH}	Output High Voltage	IOH = -2.5mA	3.0	-	V
		IOH = -100µA	V_{CC} - 0.4		V
V_{OL}	Output Low Voltage	IOL = +2.5mA	-	0.4	V
I_I	Input Leakage Current	V_{IN} = 0V or V_{CC} Pins 17 thru 19, 21 thru 23 and 33	-1.0	1.0	µA
IBHH	Input Current-Bus Hold High	V_{IN} = - 3.0V (Note 1)	-40	-400	µA
IBHL	Input Current-Bus Hold Low	V_{IN} = - 0.8V (Note 2)	40	400	µA
I_O	Output Leakage Current	V_{OUT} = 0V (Note 5)	-	-10.0	µA
ICCSB	Standby Power Supply Current	V_{CC} = 5.5V (Note 3)	-	500	µA
ICCOP	Operating Power Supply Current	FREQ = Max, V_{IN} = V_{CC} or GND, Outputs Open	-	10	mA/MHz

NOTES:

1. IBHH should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins 2 thru16, 26 thru 32, 34 thru 39.
2. IBHL should be measured after lowering V_{IN} to GND and then raising to 0.8V on the following pins: 2 thru16, 35 thru 39.
3. ICCSB tested during clock high time after HALT instruction executed. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs unloaded.
4. MN/$\overline{MX}$ is a strap option and should be held to V_{CC} or GND.
5. IO should be measured by putting the pin in a high impedance state and then driving V_{OUT} to GND on the following pins: 26-29 and 32.

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNITS
C_{IN}	Input Capacitance	FREQ = 1MHz. All measurements are referenced to device GND	25	pF
C_{OUT}	Output Capacitance	FREQ = 1MHz. All measurements are referenced to device GND	25	pF
CI/O	I/O Capacitance	FREQ = 1MHz. All measurements are referenced to device GND	25	pF

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V ±10%; T_A = -55° to +125°C (M80C88) **(Continued)**

SYMBOL		PARAMETER	TEST CONDITIONS	80C88		80C88-2		UNITS
				MIN	MAX	MIN	MAX	
(33)	TCLRL	$\overline{RD}$ Active Delay	CL = 100pF	10	165	10	100	ns
(34)	TCLRH	$\overline{RD}$ Inactive Delay	CL = 100pF	10	150	10	80	ns
(35)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	CL = 100pF	TCLCL-45	-	TCLCL-40	-	ns
(36)	TCLHAV	HLDA Valid Delay	CL = 100pF	10	160	10	100	ns
(37)	TRLRH	$\overline{RD}$ Width	CL = 100pF	2TCLCL-75	-	2TCLCL-50	-	ns
(38)	TWLWH	$\overline{WR}$ Width	CL = 100pF	2TCLCL-60	-	2TCLCL-40	-	ns
(39)	TAVAL	Address Valid to ALE Low	CL = 100pF	TCLCH-60	-	TCLCH-40	-	ns
(40)	TOLOH	Output Rise Time	From 0.8V to 2.0V	-	15	-	15	ns
(41)	TOHOL	Output Fall Time	From 2.0V to 0.8V	-	15	-	15	ns

NOTES:

6. Signal at 82C84A shown for reference only.
7. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
8. Applies only to T2 state (8ns into T3).

Waveforms

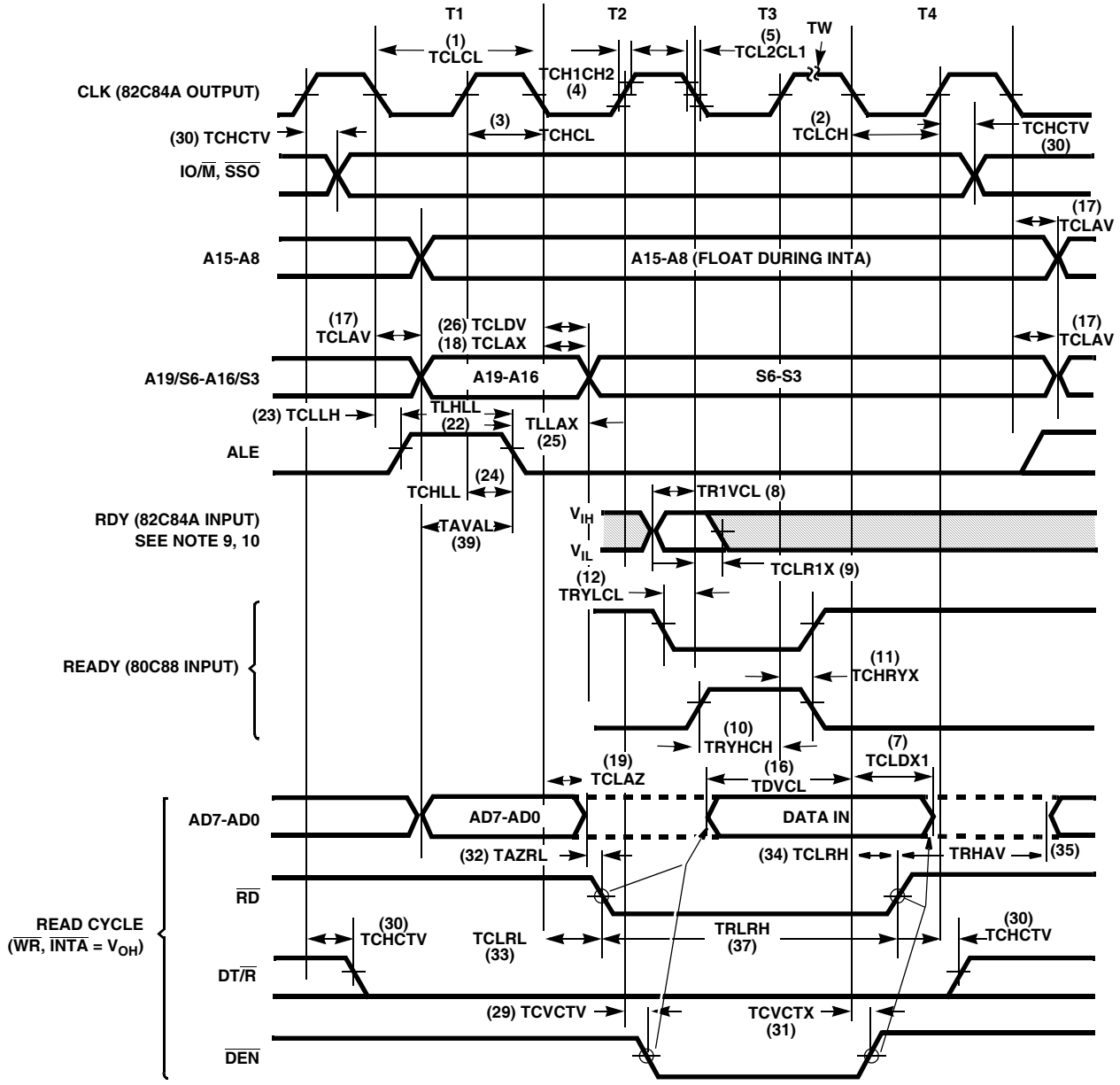


FIGURE 9. BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

9. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.

10. Signals at 82C84A are shown for reference only.

Waveforms (Continued)

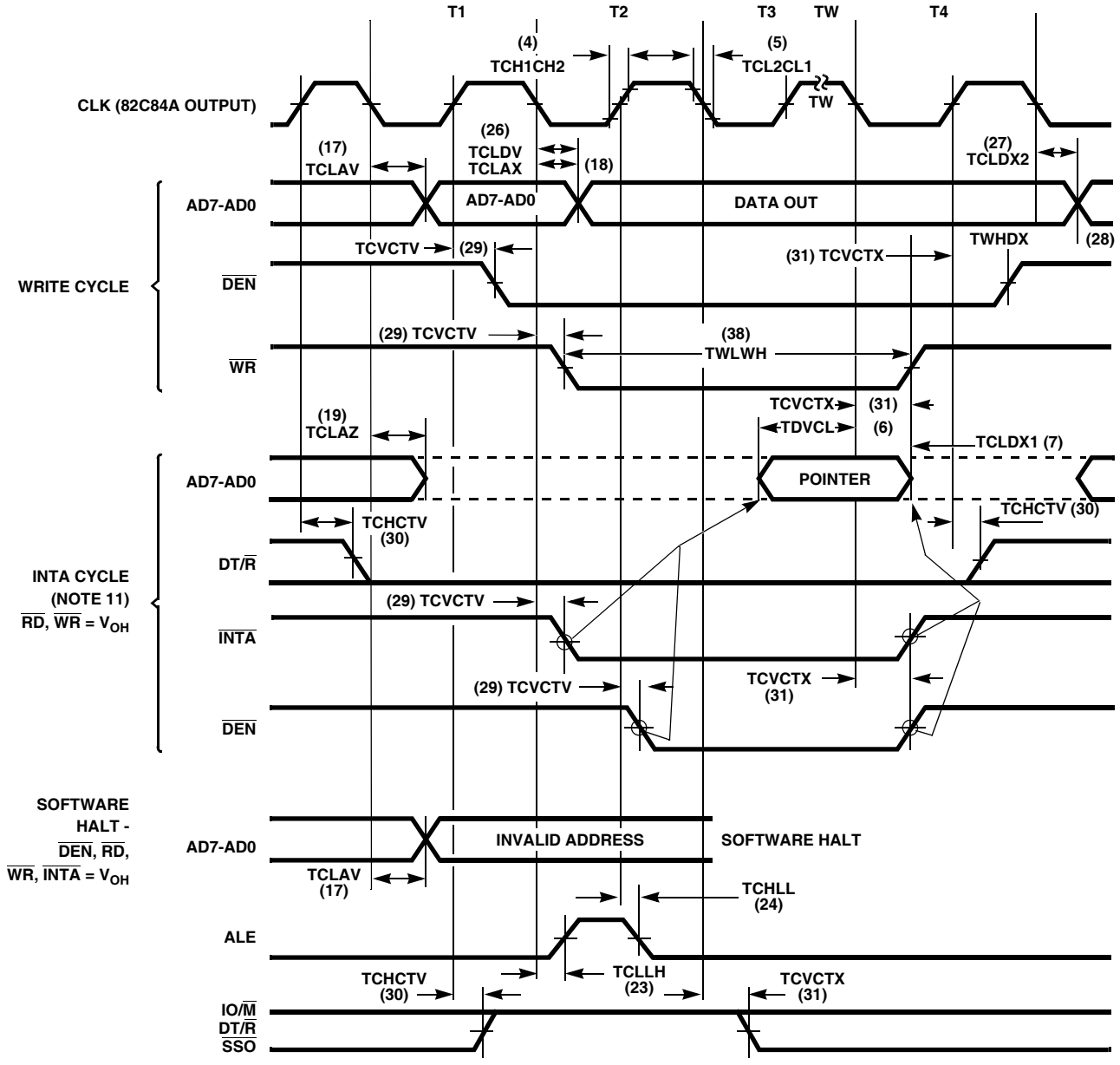


FIGURE 10. BUS TIMING - MINIMUM MODE SYSTEM (Continued)

NOTES:

1. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C88 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
2. Signals at 82C84A are shown for reference only.

AC Electrical Specifications

V_{CC} = 5.0V±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V±10%; T_A = -55°C to +125°C (M80C88)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

SYMBOL		PARAMETER	TEST CONDITIONS	80C88		80C88-2		UNITS
				MIN	MAX	MIN	MAX	
TIMING REQUIREMENTS								
(1)	TCLCL	CLK Cycle Period		200	-	125	-	ns
(2)	TCLCH	CLK Low Time		118	-	68	-	ns
(3)	TCHCL	CLK High Time		69	-	44	-	ns
(4)	TCH1CH2	CLK Rise Time	From 1.0V to 3.5V	-	10	-	10	ns
(5)	TCL2CL1	CLK Fall Time	From 3.5V to 1.0V	-	10	-	10	ns
(6)	TDVCL	Data in Setup Time		30	-	20	-	ns
(7)	TCLDX1	Data In Hold Time		10	-	10	-	ns
(8)	TR1VCL	RDY Setup Time into 82C84 (Notes 13,14)		35	-	35	-	ns
(9)	TCLR1X	RDY Hold Time into 82C84 (Notes 13,14)		0	-	0	-	ns
(10)	TRYHCH	READY Setup Time into 80C88		118	-	68	-	ns
(11)	TCHRYX	READY Hold Time into 80C88		30	-	20	-	ns
(12)	TRYLCL	READY Inactive to CLK (Note15)		-8	-	-8	-	ns
(13)	TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 14)		30	-	15	-	ns
(14)	TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time		30	-	15	-	ns
(15)	TCHGX	$\overline{RQ}$ Hold Time into 80C88 (Note 16)		40	TCHCL + 10	30	TCHCL + 10	ns
(16)	TILIH	Input Rise Time (Except CLK)	From 0.8V to 2.0V	-	15	-	15	ns
(17)	TIHIL	Input Fall Time (Except CLK)	From 2.0V to 0.8V	-	15	-	15	ns
TIMING RESPONSES								
(18)	TCLML	Command Active Delay (Note13)	CL = 100pF for all 80C88 outputs in addition to internal loads.	5	35	5	35	ns
(19)	TCLMH	Command Inactive (Note 13)		5	35	5	35	ns
(20)	TRYHSH	READY Active to Status Passive (Notes 15, 17)		-	110	-	65	ns
(21)	TCHSV	Status Active Delay		10	110	10	60	ns
(22)	TCLSH	Status Inactive Delay (Note 17)		10	130	10	70	ns
(23)	TCLAV	Address Valid Delay		10	110	10	60	ns
(24)	TCLAX	Address Hold Time		10	-	10	-	ns
(25)	TCLAZ	Address Float Delay		TCLAX	80	TCLAX	50	ns
(26)	TCHSZ	Status Float Delay		-	80	-	50	ns
(27)	TSVLH	Status Valid to ALE High (Note 13)		-	20	-	20	ns
(28)	TSVMCH	Status Valid to MCE High (Note 13)		-	30	-	30	ns
(29)	TCLLH	CLK Low to ALE Valid (Note 13)		-	20	-	20	ns
(30)	TCLMCH	CLK Low to MCE High (Note 13)		-	25	-	25	ns
(31)	TCHLL	ALE Inactive Delay (Note 13)		4	18	4	18	ns

AC Electrical Specifications

V_{CC} = 5.0V±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V±10%; T_A = -55°C to +125°C (M80C88)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER) (Continued)

SYMBOL		PARAMETER	TEST CONDITIONS	80C88		80C88-2		UNITS
				MIN	MAX	MIN	MAX	
(32)	TCLMCL	MCE Inactive Delay (Note 13)	CL = 100pF for all 80C88 outputs in addition to internal loads.	-	15	-	15	ns
(33)	TCLDV	Data Valid Delay		10	110	10	60	ns
(34)	TCLDX2	Data Hold Time		10	-	10	-	ns
(35)	TCVNV	Control Active Delay (Note 13)		5	45	5	45	ns
(36)	TCVNX	Control Inactive Delay (Note 13)		10	45	10	45	ns
(37)	TAZRL	Address Float to Read Active		0	-	0	-	ns
(38)	TCLRL	$\overline{RD}$ Active Delay		10	165	10	100	ns
(39)	TCLRH	$\overline{RD}$ Inactive Delay		10	150	10	80	ns
(40)	TRHAV	$\overline{RD}$ Inactive to Next Address Active		TCLCL - 45	-	TCLCL - 40	-	ns
(41)	TCHDTL	Direction Control Active Delay (Note 13)		-	50	-	50	ns
(42)	TCHDTH	Direction Control Inactive Delay (Note 1)		-	30	-	30	ns
(43)	TCLGL	$\overline{GT}$ Active Delay		0	85	0	50	ns
(44)	TCLGH	$\overline{GT}$ Inactive Delay		0	85	0	50	ns
(45)	TRLRH	$\overline{RD}$ Width		2TCLCL - 75	-	2TCLCL - 50	-	ns
(46)	TOLOH	Output Rise Time	From 0.8V to 2.0V	-	15	-	15	ns
(47)	TOHOL	Output Fall Time	From 2.0V to 0.8V	-	15	-	15	ns

NOTES:

3. Signal at 82C84A or 82C88 shown for reference only.
4. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
5. Applies only to T2 state (8ns into T3).
6. The 80C88 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
7. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

Waveforms (Continued)

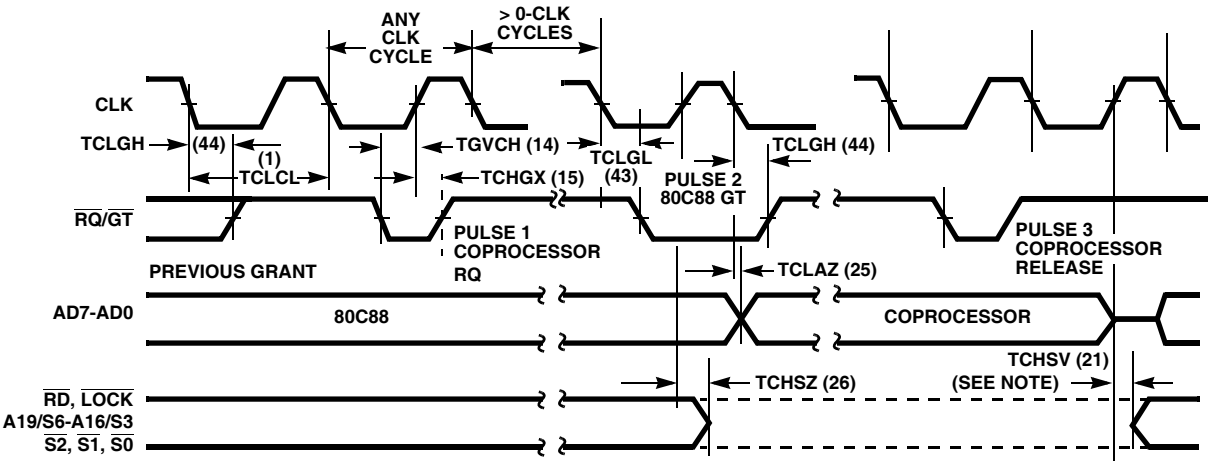


FIGURE 13. REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

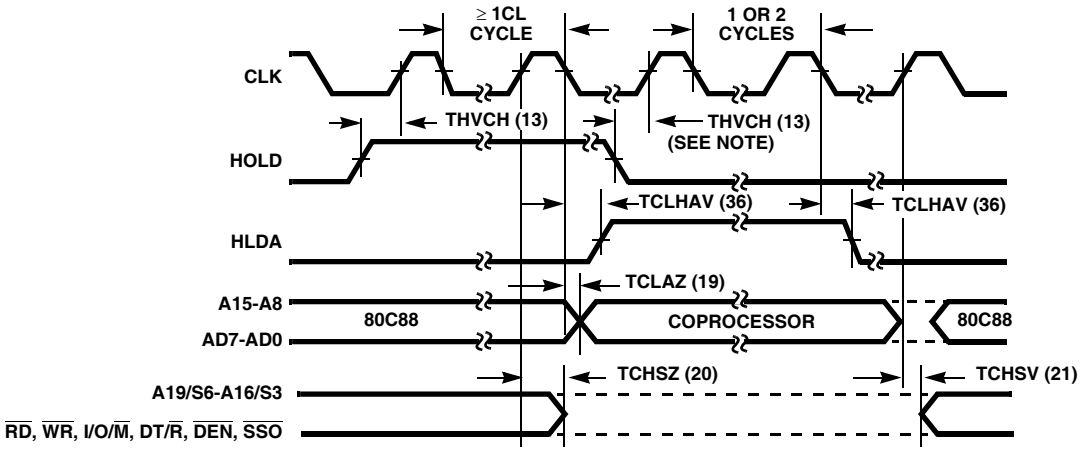


FIGURE 14. HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

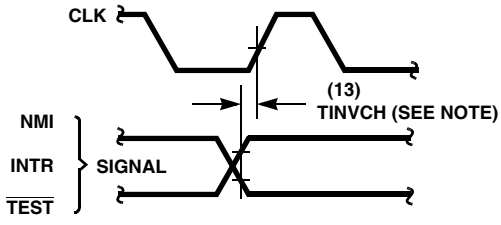


FIGURE 15. ASYNCHRONOUS SIGNAL RECOGNITION

NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

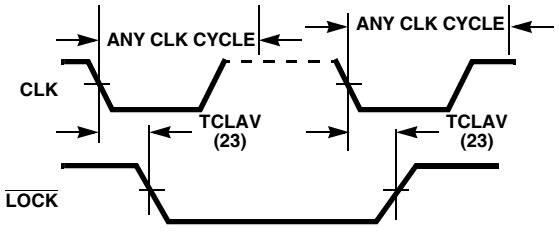


FIGURE 16. BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

Waveforms (Continued)

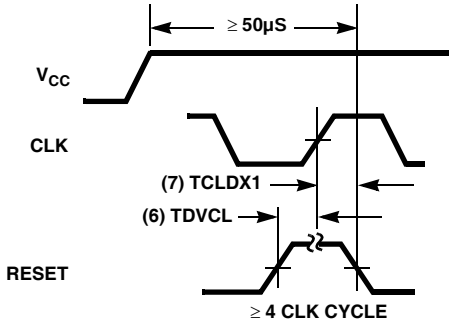
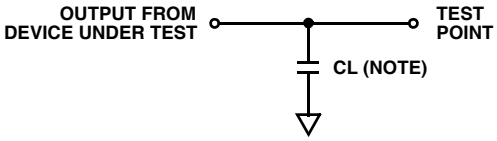


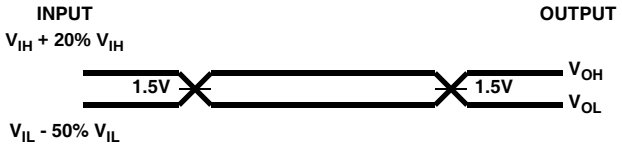
FIGURE 17. RESET TIMING

AC Test Circuit



NOTE: Includes stay and jig capacitance.

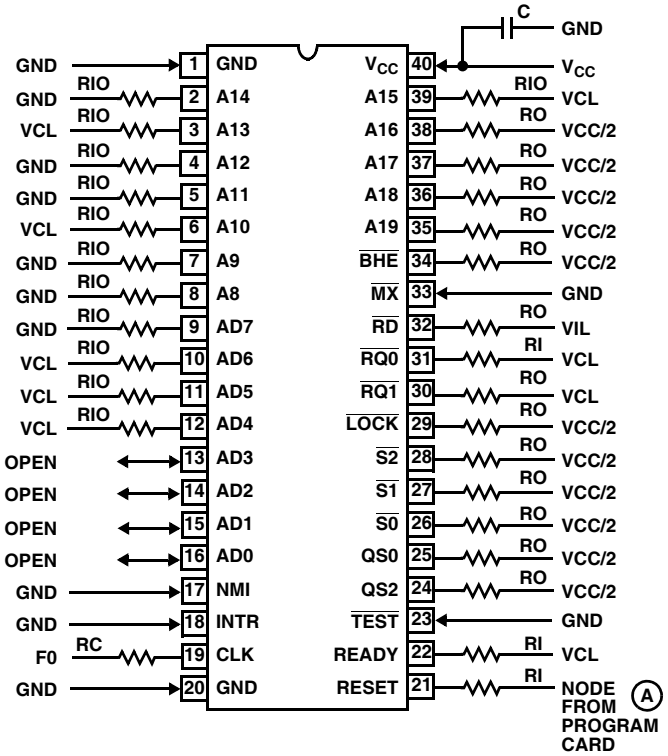
AC Testing Input, Output Waveform



17. All input signals (other than CLK) must switch between V_{ILMAX} -50% V_{IL} and V_{IHMIN} +20% V_{IH}. CLK must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times are driven at 1ns/V.

Burn-In Circuits

MD80C88 (CERDIP)



Instruction Set Summary

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
DATA TRANSFER				
MOV = MOVE:				
Register/Memory to/from Register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to Register	1 0 1 1 w reg	data	data if w 1	
Memory to Accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to Memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/Memory to Segment Register ††	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment Register to Register/Memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment Register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment Register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/Memory with Register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with Accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed Port	1 1 1 0 0 1 0 w	port		
Variable Port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed Port	1 1 1 0 0 1 1 w	port		
Variable Port	1 1 1 0 1 1 1 w			
XLAT = Translate Byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to Register2	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load Pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load Pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with Flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into Flags	1 0 0 1 1 1 1 0			
PUSHF = Push Flags	1 0 0 1 1 1 0 0			
POPF = Pop Flags	1 0 0 1 1 1 0 1			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS= Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then “to” reg; if d = 0 then “from” reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0†, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high:disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP †
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
† except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
†† MOV CS, REG/MEMORY not allowed.
if s:w = 01 then 16-bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then “count” = 1; if v = 1 then “count” in (C_L)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 11 0

REG is assigned according to the following table:

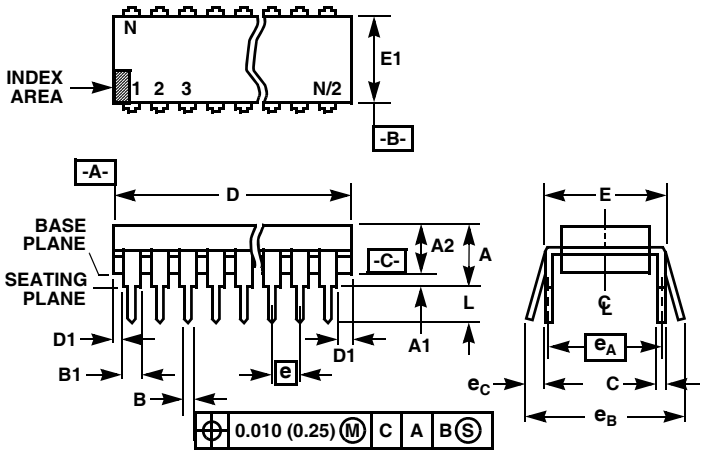
16-BIT (w = 1)	8-BIT (w = 0)	SEGMENT
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS =

X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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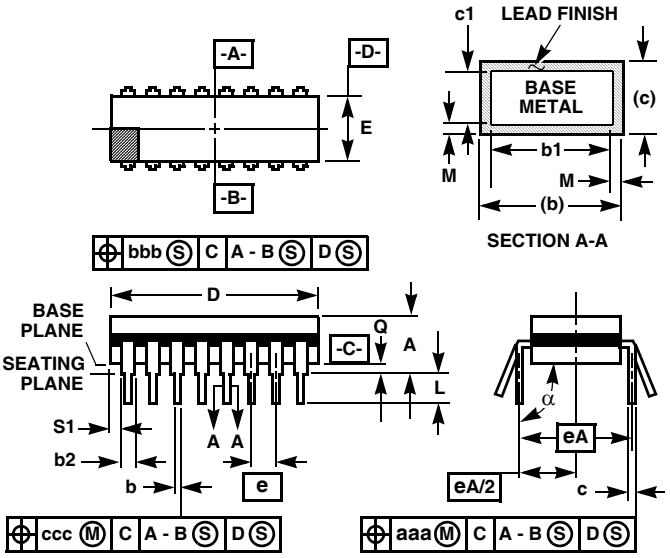
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F40.6 MIL-STD-1835 GDIP1-T40 (D-5, CONFIGURATION A)
40 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	40		40		8

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