**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HCS12 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | EBI/EMI, I²C, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 60 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 2.75V |
| Data Converters | A/D 16x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-QFP |
| Supplier Device Package | 80-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12e128cfue |

## 0x0020 – 0x002F DBG (Including BKP) Map 1 of 1 (HCS12 Debug) (continued)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0026 | DBGCCH | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | — | W | | | | | | | | |
| 0x0027 | DBGCCL | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | — | W | | | | | | | | |
| 0x0028 | DBGC2 | R | BKABEN | FULL | BDM | TAGAB | BKCEN | TAGC | RWCEN | RWC |
| | BKPCT0 | W | | | | | | | | |
| 0x0029 | DBGC3 | R | BKAMBH | BKAMBL | BKBMBH | BKBMBL | RWAEN | RWA | RWBEN | RWB |
| | BKPCT1 | W | | | | | | | | |
| 0x002A | DBGCAX | R | PAGSEL | | EXTCMP | | | | | |
| | BKP0X | W | | | | | | | | |
| 0x002B | DBGCAH | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | BKP0H | W | | | | | | | | |
| 0x002C | DBGCAL | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | BKP0L | W | | | | | | | | |
| 0x002D | DBGCBX | R | PAGSEL | | EXTCMP | | | | | |
| | BKP1X | W | | | | | | | | |
| 0x002E | DBGCBH | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | BKP1H | W | | | | | | | | |
| 0x002F | DBGCBL | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | BKP1L | W | | | | | | | | |

## 0x0030 – 0x0031 MMC Map 4 of 4 (HCS12 Module Mapping Control)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0030 | PPAGE | R | 0 | 0 | PIX5 | PIX4 | PIX3 | PIX2 | PIX1 | PIX0 |
| | | W | | | | | | | | |
| 0x0031 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x0032 – 0x0033 MEBI Map 3 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0032 | PORTK | R | ECS | XCS | XAB19 | XAB18 | XAB17 | XAB16 | XAB15 | XAB14 |
| | | W | | | | | | | | |
| 0x0033 | DDRK | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |

## 0x0040 – 0x006F TIM0 (Timer 16 Bit 4 Channels) (Sheet 3 of 4)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0059 | TC4 (lo) | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |
| 0x005A | TC5 (hi) | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | W | | | | | | | | |
| 0x005B | TC5 (lo) | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |
| 0x005C | TC6 (hi) | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | W | | | | | | | | |
| 0x005D | TC6 (lo) | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |
| 0x005E | TC7 (hi) | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | W | | | | | | | | |
| 0x005F | TC7 (lo) | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |
| 0x0060 | PACTL | R | 0 | PAEN | PAMOD | PEDGE | CLK1 | CLK0 | PAOVI | PAI |
| | | W | | | | | | | | |
| 0x0061 | PAFLG | R | 0 | 0 | 0 | 0 | 0 | 0 | PAOVF | PAIF |
| | | W | | | | | | | | |
| 0x0062 | PACNT (hi) | R | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | W | | | | | | | | |
| 0x0063 | PACNT (lo) | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | W | | | | | | | | |
| 0x0064 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0065 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0066 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0067 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0068 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0069 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x006A | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x006B | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x00B0 – 0x00C7 Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00B0–0x00C7 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x00C8 – 0x00CF SCI0 (Asynchronous Serial Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00C8 | SCIBDH | R | IREN | TNP1 | TNP0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | | W | | | | | | | | |
| 0x00C9 | SCIBDL | R | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | | W | | | | | | | | |
| 0x00CA | SCICR1 | R | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | | W | | | | | | | | |
| 0x00CB | SCICR2 | R | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| | | W | | | | | | | | |
| 0x00CC | SCISR1 | R | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| | | W | | | | | | | | |
| 0x00CD | SCISR2 | R | 0 | 0 | 0 | TXPOL[1] | RXPOL[1] | BRK13 | TXDIR | RAF |
| | | W | | | | | | | | |
| 0x00CE | SCIDRH | R | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x00CF | SCIDRL | R | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | W | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

1 TXPOL and RXPOL bits are available in version V04 of SCI

## 0x00D0 – 0x00D7 SCI1 (Asynchronous Serial Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00D0 | SCIBDH | R | IREN | TNP1 | TNP0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | | W | | | | | | | | |
| 0x00D1 | SCIBDL | R | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | | W | | | | | | | | |
| 0x00D2 | SCICR1 | R | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | | W | | | | | | | | |
| 0x00D3 | SCICR2 | R | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| | | W | | | | | | | | |
| 0x00D4 | SCISR1 | R | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| | | W | | | | | | | | |

## 0x0240 – 0x027F PIM (Port Interface Module) (Sheet 4 of 4)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0270 | PTAD(H) | R | PTAD15 | PTAD14 | PTAD13 | PTAD12 | PTAD11 | PTAD10 | PTAD9 | PTAD8 |
| | | W | | | | | | | | |
| 0x0271 | PTAD(L) | R | PTAD7 | PTAD6 | PTAD5 | PTAD4 | PTAD3 | PTAD2 | PTAD1 | PTAD0 |
| | | W | | | | | | | | |
| 0x0272 | PTIAD(H) | R | PTIAD15 | PTIAD14 | PTIAD13 | PTIAD12 | PTIAD11 | PTIAD10 | PTIAD9 | PTIAD8 |
| | | W | | | | | | | | |
| 0x0273 | PTIAD(L) | R | PTIAD7 | PTIAD6 | PTIAD5 | PTIAD4 | PTIAD3 | PTIAD2 | PTIAD1 | PTIAD0 |
| | | W | | | | | | | | |
| 0x0274 | DDRAD(H) | R | DDRAD15 | DDRAD14 | DDRAD13 | DDRAD12 | DDRAD11 | DDRAD10 | DDRAD9 | DDRAD8 |
| | | W | | | | | | | | |
| 0x0275 | DDRAD(L) | R | DDRAD7 | DDRAD6 | DDRAD5 | DDRAD4 | DDRAD3 | DDRAD2 | DDRAD1 | DDRAD0 |
| | | W | | | | | | | | |
| 0x0276 | RDRAD(H) | R | RDRAD15 | RDRAD14 | RDRAD13 | RDRAD12 | RDRAD11 | RDRAD10 | RDRAD9 | RDRAD8 |
| | | W | | | | | | | | |
| 0x0277 | RDRAD(L) | R | RDRAD7 | RDRAD6 | RDRAD5 | RDRAD4 | RDRAD3 | RDRAD2 | RDRAD1 | RDRAD0 |
| | | W | | | | | | | | |
| 0x0278 | PERAD(H) | R | PERAD15 | PERAD14 | PERAD13 | PERAD12 | PERAD11 | PERAD10 | PERAD9 | PERAD8 |
| | | W | | | | | | | | |
| 0x0279 | PERAD(L) | R | PERAD7 | PERAD6 | PERAD5 | PERAD4 | PERAD3 | PERAD2 | PERAD1 | PERAD0 |
| | | W | | | | | | | | |
| 0x027A | PPSAD(H) | R | PPSAD15 | PPSAD14 | PPSAD13 | PPSAD12 | PPSAD11 | PPSAD10 | PPSAD9 | PPSAD8 |
| | | W | | | | | | | | |
| 0x027B | PPSAD(L) | R | PPSAD7 | PPSAD6 | PPSAD5 | PPSAD4 | PPSAD3 | PPSAD2 | PPSAD1 | PPSAD0 |
| | | W | | | | | | | | |
| 0x027C | PIEAD(H) | R | PIEAD15 | PIEAD14 | PIEAD13 | PIEAD12 | PIEAD11 | PIEAD10 | PIEAD9 | PIEAD8 |
| | | W | | | | | | | | |
| 0x027D | PIEAD(L) | R | PIEAD7 | PIEAD6 | PIEAD5 | PIEAD4 | PIEAD3 | PIEAD2 | PIEAD1 | PIEAD0 |
| | | W | | | | | | | | |
| 0x027E | PIFAD(H) | R | PIFAD15 | PIFAD14 | PIFAD13 | PIFAD12 | PIFAD11 | PIFAD10 | PIFAD9 | PIFAD8 |
| | | W | | | | | | | | |
| 0x027F | PIFAD(L) | R | PIFAD7 | PIFAD6 | PIFAD5 | PIFAD4 | PIFAD3 | PIFAD2 | PIFAD1 | PIFAD0 |
| | | W | | | | | | | | |

## 0x0280 – 0x03FF Reserved Space

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0280–0x2FF | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0300–0x03FF | Unimplemented | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 1.7 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters.

### 1.7.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash block description chapter for more details on the security configuration.

### 1.7.2 Operation of the Secured Microcontroller

#### 1.7.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

#### 1.7.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

### 1.7.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to

#### 1.9.2.2 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module block description chapters for register reset states. Refer to the HCS12 MEBI block description chapter for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM block description chapter for reset configurations of all peripheral module ports.

Refer to Table 1-1 for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

## 3.1.2 Block Diagram

Figure 3-1 is a block diagram of the PIM9E128V1.

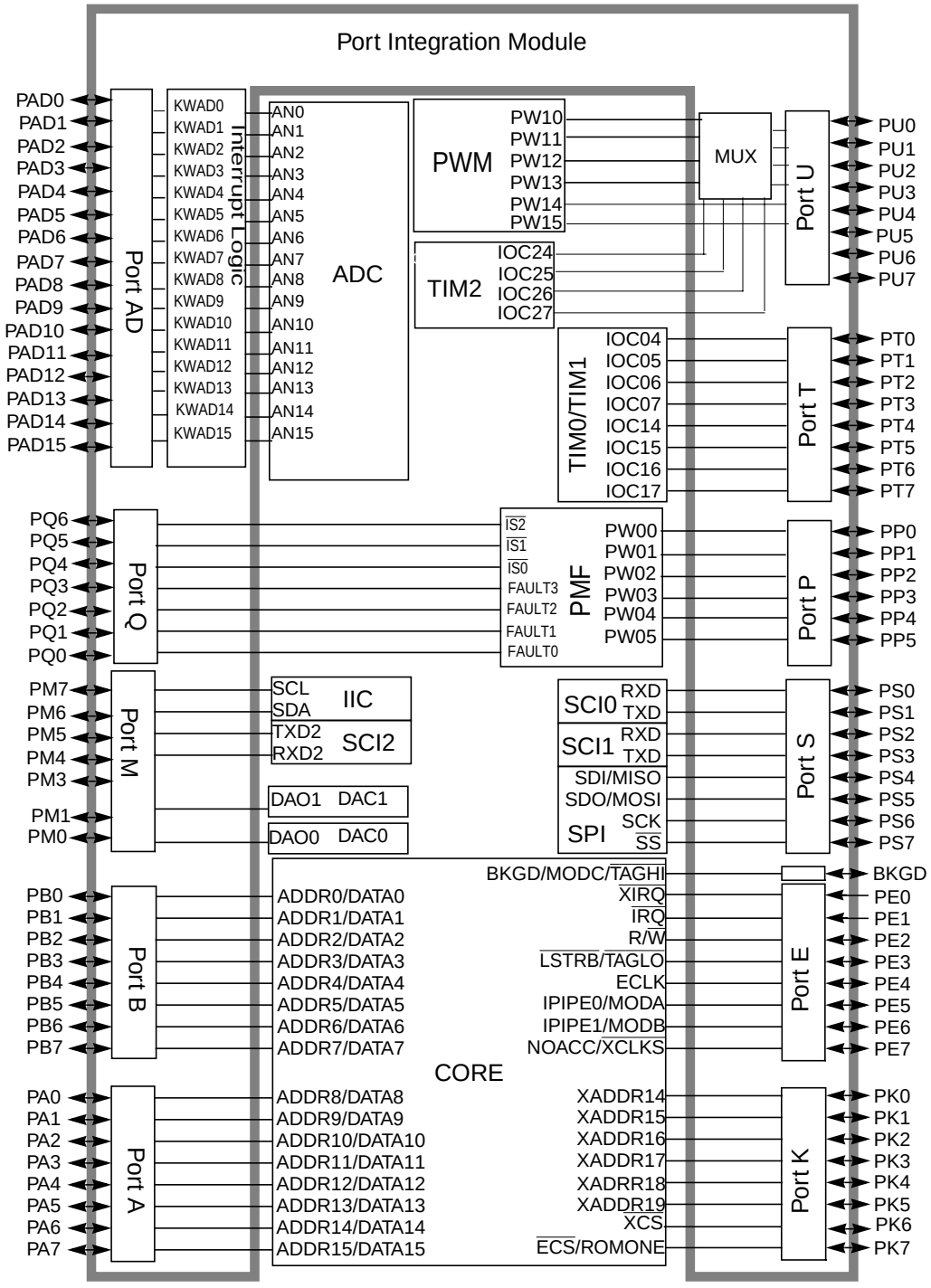


**Figure 3-1. PIM9E128V1 Block Diagram**

### 3.3.7.3 Port U Data Direction Register (DDRU)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | DDRU7 | DDRU6 | DDRU5 | DDRU4 | DDRU3 | DDRU2 | DDRU1 | DDRU0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 3-44. Port U Data Direction Register (DDRU)**

Read: Anytime. Write: Anytime.

This register configures port pins PU[7:0] as either input or output.

If a pulse width modulator channel is enabled, the associated pin is forced to be an output and the associated Data Direction Register bit has no effect. If the associated pulse width modulator channel is disabled, the corresponding DDRUx bit reverts to control the I/O direction of the associated pin.

If the TIM2 module is enabled, each port pin configured for output compare is forced to be an output and the associated Data Direction Register bit has no effect. If the associated timer output compare is disabled, the corresponding DDRUx bit reverts to control the I/O direction of the associated pin.

If the TIM2 module is enabled, each port pin configured as an input capture has the corresponding DDRUx bit controlling the I/O direction of the associated pin.

When both a timer function and a PWM function are enabled on the same pin, the MODRR register determines which function has control of the pin

**Table 3-31. DDRT Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>DDRU[7:0] | **Data Direction Port U**<br>0 Associated pin is configured as input.<br>1 Associated pin is configured as output. |

## 8.2 External Signal Description

The SCI module has a total of two external pins.

### 8.2.1 TXD — SCI Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

### 8.2.2 RXD — SCI Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

## 8.3 Memory Map and Register Definition

This subsection provides a detailed description of all the SCI registers.

### 8.3.1 Module Memory Map

The memory map for the SCI module is given in Figure 8-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

### 8.3.2 Register Descriptions

This subsection consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to reserved register locations do not have any effect and reads of these locations return a 0. Details of register bit and field function follow the register diagrams, in bit order.

| Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| SCIBDH | R | IREN | TNP1 | TNP0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | W | | | | | | | | |
| SCIBDL | R | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | W | | | | | | | | |
| SCICR1 | R | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | W | | | | | | | | |

= Unimplemented or Reserved

**Figure 8-2. SCI Registers Summary**

### 11.3.2.24 PMF Deadtime A Register (PMFDTMA)

Module Base + 0x0026

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PMFDTMA | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

= Unimplemented or Reserved

**Figure 11-30. PMF Deadtime A Register (PMFDTMA)**

Read anytime. This register cannot be modified after the WP bit is set.

**Table 11-31. PMFDTMA Field Descriptions**

| Field | Description |
|---|---|
| 11–0<br>PMFDTMA | **PMF Deadtime A Bits** — The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to a default value of 0x0FFF, selecting a deadtime of 256-PWM clock cycles minus one bus clock cycle.<br>**Note:** Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows: DT = P × PMFDTMA – 1, where DT is deadtime, P is the prescaler value, PMFDTMA is the programmed value of dead time. For example: if the prescaler is programmed for a divide-by-two and the PMFDTMA is set to five, then P = 2 and the deadtime value is equal to DT = 2 × 5 – 1 = 9 IPbus clock cycles. A special case exists when the P = 1, then DT = PMFDTMA. |

### 11.4.8.2 Automatic Fault Clearing

Setting a fault mode bit, FMODEx, configures faults from the FAULTx pin for automatic clearing.

When FMODEx is set, disabled PWM pins are enabled when the FAULTx pin returns to logic zero and a new PWM half cycle begins. See Figure 11-76. Clearing the FFLAGx flag does not affect disabled PWM pins when FMODEx is set.

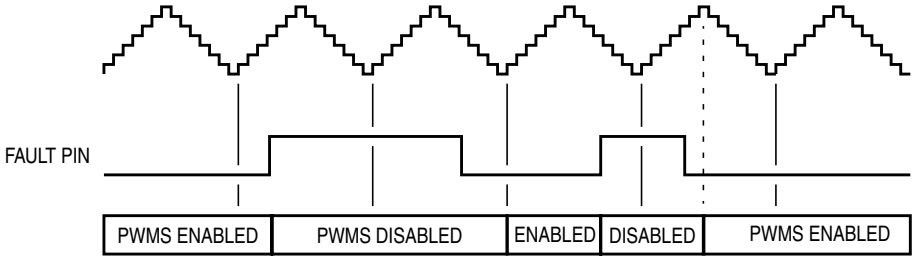


**Figure 11-76. Automatic Fault Clearing**

### 11.4.8.3 Manual Fault Clearing

Clearing a fault mode bit, FMODEx, configures faults from the FAULTx pin for manual clearing:

- PWM pins disabled by the FAULT0 pin or the FAULT2 pin are enabled by clearing the corresponding FFLAGx flag. The time at which the PWM pins are enabled depends on the corresponding QSMPx bit setting. If QSMPx = 00, the PWM pins are enabled on the next IP bus cycle when the logic level detected by the filter at the fault pin is logic zero. If QSMPx = 01,10 or 11, the PWMs are enabled when the next PWM half cycle begins regardless of the state of the logic level detected by the filter at the fault. See Figure 11-77 and Figure 11-78.
- PWM pins disabled by the FAULT1 pin or the FAULT3 pin are enabled when
  - Software clears the corresponding FFLAGx flag
  - The filter detects a logic zero on the fault pin at the start of the next PWM half cycle boundary. See Figure 11-79.

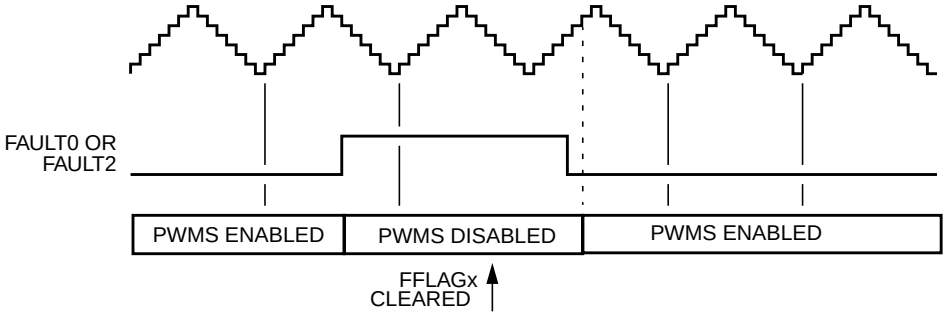


**Figure 11-77. Manual Fault Clearing (Faults 0 & 2) — QSMP = 00**

### 12.1.3 Block Diagram

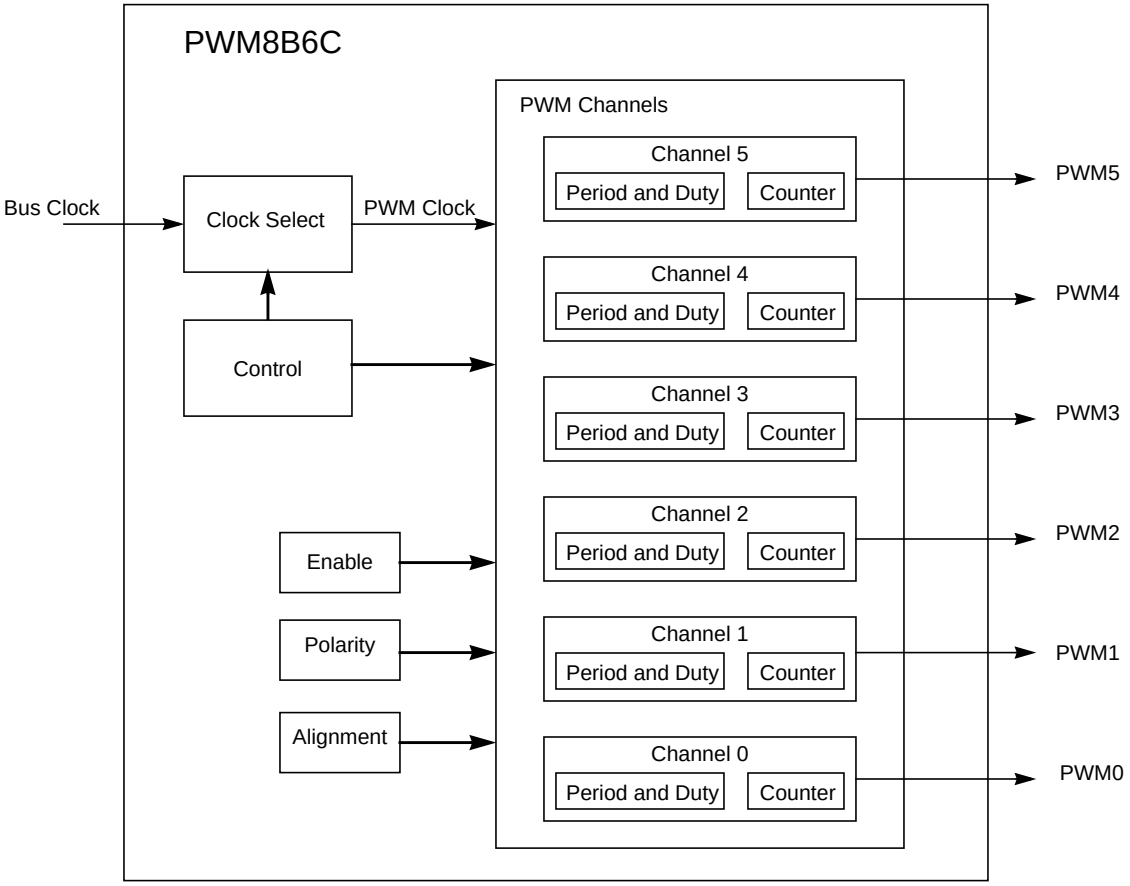


**Figure 12-1. PWM8B6CV1 Block Diagram**

## 12.2 External Signal Description

The PWM8B6CV1 module has a total of six external pins.

### 12.2.1 PWM5 — Pulse Width Modulator Channel 5 Pin

This pin serves as waveform output of PWM channel 5 and as an input for the emergency shutdown feature.

### 12.2.2 PWM4 — Pulse Width Modulator Channel 4 Pin

This pin serves as waveform output of PWM channel 4.

### 12.2.3 PWM3 — Pulse Width Modulator Channel 3 Pin

This pin serves as waveform output of PWM channel 3.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 12-18. PWM Channel Counter Registers (PWMCNT3)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 12-19. PWM Channel Counter Registers (PWMCNT4)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 12-20. PWM Channel Counter Registers (PWMCNT5)**

Read: anytime

Write: anytime (any value written causes PWM counter to be reset to 0x0000).

### 12.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

**NOTE**

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

Reference Section 12.4.2.3, “PWM Period and Duty,” for more information.

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

**NOTE**

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.

### 13.3.2.15 16-Bit Pulse Accumulator Control Register (PACTL)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | PAEN | PAMOD | PEDGE | CLK1 | CLK0 | PAOVI | PAI |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Unimplemented or Reserved

**Figure 13-22. 16-Bit Pulse Accumulator Control Register (PACTL)**

When PAEN is set, the PACT is enabled.The PACT shares the input pin with IOC7.

Read: Any time

Write: Any time

**Table 13-17. PACTL Field Descriptions**

| Field | Description |
|---|---|
| 6<br>PAEN | **Pulse Accumulator System Enable** — PAEN is independent from TEN. With timer disabled, the pulse accumulator can function unless pulse accumulator is disabled.<br>0 16-Bit Pulse Accumulator system disabled.<br>1 Pulse Accumulator system enabled. |
| 5<br>PAMOD | **Pulse Accumulator Mode** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). See Table 13-18.<br>0 Event counter mode.<br>1 Gated time accumulation mode. |
| 4<br>PEDGE | **Pulse Accumulator Edge Control** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). For PAMOD bit = 0 (event counter mode). See Table 13-18.<br>0 Falling edges on IOC7 pin cause the count to be incremented.<br>1 Rising edges on IOC7 pin cause the count to be incremented.<br>For PAMOD bit = 1 (gated time accumulation mode).<br>0 IOC7 input pin high enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing falling edge on IOC7 sets the PAIF flag.<br>1 IOC7 input pin low enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing rising edge on IOC7 sets the PAIF flag. |
| 3:2<br>CLK[1:0] | **Clock Select Bits —** Refer to Table 13-19. |

The minimum pulse width for the PAI input is greater than two bus clocks.

### 13.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

**NOTE**

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

**NOTE**

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

### 13.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

**NOTE**

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

## 13.5 Resets

The reset state of each individual bit is listed within Section 13.3, “Memory Map and Register Definition” which details the registers and their bit fields.

# Chapter 15
# Background Debug Module (BDMV4)

## 15.1 Introduction

This section describes the functionality of the background debug module (BDM) sub-block of the HCS12 core platform.

A block diagram of the BDM is shown in Figure 15-1.

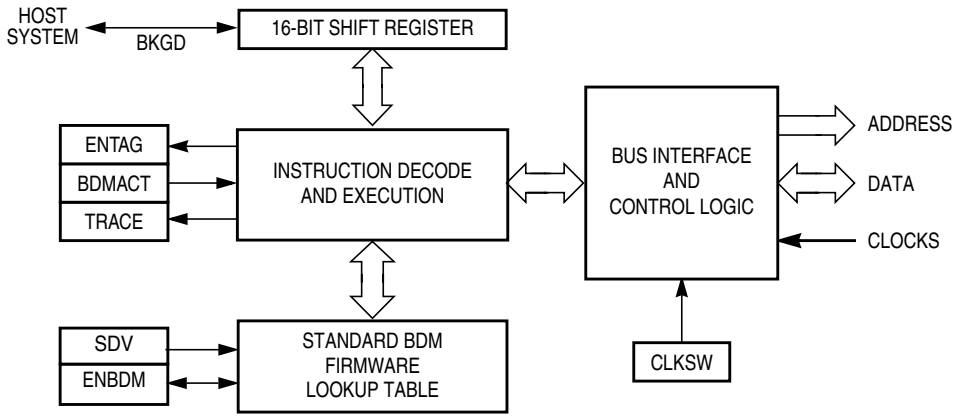


**Figure 15-1. BDM Block Diagram**

The background debug module (BDM) sub-block is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. All interfacing with the BDM is done via the BKGD pin.

BDMV4 has enhanced capability for maintaining synchronization between the target and host while allowing more flexibility in clock rates. This includes a sync signal to show the clock rate and a handshake signal to indicate when an operation is complete. The system is backwards compatible with older external interfaces.

### 15.1.1 Features

- Single-wire communication with host development system
- BDMV4 (and BDM2): Enhanced capability for allowing more flexibility in clock rates
- BDMV4: SYNC command to determine communication rate
- BDMV4: GO_UNTIL command
- BDMV4: Hardware handshake protocol to increase the performance of the serial communication
- Active out of reset in special single-chip mode

## 15.3.2 Register Descriptions

| Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Reserved | R | X | X | X | X | X | X | 0 | 0 |
| | W | | | | | | | | |
| BDMSTS | R | ENBDM | BDMACT | ENTAG | SDV | TRACE | CLKSW | UNSEC | 0 |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |
| BDMCCR | R | CCR7 | CCR6 | CCR5 | CCR4 | CCR3 | CCR2 | CCR1 | CCR0 |
| | W | | | | | | | | |
| BDMINR | R | 0 | REG14 | REG13 | REG12 | REG11 | 0 | 0 | 0 |
| | W | | | | | | | | |
| Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | W | | | | | | | | |
| Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |
| Reserved | R | X | X | X | X | X | X | X | X |
| | W | | | | | | | | |

| | | | |
|---|---|---|---|
| | = Unimplemented, Reserved | | = Implemented (do not alter) |
| X | = Indeterminate | 0 | = Always read zero |

**Figure 15-2. BDM Register Summary**

## 16.3 Memory Map and Register Definition

A summary of the registers associated with the DBG sub-block is shown in Figure 16-3. Detailed descriptions of the registers and bits are given in the subsections that follow.

### 16.3.1 Module Memory Map

**Table 16-2. DBGV1 Memory Map**

| Address Offset | Use | Access |
|---|---|---|
| | Debug Control Register (DBGC1) | R/W |
| | Debug Status and Control Register (DBGSC) | R/W |
| | Debug Trace Buffer Register High (DBGTBH) | R |
| | Debug Trace Buffer Register Low (DBGTBL) | R |
| 4 | Debug Count Register (DBGCNT) | R |
| 5 | Debug Comparator C Extended Register (DBGCCX) | R/W |
| 6 | Debug Comparator C Register High (DBGCCH) | R/W |
| | Debug Comparator C Register Low (DBGCCL) | R/W |
| 8 | Debug Control Register 2 (DBGC2) / (BKPCT0) | R/W |
| 9 | Debug Control Register 3 (DBGC3) / (BKPCT1) | R/W |
| A | Debug Comparator A Extended Register (DBGCAX) / (/BKP0X) | R/W |
| B | Debug Comparator A Register High (DBGCAH) / (BKP0H) | R/W |
| | Debug Comparator A Register Low (DBGCAL) / (BKP0L) | R/W |
| | Debug Comparator B Extended Register (DBGCBX) / (BKP1X) | R/W |
| E | Debug Comparator B Register High (DBGCBH) / (BKP1H) | R/W |
| F | Debug Comparator B Register Low (DBGCBL) / (BKP1L) | R/W |

### 16.3.2 Register Descriptions

This section consists of the DBG register descriptions in address order. Most of the register bits can be written to in either BKP or DBG mode, although they may not have any effect in one of the modes. However, the only bits in the DBG module that can be written while the debugger is armed (ARM = 1) are DBGEN and ARM

| Name[1] | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DBGC1 | R | DBGEN | ARM | TRGSEL | BEGIN | DBGBRK | 0 | CAPMOD | |
| | W | | | | | | | | |
| DBGSC | R | AF | BF | CF | 0 | TRG | | | |
| | W | | | | | | | | |

= Unimplemented or Reserved

**Figure 16-3. DBG Register Summary**

## Table A-27. Expanded Bus Timing Characteristics (3.3V Range)

| Conditions are VDDX=3.3V+/-10%, Junction Temperature -40˚C to +140˚C, $C_{LOAD}$ = 50pF | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | P | Frequency of operation (E-clock) | $f_o$ | 0 | — | 16.0 | MHz |
| 2 | P | Cycle time | $t_{cyc}$ | 62.5 | — | — | ns |
| 3 | D | Pulse width, E low | $PW_{EL}$ | 30 | — | — | ns |
| 4 | D | Pulse width, E high[1] | $PW_{EH}$ | 30 | — | — | ns |
| 5 | D | Address delay time | $t_{AD}$ | — | — | 16 | ns |
| 6 | D | Address valid time to E rise ($PW_{EL}$–$t_{AD}$) | $t_{AV}$ | 16 | — | — | ns |
| 7 | D | Muxed address hold time | $t_{MAH}$ | 2 | — | — | ns |
| 8 | D | Address hold to data valid | $t_{AHDS}$ | 7 | — | — | ns |
| 9 | D | Data hold to address | $t_{DHA}$ | 2 | — | — | ns |
| 10 | D | Read data setup time | $t_{DSR}$ | 15 | — | — | ns |
| 11 | D | Read data hold time | $t_{DHR}$ | 0 | — | — | ns |
| 12 | D | Write data delay time | $t_{DDW}$ | — | — | 15 | ns |
| 13 | D | Write data hold time | $t_{DHW}$ | 2 | — | — | ns |
| 14 | D | Write data setup time[1] ($PW_{EH}$–$t_{DDW}$) | $t_{DSW}$ | 15 | — | — | ns |
| 15 | D | Address access time[1] ($t_{cyc}$–$t_{AD}$–$t_{DSR}$) | $t_{ACCA}$ | 29 | — | — | ns |
| 16 | D | E high access time[1] ($PW_{EH}$–$t_{DSR}$) | $t_{ACCE}$ | 15 | — | — | ns |
| 17 | D | Non-multiplexed address delay time | $t_{NAD}$ | — | — | 14 | ns |
| 18 | D | Non-muxed address valid to E rise ($PW_{EL}$–$t_{NAD}$) | $t_{NAV}$ | 16 | — | — | ns |
| 19 | D | Non-multiplexed address hold time | $t_{NAH}$ | 2 | — | — | ns |
| 20 | D | Chip select delay time | $t_{CSD}$ | — | — | 25 | ns |
| 21 | D | Chip select access time[1] ($t_{cyc}$–$t_{CSD}$–$t_{DSR}$) | $t_{ACCS}$ | 22.5 | — | — | ns |
| 22 | D | Chip select hold time | $t_{CSH}$ | 2 | — | — | ns |
| 23 | D | Chip select negated time | $t_{CSN}$ | 8 | — | — | ns |
| 24 | D | Read/write delay time | $t_{RWD}$ | — | — | 14 | ns |
| 25 | D | Read/write valid time to E rise ($PW_{EL}$–$t_{RWD}$) | $t_{RWV}$ | 16 | — | — | ns |
| 26 | D | Read/write hold time | $t_{RWH}$ | 2 | — | — | ns |
| 27 | D | Low strobe delay time | $t_{LSD}$ | — | — | 14 | ns |
| 28 | D | Low strobe valid time to E rise ($PW_{EL}$–$t_{LSD}$) | $t_{LSV}$ | 16 | — | — | ns |
| 29 | D | Low strobe hold time | $t_{LSH}$ | 2 | — | — | ns |
| 30 | D | NOACC strobe delay time | $t_{NOD}$ | — | — | 14 | ns |
| 31 | D | NOACC valid time to E rise ($PW_{EL}$–$t_{NOD}$) | $t_{NOV}$ | 16 | — | — | ns |
| 32 | D | NOACC hold time | $t_{NOH}$ | 2 | — | — | ns |
| 33 | D | IPIPO[1:0] delay time | $t_{P0D}$ | 2 | — | 14 | ns |
| 34 | D | IPIPO[1:0] valid time to E rise ($PW_{EL}$–$t_{P0D}$) | $t_{P0V}$ | 16 | — | — | ns |
| 35 | D | IPIPO[1:0] delay time[1] ($PW_{EH}$-$t_{P1V}$) | $t_{P1D}$ | 2 | — | 25 | ns |
| 36 | D | IPIPO[1:0] valid time to E fall | $t_{P1V}$ | 11 | — | — | ns |

1 Affected by clock stretch: add N x $t_{cyc}$ where N=0,1,2 or 3, depending on the number of clock stretches.