Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12e128mfue

Appendix A
Electrical Characteristics

Appendix B
Package Information

Appendix C
Ordering Information

1.4.37 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0. While in reset and immediately out of reset the PS0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the SCI block description chapter for information about pin configurations.

1.4.38 PT[7:4] / IOC1[7:4]— Port T I/O Pins [7:4]

PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4]. While in reset and immediately out of reset the PT[7:4] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the TIM_16B4C block description chapter for information about pin configurations.

1.4.39 PT[3:0] / IOC0[7:4]— Port T I/O Pins [3:0]

PT[3:0] are general purpose input or output pins. When the Timer system 0 (TIM0) is enabled they can also be configured as the TIM0 input capture or output compare pins IOC0[7-4]. While in reset and immediately out of reset the PT[3:0] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the TIM_16B4C block description chapter for information about pin configurations.

1.4.40 PU[7:6] — Port U I/O Pins [7:6]

PU[7:6] are general purpose input or output pins. While in reset and immediately out of reset the PU[7:6] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 for information about pin configurations. PU[7:6] are not available in the 80 pin package version.

1.4.41 PU[5:4] / PW1[5:4] — Port U I/O Pins [5:4]

PU[5:4] are general purpose input or output pins. When the Pulse Width Modulator (PWM) is enabled the PU[5:4] output pins, individually or as a pair, can be configured as PW1[5:4] outputs. While in reset and immediately out of reset the PU[5:4] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the PWM_8B6C block description chapter for information about pin configurations. PU[5:4] are not available in the 80 pin package version.

1.4.42 PU[3:0] / IOC2[7:4]/PW1[3:0] — Port U I/O Pins [3:0]

PU[3:0] are general purpose input or output pins. When the Timer system 2 (TIM2) is enabled they can also be configured as the TIM2 input capture or output compare pins IOC2[7-4]. When the Pulse Width Modulator (PWM) is enabled the PU[3:0] output pins, individually or as a pair, can be configured as PW1[3:0] outputs. The MODRR register in the Port Integration Module determines if the TIM2 or PWM function is selected. While in reset and immediately out of reset the PU[3:0] pins are configured as a high

Table 3-1. Detailed Signal Descriptions (Sheet 5 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port S	PS7	$\overline{SS}$	Serial peripheral interface slave select input/output in master mode, input in slave mode	GPIO
		GPIO	General-purpose I/O	
	PS6	SCK	Serial peripheral interface serial clock pin	
		GPIO	General-purpose I/O	
	PS5	MOSI	Serial peripheral interface master out/slave in pin	
		GPIO	General-purpose I/O	
	PS4	MISO	Serial peripheral interface master in/slave out pin	
		GPIO	General-purpose I/O	
	PS3	TXD0	Serial communication interface 1 transmit pin	
		GPIO	General-purpose I/O	
	PS2	RXD0	Serial communication interface 1 receive pin	
		GPIO	General-purpose I/O	
	PS1	TXD0	Serial communication interface 0 transmit pin	
		GPIO	General-purpose I/O	
	PS0	RXD0	Serial communication interface 0 receive pin	
		GPIO	General-purpose I/O	
Port T	PT7	IOC7	Timer 1 channel 7	GPIO
		GPIO	General-purpose I/O	
	PT6	IOC6	Timer 1 channel 6	
		GPIO	General-purpose I/O	
	PT5	IOC5	Timer 1 channel 5	
		GPIO	General-purpose I/O	
	PT4	IOC4	Timer 1 channel 4	
		GPIO	General-purpose I/O	
	PT3	IOC3	Timer 0 channel 7	
		GPIO	General-purpose I/O	
	PT2	IOC2	Timer 0 channel 6	
		GPIO	General-purpose I/O	
	PT1	IOC1	Timer 0 channel 5	
		GPIO	General-purpose I/O	
	PT0	IOC0	Timer 0 channel 4	
		GPIO	General-purpose I/O	

3.3.3.5 Port P Pull Device Enable Register (PERP)

	7	6	5	4	3	2	1	0
R	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 3-21. Port P Pull Device Enable Register (PERP)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 3-16. PERP Field Descriptions

Field	Description
5:0 PERP[5:0]	**Pull Device Enable Port P** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

3.3.3.6 Port P Polarity Select Register (PPSP)

	7	6	5	4	3	2	1	0
R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 3-22. Port P Polarity Select Register (PPSP)

Read: Anytime. Write: Anytime.

The Port P Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port P Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 3-17. PPSP Field Descriptions

Field	Description
5:0 PPSP[5:0]	**Polarity Select Port P** 0 A pull-up device is connected to the associated port P pin. 1 A pull-down device is connected to the associated port P pin.

4.4.6 Real-Time Interrupt (RTI)

The RTI can be used to generate a hardware interrupt at a fixed periodic rate. If enabled (by setting RTIE=1), this interrupt will occur at the rate selected by the RTICTL register. The RTI runs with a gated OSCCLK (see Section Figure 4-22., “Clock Chain for RTI”). At the end of the RTI time-out period the RTIF flag is set to 1 and a new RTI time-out period starts immediately.

A write to the RTICTL register restarts the RTI time-out period.

If the PRE bit is set, the RTI will continue to run in pseudo-stop mode.

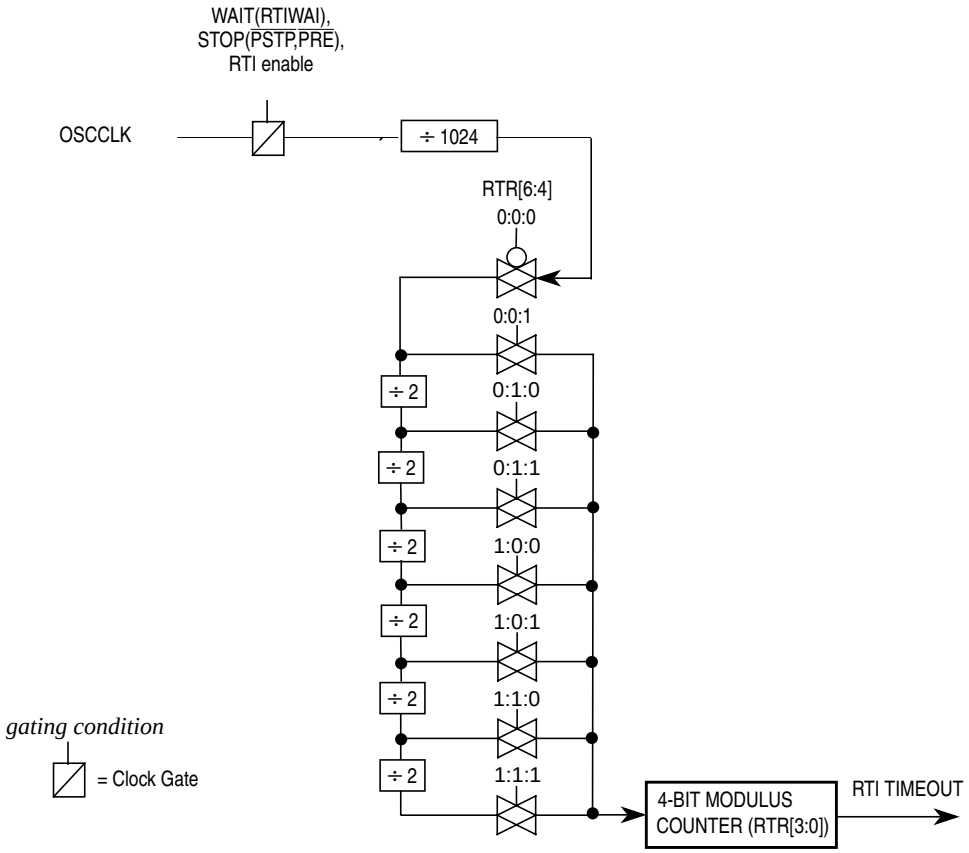


Figure 4-22. Clock Chain for RTI

4.4.7 Modes of Operation

4.4.7.1 Normal Mode

The CRGV4 block behaves as described within this specification in all normal modes.

4.4.7.2 Self-Clock Mode

The VCO has a minimum operating frequency, f_{SCM}. If the external clock frequency is not available due to a failure or due to long crystal start-up time, the bus clock and the core clock are derived from the VCO

Table 6-6. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

10.2 External Signal Description

The IICV2 module has two external pins.

10.2.1 IIC_SCL — Serial Clock Line Pin

This is the bidirectional serial clock line (SCL) of the module, compatible to the IIC bus specification.

10.2.2 IIC_SDA — Serial Data Line Pin

This is the bidirectional serial data line (SDA) of the module, compatible to the IIC bus specification.

10.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the IIC module.

10.3.1 Module Memory Map

The memory map for the IIC module is given below in Table 10-1. The address listed for each register is the address offset.The total address for each register is the sum of the base address for the IIC module and the address offset for each register.

10.3.2.2 IIC Frequency Divider Register (IBFD)

	7	6	5	4	3	2	1	0
R W	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-3. IIC Bus Frequency Divider Register (IBFD)

Read and write anytime

Table 10-3. IBFD Field Descriptions

Field	Description
7:0 IBC[7:0]	**I Bus Clock Rate 7:0** — This field is used to prescale the clock for bit rate selection. The bit clock generator is implemented as a prescale divider — IBC7:6, prescaled shift register — IBC5:3 select the prescaler divider and IBC2-0 select the shift register tap point. The IBC bits are decoded to give the tap and prescale values as shown in Table 10-4.

Table 10-4. I-Bus Tap and Prescale Values

IBC2-0 (bin)	SCL Tap (clocks)	SDA Tap (clocks)
000	5	1
001	6	1
010	7	2
011	8	2
100	9	3
101	10	3
110	12	4
111	15	4

IBC5-3 (bin)	scl2start (clocks)	scl2stop (clocks)	scl2tap (clocks)	tap2tap (clocks)
000	2	7	4	1
001	2	7	4	2
010	2	9	6	4
011	6	9	6	8
100	14	17	14	16
101	30	33	30	32
110	62	65	62	64
111	126	129	126	128

11.4.5.1 Top/Bottom Correction

In complementary mode, either the top or the bottom transistor controls the output voltage. However, deadtime has to be inserted to avoid overlap of conducting interval between the top and bottom transistor. Both transistors in complementary mode are off during deadtime, allowing the output voltage to be determined by the current status of load and introduce distortion in the output voltage. See Figure 11-53. On AC induction motors running open-loop, the distortion typically manifests itself as poor low-speed performance, such as torque ripple and rough operation.

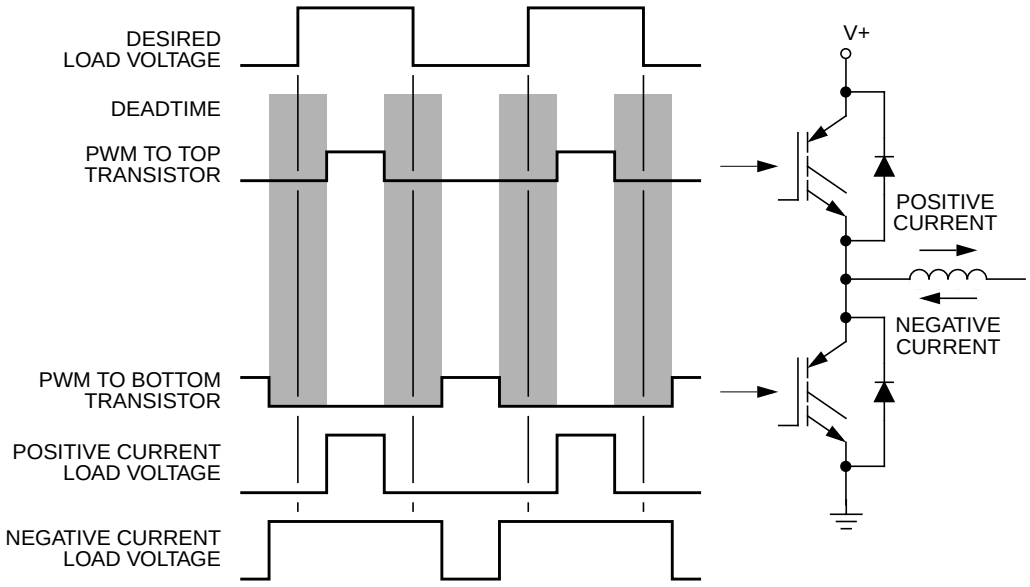


Figure 11-53. Deadtime Distortion

During deadtime, load inductance distorts output voltage by keeping current flowing through the diodes. This deadtime current flow creates a load voltage that varies with current direction. With a positive current flow, the load voltage during deadtime is equal to the bottom supply, putting the top transistor in control. With a negative current flow, the load voltage during deadtime is equal to the top supply putting the bottom transistor in control.

Remembering that the original PWM pulse widths were shortened by deadtime insertion, the averaged sinusoidal output will be less than desired value. However, when deadtime is inserted, it creates a distortion in motor current waveform. This distortion is aggravated by dissimilar turn-on and turn-off delays of each of the transistors. By giving the PWM module information on which transistor is controlling at a given time this distortion can be corrected.

For a typical circuit in complementary channel operation, only one of the transistors will be effective in controlling the output voltage at any given time. This depends on the direction of the motor current for that pair. See Figure 11-53. To correct distortion one of two different factors must be added to the desired PWM value, depending on whether the top or bottom transistor is controlling the output voltage. Therefore, the software is responsible for calculating both compensated PWM values prior to placing them in an odd-numbered/even numbered PWM register pair. Either the odd or the even PMFVAL register controls the pulse width at any given time.

- BKGD — Background interface pin
- $\overline{\text{TAGHI}}$ — High byte instruction tagging pin
- $\overline{\text{TAGLO}}$ — Low byte instruction tagging pin
- BKGD and $\overline{\text{TAGHI}}$ share the same pin.
- $\overline{\text{TAGLO}}$ and $\overline{\text{LSTRB}}$ share the same pin.

NOTE

Generally these pins are shared as described, but it is best to check the device overview chapter to make certain. All MCUs at the time of this writing have followed this pin sharing scheme.

15.2.1 BKGD — Background Interface Pin

Debugging control logic communicates with external devices serially via the single-wire background interface pin (BKGD). During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the background debug mode.

15.2.2 $\overline{\text{TAGHI}}$ — High Byte Instruction Tagging Pin

This pin is used to tag the high byte of an instruction. When instruction tagging is on, a logic 0 at the falling edge of the external clock (ECLK) tags the high half of the instruction word being read into the instruction queue.

15.2.3 $\overline{\text{TAGLO}}$ — Low Byte Instruction Tagging Pin

This pin is used to tag the low byte of an instruction. When instruction tagging is on and low strobe is enabled, a logic 0 at the falling edge of the external clock (ECLK) tags the low half of the instruction word being read into the instruction queue.

16.3.2.5 Debug Comparator C Extended Register (DBGCCX)

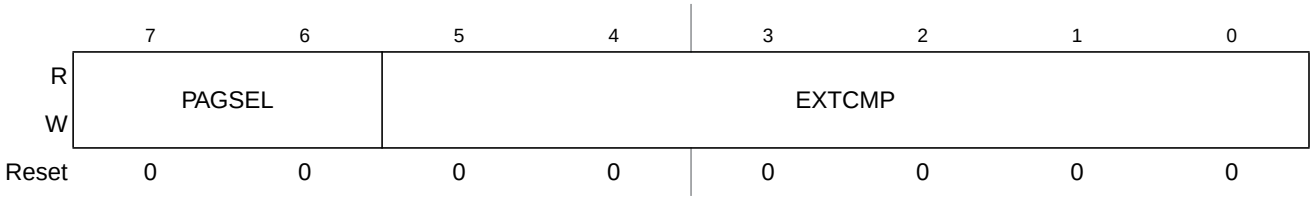


Figure 16-9. Debug Comparator C Extended Register (DBGCCX)

Table 16-10. DBGCCX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — In both BKP and DBG mode, PAGSEL selects the type of paging as shown in Table 16-11. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively).
5:0 EXTCMP	**Comparator C Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 16-11 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core. **Note:** Comparator C can be used when the DBG module is configured for BKP mode. Extended addressing comparisons for comparator C use PAGSEL and will operate differently to the way that comparator A and B operate in BKP mode.

Table 16-11. PAGSEL Decoding[1]

PAGSEL	Description	EXTCMP	Comment
00	Normal (64k)	Not used	No paged memory
01	PPAGE (256 — 16K pages)	EXTCMP[5:0] is compared to address bits [21:16][2]	PPAGE[7:0] / XAB[21:14] becomes address bits [21:14][1]
10[3]	DPAGE (reserved) (256 — 4K pages)	EXTCMP[3:0] is compared to address bits [19:16]	DPAGE / XAB[21:14] becomes address bits [19:12]
11[2]	EPAGE (reserved) (256 — 1K pages)	EXTCMP[1:0] is compared to address bits [17:16]	EPAGE / XAB[21:14] becomes address bits [17:10]

1 See Figure 16-10.

2 Current HCS12 implementations have PPAGE limited to 6 bits. Therefore, EXTCMP[5:4] should be set to 00.

3 Data page (DPAGE) and Extra page (EPAGE) are reserved for implementation on devices that support paged data and extra space.

18.3.2.4 Data Direction Register B (DDRB)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 18-5. Data Direction Register B (DDRB)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

This register controls the data direction for port B. When port B is operating as a general-purpose I/O port, DDRB determines the primary direction for each port B pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTB register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. It is reset to 0x00 so the DDR does not override the three-state control signals.

Table 18-4. DDRB Field Descriptions

Field	Description
7:0 DDRB	**Data Direction Port B** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output

18.4.3 Modes of Operation

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (Table 18-16). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 18-16. Mode Selection

MODC	MODB	MODA	Mode Description
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	Emulation Expanded Narrow, BDM allowed
0	1	0	Special Test (Expanded Wide), BDM allowed
0	1	1	Emulation Expanded Wide, BDM allowed
1	0	0	Normal Single Chip, BDM allowed
1	0	1	Normal Expanded Narrow, BDM allowed
1	1	0	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	Normal Expanded Wide, BDM allowed

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of Port E are not mode dependent. Bit 1 of Port E is a general purpose input or the $\overline{\text{IRQ}}$ interrupt input. $\overline{\text{IRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of Port E is a general purpose input or the $\overline{\text{XIRQ}}$ interrupt input. $\overline{\text{XIRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

18.4.3.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

18.4.3.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

18.4.3.3.1 Peripheral Mode

This mode is intended for factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

18.4.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or emulation narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E, R/$\overline{W}$, and $\overline{LSTRB}$ are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{W}$ will remain high, data will maintain its previous state, and address and $\overline{LSTRB}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

In Table A-18 the timing characteristics for slave mode are listed.

Table A-18. SPI Slave Mode Timing Characteristics

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	P	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	P	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	D	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	D	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	D	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	D	Slave Access Time (time to data active)	t_{a}	—	—	20	ns
8	D	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	30 + t_{bus}[1]	ns
10	D	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	30 + t_{bus}[1]	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1 t_{bus} added due to internal synchronization delay

A.6 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

A.6.1 ATD Operating Characteristics — 5V Range

The Table A-19 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-19. 5V ATD Operating Characteristics

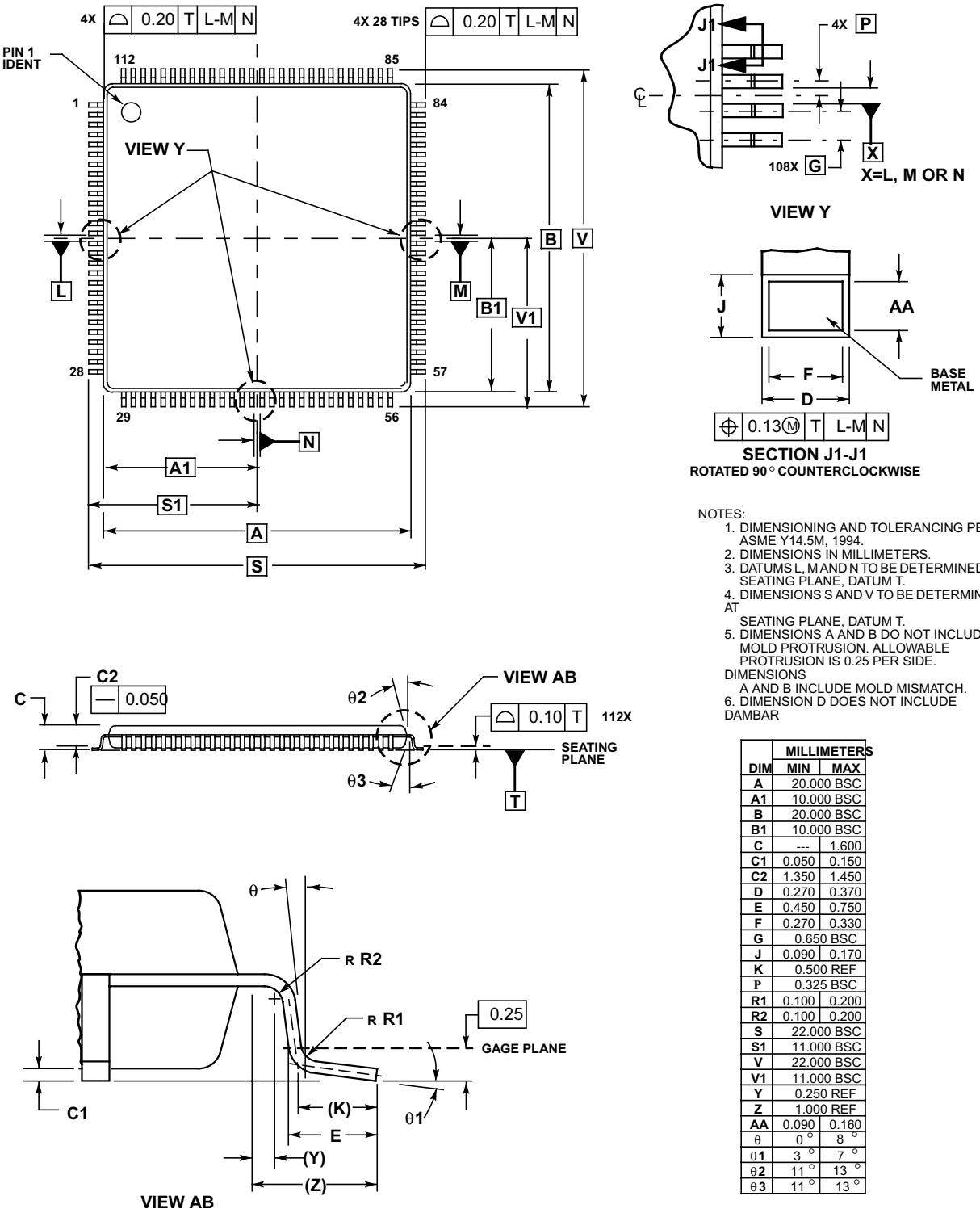
Conditions are shown in Table A-4 unless otherwise noted. Supply Voltage 5V-10% <= VDDA <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA/2}$	 — —	 $V_{DDA/2}$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}–V_{RL}	4.75	5.0	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[3] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5	 — — —	 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6	 — —	 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA} = 5.0 Volts)	t_{SR}	—	—	20	µs
7	P	Reference Supply current	I_{REF}	—	—	0.375	mA

1 Full accuracy is not guaranteed when differential voltage is less than 4.75V

2 The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

3 Reduced accuracy see Table A-22 and Table A-23.

B.3 112-Pin LQFP Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure B-3. 112-Pin QFP Mechanical Dimensions (Case no. 987)