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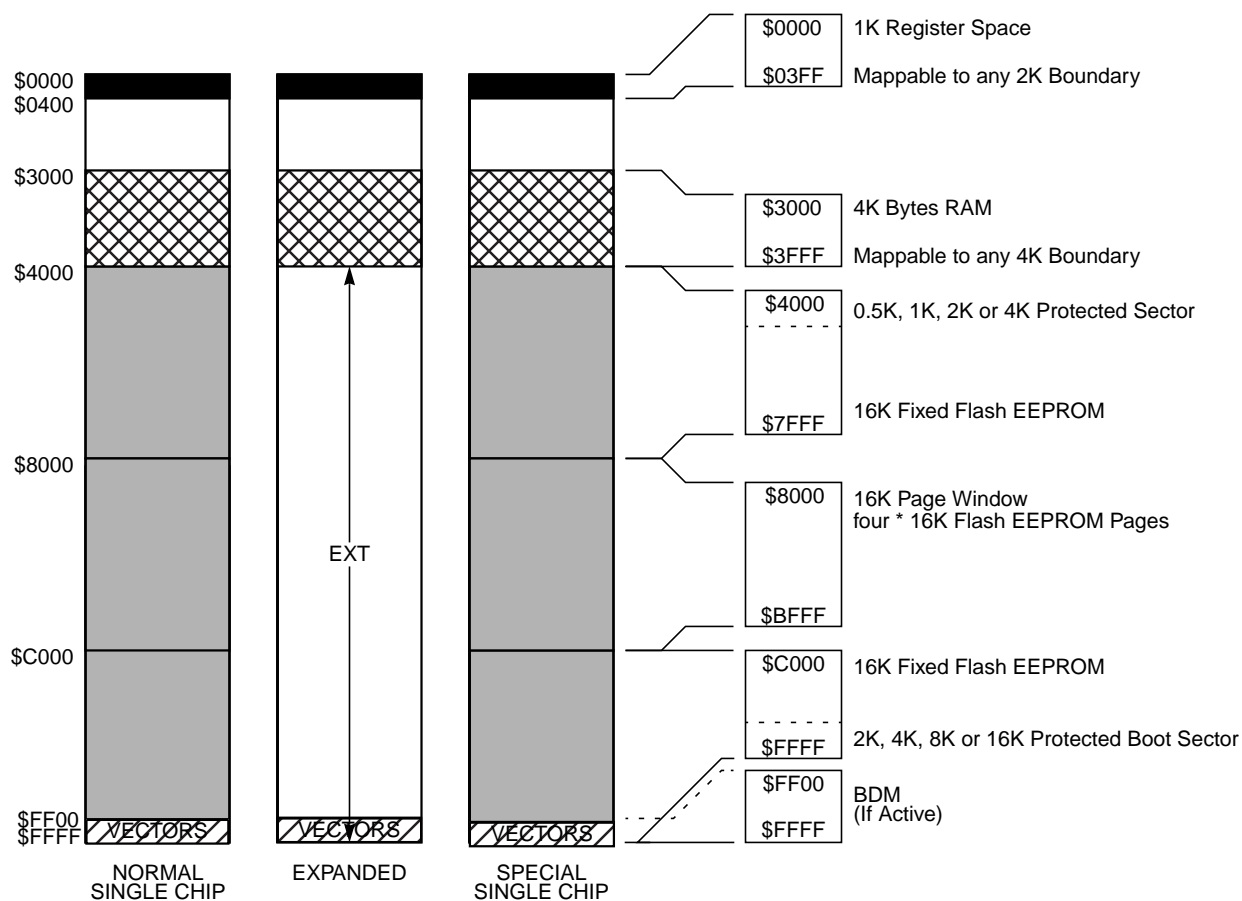
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Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I ² C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12e64cfu



The figure shows a useful map, which is not the map out of reset. After reset the map is:

\$0000-\$03FF: Register Space
 \$0000-\$0FFF: 4K RAM (only 3K RAM visible \$0400-\$0FFF)

Figure 1-3. MC9S12E64 User Configurable Memory Map

3.3.1.3 Port AD Data Direction Register (DDRAD)

	7	6	5	4	3	2	1	0
R	DDRAD15	DDRAD14	DDRAD13	DDRAD12	DDRAD11	DDRAD10	DDRAD9	DDRAD8
W								
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 3-4. Port AD Data Direction Register (DDRAD)

Read: Anytime. Write: Anytime.

This register configures port pins PAD[15:0] as either input or output.

If a data direction bit is 0 (pin configured as input), then a read value on PTADx depends on the associated ATDDIEN0(1) bit. If the associated ATDDIEN0(1) bit is set to 1 (digital input buffer is enabled), a read on PTADx returns the value on port AD pin. If the associated ATDDIEN0(1) bit is set to 0 (digital input buffer is disabled), a read on PTADx returns a 1.

Table 3-3. DDRAD Field Descriptions

Field	Description
15:0 DDRAD[15:0]	Data Direction Port AD 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.2.10 Reserved Register (FORBYP)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-13. Reserved Register (FORBYP)

Read: always read 0x0000 except in special modes

Write: only in special modes

4.3.2.11 Reserved Register (CTCTL)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-14. Reserved Register (CTCTL)

Read: always read 0x0080 except in special modes

Write: only in special modes

writes (0x0055 or 0x00AA) to the ARMCOP register must occur in the last 25% of the selected time-out period. A premature write the CRG will immediately generate a reset.

As soon as the reset sequence is completed the reset generator checks the reset condition. If no clock monitor failure is indicated and the latched state of the COP timeout is true, processing begins by fetching the COP vector.

4.5.3 Power-On Reset, Low Voltage Reset

The on-chip voltage regulator detects when V_{DD} to the MCU has reached a certain level and asserts power-on reset or low voltage reset or both. As soon as a power-on reset or low voltage reset is triggered the CRG performs a quality check on the incoming clock signal. As soon as clock quality check indicates a valid oscillator clock signal the reset sequence starts using the oscillator clock. If after 50 check windows the clock quality check indicated a non-valid oscillator clock the reset sequence starts using self-clock mode.

Figure 4-26 and Figure 4-27 show the power-up sequence for cases when the $\overline{\text{RESET}}$ pin is tied to V_{DD} and when the $\overline{\text{RESET}}$ pin is held low.

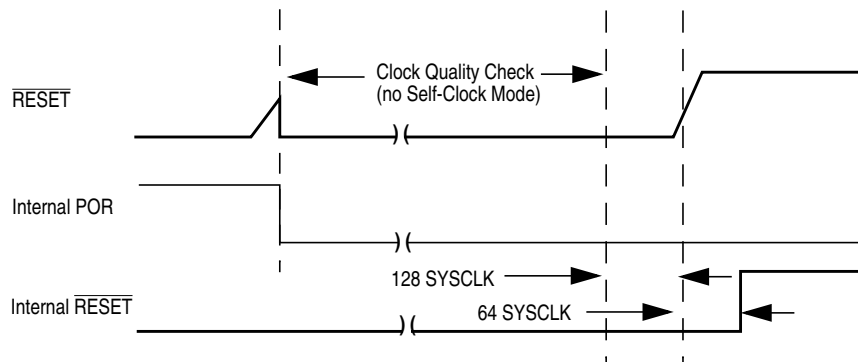


Figure 4-26. $\overline{\text{RESET}}$ Pin Tied to V_{DD} (by a Pull-Up Resistor)

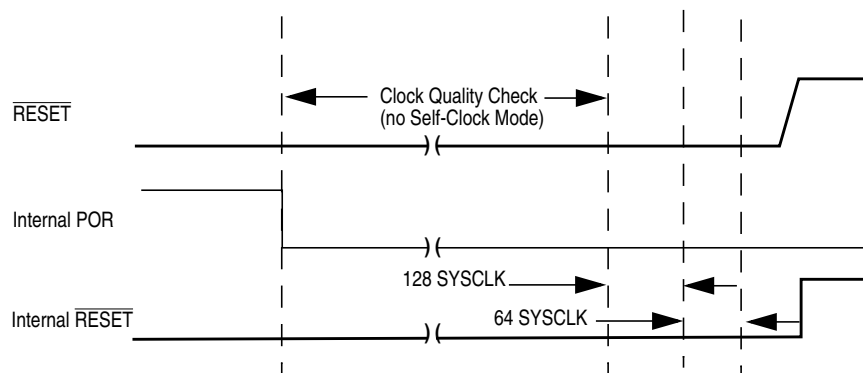


Figure 4-27. $\overline{\text{RESET}}$ Pin Held Low Externally

chip dependent. The SCI only has a single interrupt line (SCI interrupt signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

8.5.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission. Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

8.5.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL). TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

8.5.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

8.5.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

8.5.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. After the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

8.5.2 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

Chapter 9

Serial Peripheral Interface (SPIV3)

9.1 Introduction

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or the SPI operation can be interrupt driven.

9.1.1 Features

The SPIV3 includes these distinctive features:

- Master mode and slave mode
- Bidirectional mode
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- Control of SPI operation during wait mode

9.1.2 Modes of Operation

The SPI functions in three modes, run, wait, and stop.

- Run Mode
This is the basic mode of operation.
- Wait Mode
SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in Run Mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into Run Mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.
- Stop Mode
The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

This is a high level description only, detailed descriptions of operating modes are contained in [Section 9.4, “Functional Description.”](#)

Table 10-8. IBSR Field Descriptions (continued)

Field	Description
2 SRW	Slave Read/Write — When IAAS is set this bit indicates the value of the R/W command bit of the calling address sent from the master This bit is only valid when the I-bus is in slave mode, a complete address transfer has occurred with an address match and no other transfers have been initiated. Checking this bit, the CPU can select slave transmit/receive mode according to the command of the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IBIF	I-Bus Interrupt — The IBIF bit is set when one of the following conditions occurs: — Arbitration lost (IBAL bit set) — Byte transfer complete (TCF bit set) — Addressed as slave (IAAS bit set) It will cause a processor interrupt request if the IBIE bit is set. This bit must be cleared by software, writing a one to it. A write of 0 has no effect on this bit.
0 RXAK	Received Acknowledge — The value of SDA during the acknowledge bit of a bus cycle. If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If RXAK is high, it means no acknowledge signal is detected at the 9th clock. 0 Acknowledge received 1 No acknowledge received

10.3.2.5 IIC Data I/O Register (IBDR)

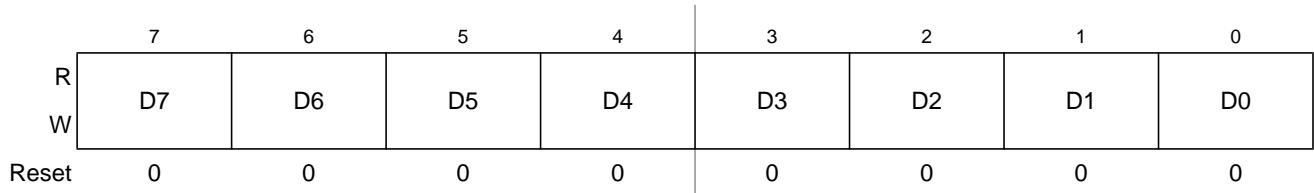


Figure 10-7. IIC Bus Data I/O Register (IBDR)

In master transmit mode, when data is written to the IBDR a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates next byte data receiving. In slave mode, the same functions are available after an address match has occurred. Note that the Tx/Rx bit in the IBCR must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, then reading the IBDR will not initiate the receive.

Reading the IBDR will return the last byte received while the IIC is configured in either master receive or slave receive modes. The IBDR does not reflect every byte that is transmitted on the IIC bus, nor can software verify that a byte has been written to the IBDR correctly by reading it back.

In master transmit mode, the first byte of data written to IBDR following assertion of $\overline{MS}/\overline{SL}$ is used for the address transfer and should comprise of the calling address (in position D7:D1) concatenated with the required R/\overline{W} bit (in position D0).

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDA line for the master to generate STOP or START signal.

10.4.1.4 STOP Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called repeated START. A STOP signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see [Figure 10-8](#)).

The master can generate a STOP even if the slave has generated an acknowledge at which point the slave must release the bus.

10.4.1.5 Repeated START Signal

As shown in [Figure 10-8](#), a repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

10.4.1.6 Arbitration Procedure

The Inter-IC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case the transition from master to slave mode does not generate a STOP condition. Meanwhile, a status bit is set by hardware to indicate loss of arbitration.

10.4.1.7 Clock Synchronization

Because wire-AND logic is performed on SCL line, a high-to-low transition on SCL line affects all the devices connected on the bus. The devices start counting their low period and as soon as a device's clock has gone low, it holds the SCL line low until the clock high state is reached. However, the change of low to high in this device clock may not change the state of the SCL line if another device clock is within its low period. Therefore, synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time (see [Figure 10-9](#)). When all devices concerned have counted off their low period, the synchronized clock SCL line is released and pulled high. There is then no difference between the device clocks and the state of the SCL line and all the devices start counting their high periods. The first device to complete its high period pulls the SCL line low again.

In slave transmitter routine, the received acknowledge bit (RXAK) must be tested before transmitting the next byte of data. Setting RXAK means an 'end of data' signal from the master receiver, after which it must be switched from transmitter mode to receiver mode by software. A dummy read then releases the SCL line so that the master can generate a STOP signal.

10.7.1.7 Arbitration Lost

If several masters try to engage the bus simultaneously, only one master wins and the others lose arbitration. The devices which lost arbitration are immediately switched to slave receive mode by the hardware. Their data output to the SDA line is stopped, but SCL continues to be generated until the end of the byte during which arbitration was lost. An interrupt occurs at the falling edge of the ninth clock of this transfer with IBAL=1 and MS/SL=0. If one master attempts to start transmission while the bus is being engaged by another master, the hardware will inhibit the transmission; switch the MS/SL bit from 1 to 0 without generating STOP condition; generate an interrupt to CPU and set the IBAL to indicate that the attempt to engage the bus is failed. When considering these cases, the slave service routine should test the IBAL first and the software should clear the IBAL bit if it is set.

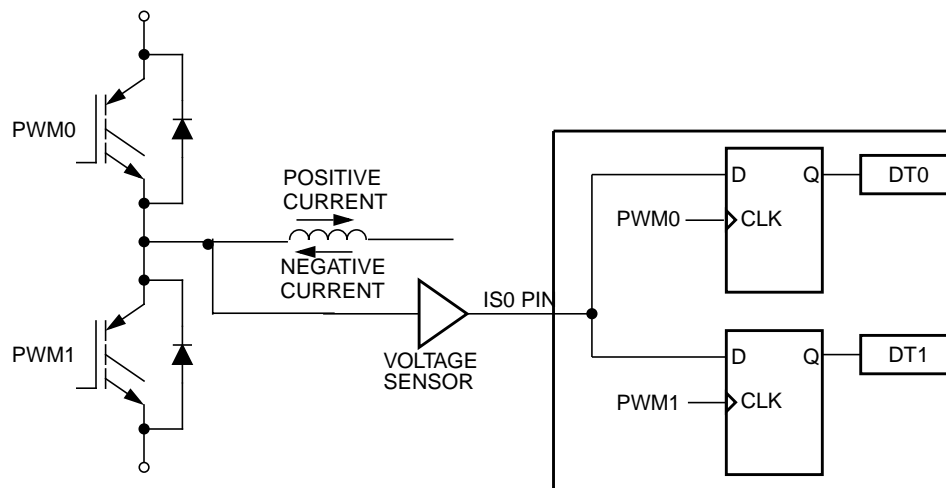


Figure 11-55. Current-Status Sense Scheme for Deadtime Correction

If both D flip-flops latch low, $DT0 = 0$, $DT1 = 0$, during deadtime periods if current is large and flowing out of the complementary circuit. See Figure 11-55. If both D flip-flops latch the high, $DT0 = 1$, $DT1 = 1$, during deadtime periods if current is also large and flowing into the complementary circuit. However, under low-current, the output voltage of the complementary circuit during deadtime is somewhere between the high and low levels. The current cannot free-wheel throughout the opposition anti-body diode, regardless of polarity, giving additional distortion when the current crosses zero. Sampled results will be $DT0 = 0$ and $DT1 = 1$. Thus, the best time to change one PWM value register to another is just before the current zero crossing.

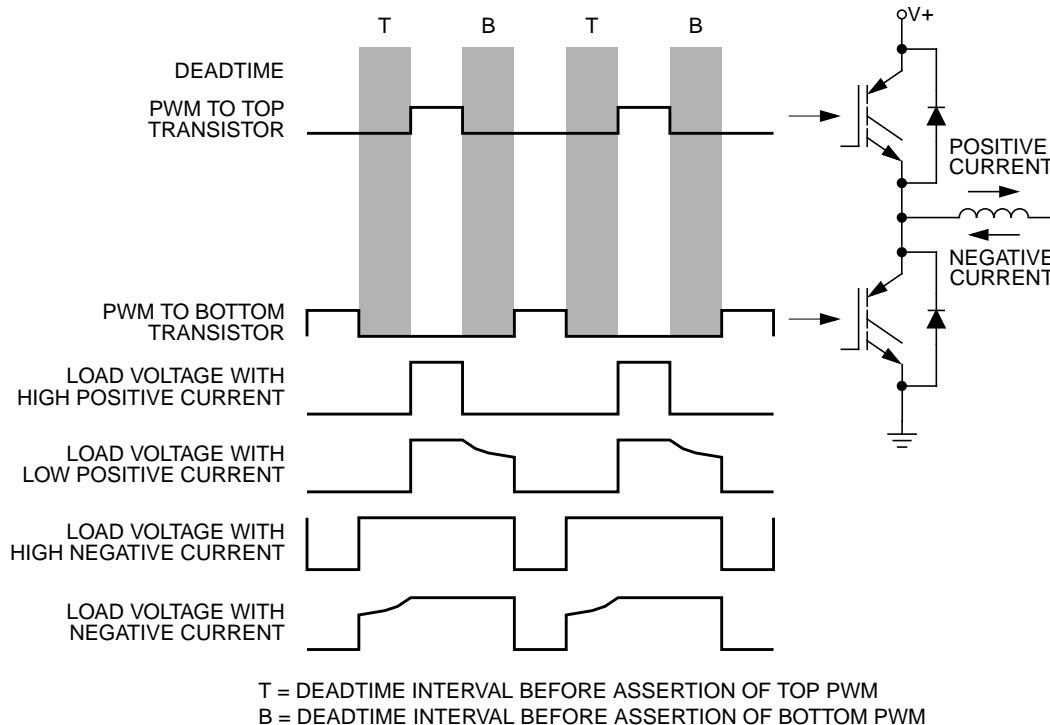


Figure 11-56. Output Voltage Waveforms

11.7 Interrupts

Seven PWM sources can generate CPU interrupt requests:

- Reload flag x (PWMRFx)—PWMRFx is set at the beginning of every PWM Generator x reload cycle. The reload interrupt enable bit, PWMRIEx, enables PWMRFx to generate CPU interrupt requests.
where x is A, B and C.
- Fault flag x (FFLAGx)—The FFLAGx bit is set when a logic one occurs on the FAULTx pin. The fault pin interrupt enable x bit, FIEEx, enables the FFLAGx flag to generate CPU interrupt requests.
where x is 0, 1, 2 and 3.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMDTY0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	Bit 7	6	5	4	3	2	1	Bit 0
PWMSDB	R	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
	W	PWMIF	PWMIE	PWMRSTRT	PWMLVL		PWM5IN	PWM5INL	PWM5ENA

= Unimplemented or Reserved

Figure 12-2. PWM Register Summary (continued)

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx period = channel clock period * PWMPERx center aligned output (CAEx = 1)
- PWMx period = channel clock period * (2 * PWMPERx)

For boundary case programming values, please refer to [Section 12.4.2.8, “PWM Boundary Cases.”](#)

	7	6	5	4	3	2	1	0
R								
W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-21. PWM Channel Period Registers (PWMPER0)

	7	6	5	4	3	2	1	0
R								
W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-22. PWM Channel Period Registers (PWMPER1)

	7	6	5	4	3	2	1	0
R								
W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-23. PWM Channel Period Registers (PWMPER2)

	7	6	5	4	3	2	1	0
R								
W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-24. PWM Channel Period Registers (PWMPER3)

	7	6	5	4	3	2	1	0
R								
W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-25. PWM Channel Period Registers (PWMPER4)

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000C TIE	R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
	W								
0x000E TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x0017 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0018–0x001F TCxH–TCxL	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
0x0020 PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
	W								
0x0021 PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
	W								
0x0022 PACNTH	R	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
	W								
0x0023 PACNTL	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
0x0024–0x002F Reserved	R								
	W								


 = Unimplemented or Reserved

Figure 13-5. TIM16B4CV1 Register Summary (continued)

13.3.2.17 Pulse Accumulators Count Registers (PACNT)

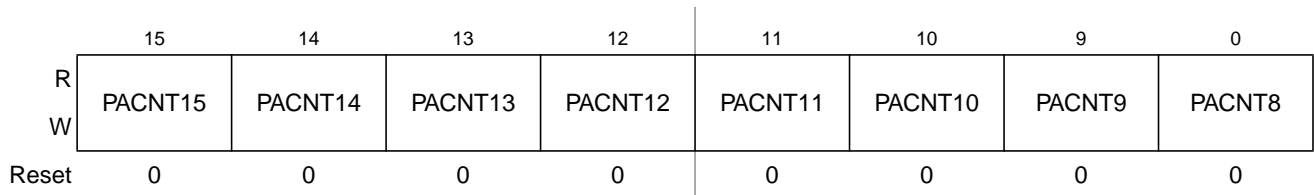


Figure 13-24. Pulse Accumulator Count Register High (PACNTH)

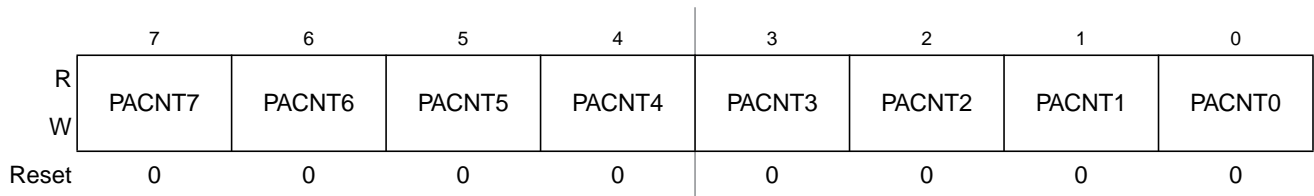


Figure 13-25. Pulse Accumulator Count Register Low (PACNTL)

Read: Anytime

Write: Anytime

These registers contain the number of active input edges on its input pin since the last reset.

When PACNT overflows from 0xFFFF to 0x0000, the Interrupt flag PAOVF in PAFLG (0x0021) is set.

Full count register access should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

NOTE

Reading the pulse accumulator counter registers immediately after an active edge on the pulse accumulator input pin may miss the last count because the input has to be synchronized with the bus clock first.

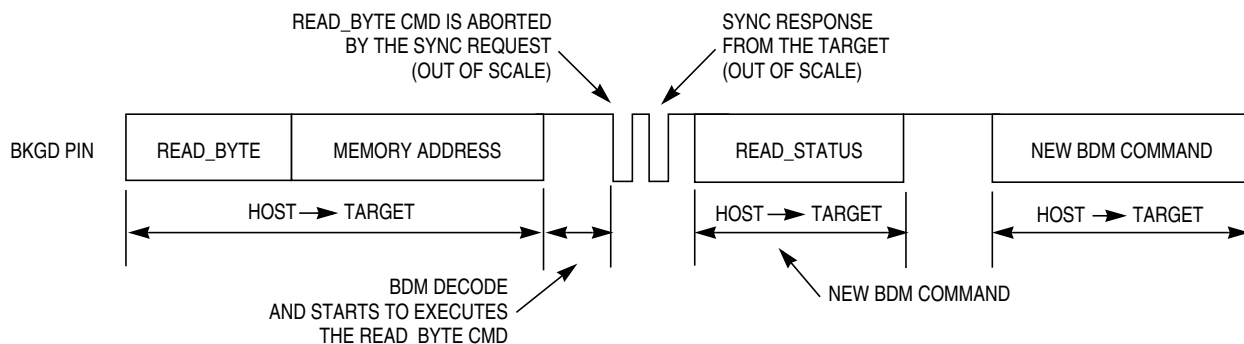


Figure 15-12. ACK Abort Procedure at the Command Level

Figure 15-13 shows a conflict between the ACK pulse and the SYNC request pulse. This conflict could occur if a POD device is connected to the target BKGD pin and the target is already in debug active mode. Consider that the target CPU is executing a pending BDM command at the exact moment the POD is being connected to the BKGD pin. In this case, an ACK pulse is issued along with the SYNC command. In this case, there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. Because this is not a probable situation, the protocol does not prevent this conflict from happening.

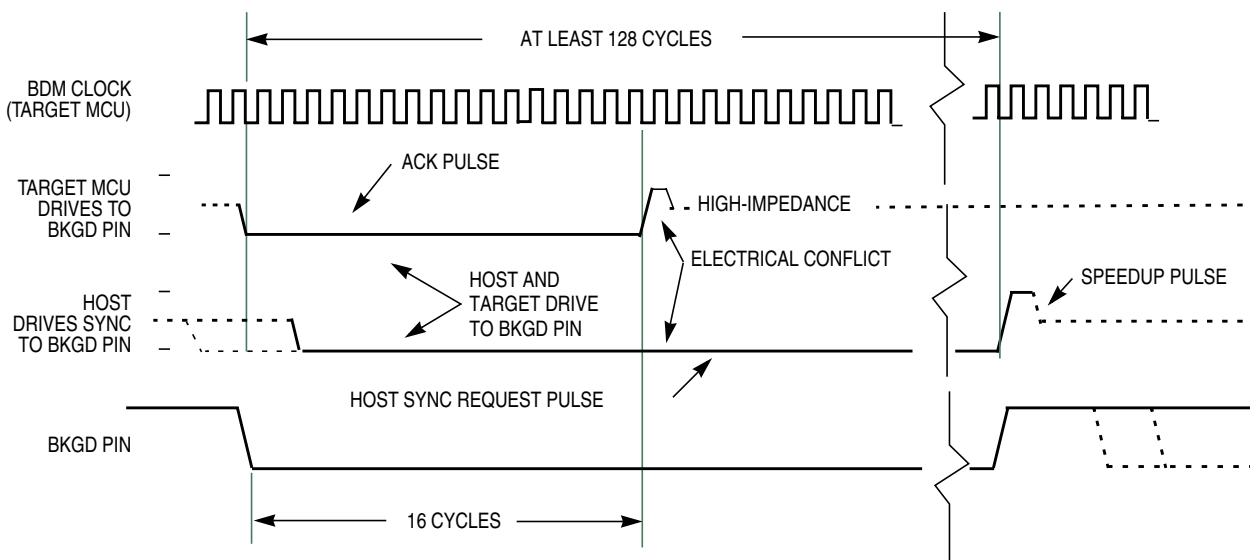


Figure 15-13. ACK Pulse and SYNC Request Conflict

NOTE

This information is being provided so that the MCU integrator will be aware that such a conflict could eventually occur.

The hardware handshake protocol is enabled by the `ACK_ENABLE` and disabled by the `ACK_DISABLE` BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

19.3.2.2 Initialization of Internal Registers Position Register (INITRG)

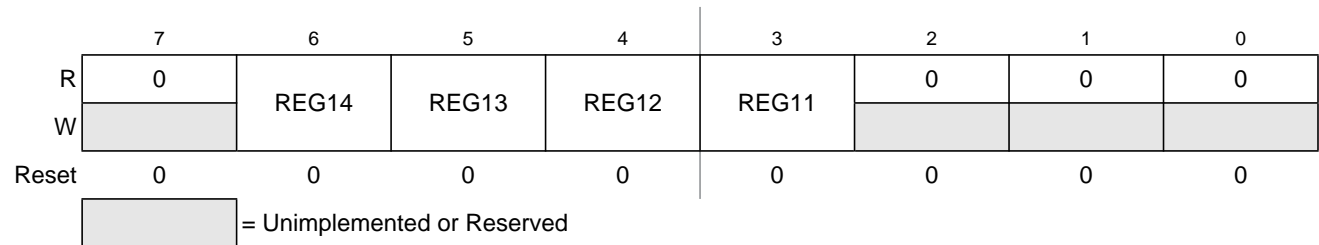


Figure 19-4. Initialization of Internal Registers Position Register (INITRG)

Read: Anytime

Write: Once in normal and emulation modes and anytime in special modes

This register initializes the position of the internal registers within the on-chip system memory map. The registers occupy either a 1K byte or 2K byte space and can be mapped to any 2K byte space within the first 32K bytes of the system’s address space.

Table 19-3. INITRG Field Descriptions

Field	Description
6:3 REG[14:11]	Internal Register Map Position — These four bits in combination with the leading zero supplied by bit 7 of INITRG determine the upper five bits of the base address for the system’s internal registers (i.e., the minimum base address is 0x0000 and the maximum is 0x7FFF).

A.2 Voltage Regulator

This section describes the characteristics of the on chip voltage regulator.

Table A-9. Voltage Regulator Electrical Parameters

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Input Voltages	$V_{VDDR,A}$	2.97	—	5.5	V
3	P	Output Voltage Core Full Performance Mode	V_{DD}	2.35	2.5	2.75	V
4	P	Output Voltage PLL Full Performance Mode	V_{DDPLL}	2.35	2.5	2.75	V
5	P	Low Voltage Interrupt ¹ Assert Level Deassert Level	V_{LVIA} V_{LVID}	4.1 4.25	4.37 4.52	4.66 4.77	V V
6	P	Low Voltage Reset ² Assert Level Deassert Level	V_{LVRA} V_{LVRD}	2.25 —	— —	— 2.55	V V
7	C	Power-on Reset ³ Assert Level Deassert Level	V_{PORA} V_{PORD}	0.97 —	— —	— 2.05	V V

¹ Monitors V_{DDA} , active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.

² Monitors V_{DD} , active only in Full Performance Mode. V_{LVRA} and V_{PORD} must overlap

³ Monitors V_{DD} . Active in all modes.

The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Freescale and are subject to change without notice.

A.6.3.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq 1\text{LSB}$, then the external filter capacitor, $C_f \geq 1024 * (C_{\text{INS}} - C_{\text{INN}})$.

A.6.3.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (0xFF in 8-bit mode) for analog inputs greater than VRH and 0x000 for values less than VRL unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as

$V_{\text{ERR}} = K * R_S * I_{\text{INJ}}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-21. ATD Electrical Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Max input Source Resistance	R_S	—	—	1	K Ω
2	T	Total Input Capacitance	C_{INN} C_{INS}	—	—	10	pF
		Non Sampling Sampling		—	—	15	
3	C	Disruptive Analog Input Current	I_{NA}	−2.5	—	2.5	mA
4	C	Coupling Ratio positive current injection	K_p	—	—	10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n	—	—	10^{-2}	A/A

B.2 80-Pin QFP Package

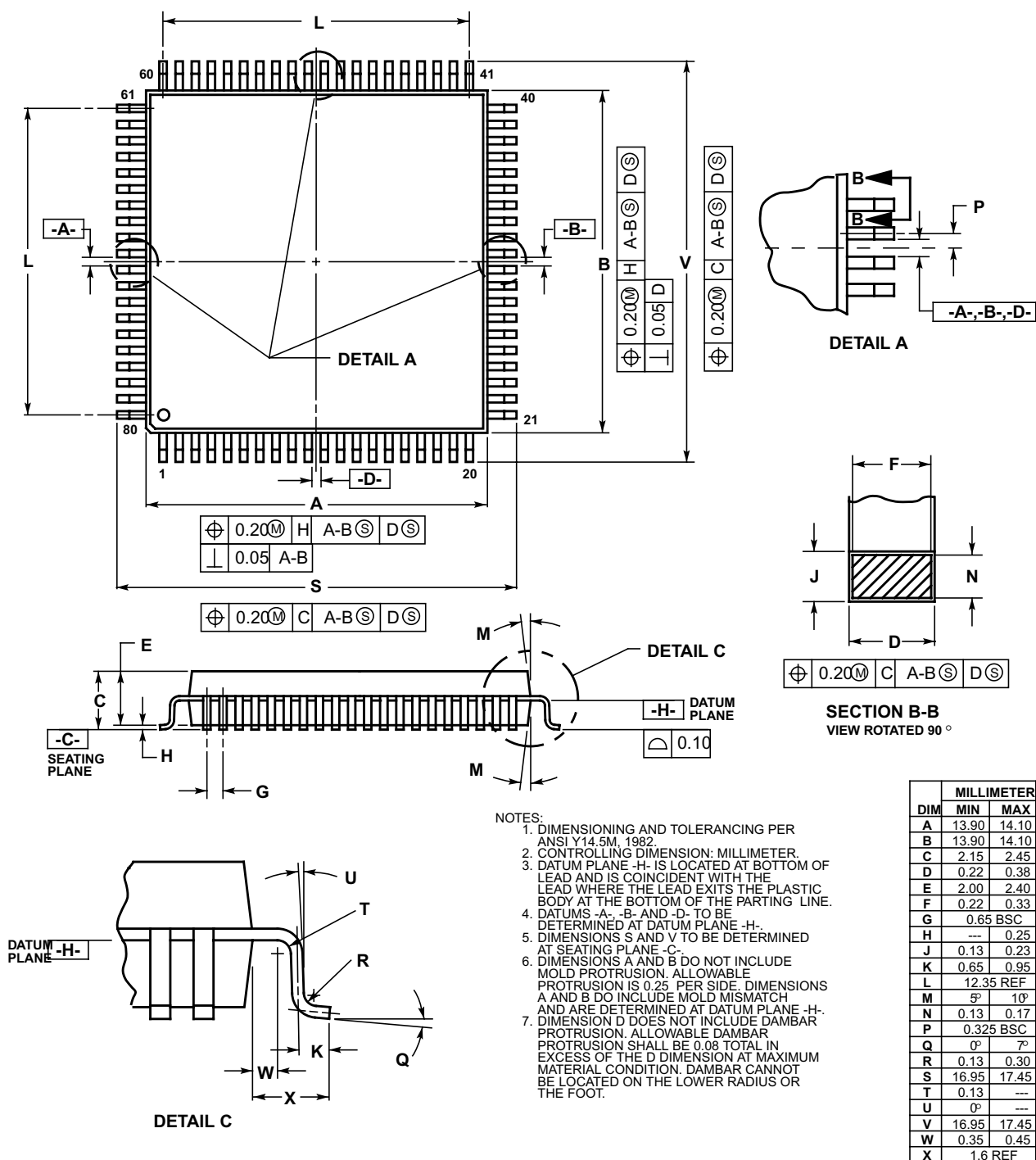


Figure B-2. 80-Pin QFP Mechanical Dimensions (Case no. 841B)