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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	92
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.135V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12e64cpv

Chapter 2
128 Kbyte Flash Module (FTS128K1V1)

Chapter 3
Port Integration Module (PIM9E128V1)

Chapter 13
Timer Module (TIM16B4CV1)

Chapter 14
Dual Output Voltage Regulator (VREG3V3V2)

Chapter 15
Background Debug Module (BDMV4)

0x0240 – 0x027F PIM (Port Interface Module) (Sheet 3 of 4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x025D	PPSP	R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
		W								
0x025E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0260	PTQ	R	0	PTQ6	PTQ5	PTQ4	PTQ3	PTQ2	PTQ1	PTQ0
		W								
0x0261	PTIQ	R	0	PTIQ6	PTIQ5	PTIQ4	PTIQ3	PTIQ2	PTIQ1	PTIQ0
		W								
0x0262	DDRQ	R	0	DDRQ6	DDRQ5	DDRQ4	DDRQ3	DDRQ2	DDRQ1	DDRQ0
		W								
0x0263	RDRQ	R	0	RDRQ6	RDRQ5	RDRQ4	RDRQ3	RDRQ2	RDRQ1	RDRQ0
		W								
0x0264	PERQ	R	0	PERQ6	PERQ5	PERQ4	PERQ3	PERQ2	PERQ1	PERQ0
		W								
0x0265	PPSQ	R	0	PPSQ6	PPSQ5	PPSQ4	PPSQ3	PPSQ2	PPSQ1	PPSQ0
		W								
0x0266	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0267	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0268	PTU	R	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		W								
0x0269	PTIU	R	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		W								
0x026A	DDRU	R	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		W								
0x026B	RDRU	R	RDRU7	RDRU6	RDRU5	RDRU4	RDRU3	RDRU2	RDRU1	RDRU0
		W								
0x026C	PERU	R	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		W								
0x026D	PPSU	R	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		W								
0x026E	MODRR	R	0	0	0	0	MODRR3	MODRR2	MODRR1	MODRR0
		W								
0x026F	Reserved	R	0	0	0	0	0	0	0	0
		W								

1.4.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when RESET is low. PE5 is not available in the 80-pin package version.

1.4.11 PE4 / ECLK— Port E I/O Pin 4 / E-Clock Output

PE4 is a general purpose input or output pin. In Normal Single Chip mode PE4 is configured with an active pull-up while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. In all modes except Normal Single Chip Mode, the PE4 pin is initially configured as the output connection for the internal bus clock (ECLK). ECLK is used as a timing reference and to demultiplex the address and data in expanded modes. The ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the ECLK, are halted when the MCU is in STOP mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. The PE4 pin is initially configured as ECLK output with stretch in all expanded modes. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the ECLK is available for use in external select decode logic or as a constant speed clock for use in the external application system.

1.4.12 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3 / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

PE3 can be used as a general-purpose I/O in all modes and is an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. PE3 can also be configured as a Low-Byte Strobe ($\overline{\text{LSTRB}}$). The $\overline{\text{LSTRB}}$ signal is used in write operations, so external low byte writes will not be possible until this function is enabled. $\overline{\text{LSTRB}}$ can be enabled by setting the LSTRE bit in the PEAR register. In Expanded Wide and Emulation Narrow modes, and when BDM tagging is enabled, the $\overline{\text{LSTRB}}$ function is multiplexed with the $\overline{\text{TAGLO}}$ function. When enabled a logic zero on the $\overline{\text{TAGLO}}$ pin at the falling edge of ECLK will tag the low byte of an instruction word being read into the instruction queue. PE3 is not available in the 80 pin package version.

1.4.13 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2 / Read/$\overline{\text{Write}}$

PE2 can be used as a general-purpose I/O in all modes and is configured an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. If the read/$\overline{\text{write}}$ function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until the read/$\overline{\text{write}}$ function is enabled. The PE2 pin is not available in the 80 pin package version.

1.4.14 PE1 / $\overline{\text{IRQ}}$ — Port E input Pin 1 / Maskable Interrupt Pin

PE1 is always an input and can always be read. The PE1 pin is also the $\overline{\text{IRQ}}$ input used for requesting an asynchronous interrupt to the MCU. During reset, the I bit in the condition code register (CCR) is set and any $\overline{\text{IRQ}}$ interrupt is masked until software enables it by clearing the I bit. The $\overline{\text{IRQ}}$ is software

programmable to either falling edge-sensitive triggering or level-sensitive triggering based on the setting of the IRQE bit in the IRQCR register. The $\overline{\text{IRQ}}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit in the IRQCR register. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

1.4.15 PE0 / $\overline{\text{XIRQ}}$ — Port E input Pin 0 / Non Maskable Interrupt Pin

PE0 is always an input and can always be read. The PE0 pin is also the $\overline{\text{XIRQ}}$ input for requesting a nonmaskable asynchronous interrupt to the MCU. During reset, the X bit in the condition code register (CCR) is set and any $\overline{\text{XIRQ}}$ interrupt is masked until MCU software enables it by clearing the X bit. Because the $\overline{\text{XIRQ}}$ input is level sensitive triggered, it can be connected to a multiple-source wired-OR network. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

1.4.16 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). In expanded modes the PK7 pin can be used to determine the reset state of the ROMON bit in the MISC register. At the rising edge of $\overline{\text{RESET}}$, the state of the PK7 pin is latched to the ROMON bit. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI block description chapter for further details. PK7 is not available in the 80 pin package version.

1.4.17 PK6 / $\overline{\text{XCS}}$ — Port K I/O Pin 6

PK6 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as an external chip select signal for most external accesses that are not selected by ECS. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI block description chapter for further details. PK6 is not available in the 80 pin package version.

1.4.18 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK[5:0] are general purpose input or output pins. In MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, PK[5:0] provide the expanded address XADDR[19:14] for the external bus. There are active pull-ups on PK[5:0] pins while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI block description chapter for further details. PK[5:0] are not available in the 80 pin package version.

1.4.19 PAD[15:0] / AN[15:0] / KWAD[15:0] — Port AD I/O Pins [15:0]

PAD[15:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input or output pin. When enabled as digital inputs or outputs, the PAD[15:0] can

2.4.1.3.1 Erase Verify Command

The erase verify operation will verify that a Flash array is erased.

An example flow to execute the erase verify operation is shown in Figure 2-22. The erase verify command write sequence is as follows:

1. Write to a Flash array address to start the command write sequence for the erase verify command. The address and data written will be ignored.
2. Write the erase verify command, 0x05, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the erase verify command.

After launching the erase verify command, the CCIF flag in the FSTAT register will set after the operation has completed unless a new command write sequence has been buffered. Upon completion of the erase verify operation, the BLANK flag in the FSTAT register will be set if all addresses in the Flash array are verified to be erased. If any address in the Flash array is not erased, the erase verify operation will terminate and the BLANK flag in the FSTAT register will remain clear.

3.2 External Signal Description

This section lists and describes the signals that connect off chip.

Table 3-1 shows all the pins and their functions that are controlled by the PIM9E128V1. The order in which the pin functions are listed represents the functions priority (top – highest priority, bottom – lowest priority).

Table 3-1. Detailed Signal Descriptions (Sheet 1 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
—	BKGD	MODC	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		BKGD	Refer to the BDM block description chapter	
		$\overline{\text{TAGHI}}$	Refer to the MEBI block description chapter	
Port A	PA7	ADDR15/DATA15	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		GPIO	General-purpose I/O	
	PA6	ADDR14/DATA14	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA5	ADDR13/DATA13	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA4	ADDR12/DATA12	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA3	ADDR11/DATA11	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA2	ADDR10/DATA10	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA1	ADDR9/DATA9	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA0	ADDR8/DATA8	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
Port B	PB7	ADDR7/DATA7	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		GPIO	General-purpose I/O	
	PB6	ADDR6/DATA6	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB5	ADDR5/DATA5	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB4	ADDR4/DATA4	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB3	ADDR3/DATA3	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB2	ADDR2/DATA2	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB1	ADDR1/DATA1	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB0	ADDR0/DATA0	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	

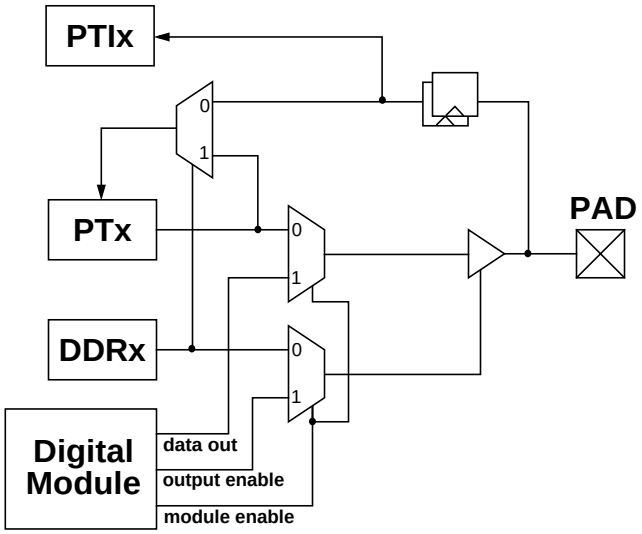

Figure 3-49. Illustration of I/O Pin Functionality

Figure 3-50 shows the state of digital inputs and outputs when an analog module drives the port. When the analog module is enabled all associated digital output ports are disabled and all associated digital input ports read “1”.

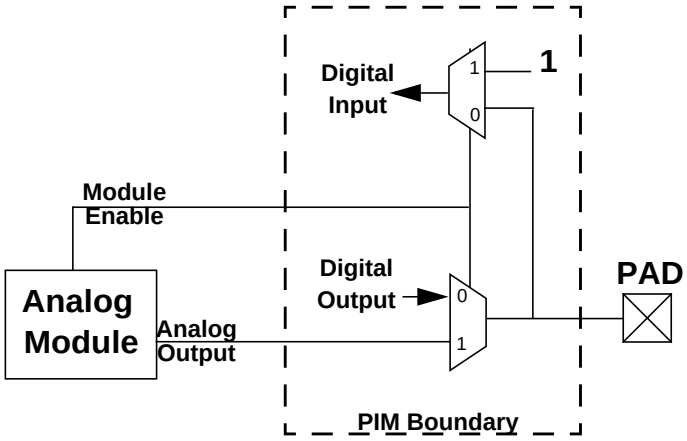

Figure 3-50. Digital Ports and Analog Module

3.4.4 Reduced Drive Register

If the port is used as an output the Reduced Drive Register allows the configuration of the drive strength.

3.4.5 Pull Device Enable Register

The Pull Device Enable Register turns on a pull-up or pull-down device. The pull device becomes active only if the pin is used as an input or as a wired-or output.

Chapter 6
Analog-to-Digital Converter (ATD10B16CV2)

6.1 Introduction

The ATD10B16C is a 16-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to the Electrical Specifications chapter for ATD accuracy.

6.1.1 Features

- 8-/10-bit resolution
- 7 µs, 10-bit single conversion time
- Sample buffer amplifier
- Programmable sample time
- Left/right justified, signed/unsigned result data
- External trigger control
- Conversion completion interrupt generation
- Analog input multiplexer for 16 analog input channels
- Analog/digital input pin multiplexing
- 1 to 16 conversion sequence lengths
- Continuous conversion mode
- Multiple channel scans

6.1.2 Modes of Operation

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

6.1.3 Block Diagram

Refer to Figure 6-1 for a block diagram of the ATD0B16C block.

- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

8.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low-power modes, wait and stop modes.

8.1.3.1 Run Mode

Normal mode of operation.

8.1.3.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.

  If SCISWAI is set, any transmission or reception in progress stops at wait mode entry. The transmission or reception resumes when either an internal or external interrupt brings the CPU out of wait mode. Exiting wait mode by reset aborts any transmission or reception in progress and resets the SCI.

8.1.3.3 Stop Mode

The SCI is inactive during stop mode for reduced power consumption. The STOP instruction does not affect the SCI register states, but the SCI bus clock will be disabled. The SCI operation resumes after an

Table 10-8. IBSR Field Descriptions (continued)

Field	Description
2 SRW	**Slave Read/Write** — When IAAS is set this bit indicates the value of the R/W command bit of the calling address sent from the master This bit is only valid when the I-bus is in slave mode, a complete address transfer has occurred with an address match and no other transfers have been initiated. Checking this bit, the CPU can select slave transmit/receive mode according to the command of the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IBIF	**I-Bus Interrupt** — The IBIF bit is set when one of the following conditions occurs: — Arbitration lost (IBAL bit set) — Byte transfer complete (TCF bit set) — Addressed as slave (IAAS bit set) It will cause a processor interrupt request if the IBIE bit is set. This bit must be cleared by software, writing a one to it. A write of 0 has no effect on this bit.
0 RXAK	**Received Acknowledge** — The value of SDA during the acknowledge bit of a bus cycle. If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If RXAK is high, it means no acknowledge signal is detected at the 9th clock. 0 Acknowledge received 1 No acknowledge received

10.3.2.5 IIC Data I/O Register (IBDR)

	7	6	5	4	3	2	1	0
R W	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Figure 10-7. IIC Bus Data I/O Register (IBDR)

In master transmit mode, when data is written to the IBDR a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates next byte data receiving. In slave mode, the same functions are available after an address match has occurred.Note that the Tx/Rx bit in the IBCR must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, then reading the IBDR will not initiate the receive.

Reading the IBDR will return the last byte received while the IIC is configured in either master receive or slave receive modes. The IBDR does not reflect every byte that is transmitted on the IIC bus, nor can software verify that a byte has been written to the IBDR correctly by reading it back.

In master transmit mode, the first byte of data written to IBDR following assertion of MS/$\overline{SL}$ is used for the address transfer and should com.prise of the calling address (in position D7:D1) concatenated with the required R/$\overline{W}$ bit (in position D0).

11.3.2 Register Descriptions

The address of a register is the sum of a base address and an address offset. The base address is defined at the chip level and the address offset is defined at the module level.

11.3.2.1 PMF Configure 0 Register (PMFCFG0)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
Reset	0	0	0	0	0	0	0	0

Figure 11-4. PMF Configure 0 Register (PMFCFG0)

Read anytime.

See bit description for write conditions.

Table 11-2. PMFCFG0 Field Descriptions

Field	Description
7 WP	**Write Protect** — This bit enables write protection to be used for all write-protectable registers. While clear, WP allows write-protected registers to be written. When set, WP prevents any further writes to write-protected registers. Once set, WP can be cleared only by reset. 0 Write-protectable registers may be written. 1 Write-protectable registers are write-protected.
6 MTG	**Multiple Timebase Generators** — This bit determines the number of timebase counters used. Once set, MTG can be cleared only by reset. If MTG is set, PWM generators B and C and registers $xx28–$xx37 are available. The three generators have their own variable frequencies and are not synchronized. If MTG is cleared, PMF registers from $xx28–$xx37 can not be written and read zeroes, and bits EDGEC and EDGEB are ignored. Pair A, Pair B and Pair C PWMs are synchronized to PWM generator A and use registers from $xx20–$xx27. 0 Single timebase generator. 1 Multiple timebase generators.
5 EDGEC	**Edge-Aligned or Center-Aligned PWM for Pair C** — This bit determines whether PWM4 and PWM5 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are center-aligned PWMs 1 PWM4 and PWM5 are edge-aligned PWMs
4 EDGEB	**Edge-Aligned or Center-Aligned PWM for Pair B** — This bit determines whether PWM2 and PWM3 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are center-aligned PWMs 1 PWM2 and PWM3 are edge-aligned PWMs

In an edge-aligned operation, the PWM counter is an up counter. The PWM output resolution is one bus clock cycle.

PWM period = PWM modulus × PWM clock period

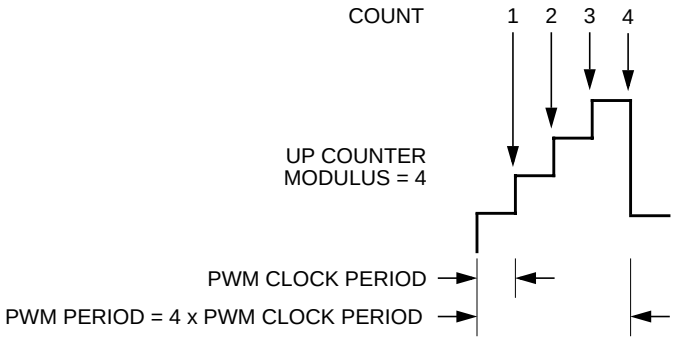

Figure 11-44. Edge-Aligned PWM Period

11.4.3.3 Duty Cycle

The signed 16-bit number written to the PMF value registers is the pulse width in PWM clock periods of the PWM generator output.

$$\text{Duty cycle} = \frac{\text{PMFVAL}}{\text{MODULUS}} \times 100$$

NOTE

A PWM value less than or equal to zero deactivates the PWM output for the entire PWM period. A PWM value greater than or equal to the modulus activates the PWM output for the entire PWM period.

Table 11-46. PWM Value and Underflow Conditions

PMFVALx	Condition	PWM Value Used
$0000–$7FFF	Normal	Value in registers
$8000–$FFFF	Underflow	$0000

13.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

	7	6	5	4	3	2	1	0
R	IOS7	IOS6	IOS5	IOS4	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 13-6. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 13-2. TIOS Field Descriptions

Field	Description
7:4 IOS[7:4]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding channel acts as an input capture. 1 The corresponding channel acts as an output compare.

13.3.2.2 Timer Compare Force Register (CFORC)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	FOC7	FOC6	FOC5	FOC4				
Reset	0	0	0	0	0	0	0	0

Figure 13-7. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 13-3. CFORC Field Descriptions

Field	Description
7:4 FOC[7:4]	**Force Output Compare Action for Channel 7:4** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. **Note:** A successful channel 7 output compare overrides any channel 6:4 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

Table 13-6. TSCR1 Field Descriptions (continued)

Field	Description
5 TSFRZ	**Timer Stops While in Freeze Mode** 0 Allows the timer counter to continue running while in freeze mode. 1 Disables the timer counter whenever the MCU is in freeze mode. This is useful for emulation. TSFRZ does not stop the pulse accumulator.
4 TFFCA	**Timer Fast Flag Clear All** 0 Allows the timer flag clearing to function normally. 1 For TFLG1(0x000E), a read from an input capture or a write to the output compare channel (0x0010–0x001F) causes the corresponding channel flag, CnF, to be cleared. For TFLG2 (0x000F), any access to the TCNT register (0x0004, 0x0005) clears the TOF flag. Any access to the PACNT registers (0x0022, 0x0023) clears the PAOVF and PAIF flags in the PAFLG register (0x0021). This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.

13.3.2.7 Timer Toggle On Overflow Register 1 (TTOV)

	7	6	5	4	3	2	1	0
R	TOV7	TOV6	TOV5	TOV4	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 13-13. Timer Toggle On Overflow Register 1 (TTOV)

Read: Anytime

Write: Anytime

Table 13-7. TTOV Field Descriptions

Field	Description
7:4 TOV[7:4]	**Toggle On Overflow Bits** — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 7 override events. 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

13.3.2.8 Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0
R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
W								
Reset	0	0	0	0	0	0	0	0

Figure 13-14. Timer Control Register 1 (TCTL1)

Read: Anytime

Write: Anytime

13.6 Interrupts

This section describes interrupts originated by the TIM16B4CV1 block. Table 13-21 lists the interrupts generated by the TIM16B4CV1 to communicate with the MCU.

Table 13-21. TIM16B8CV1 Interrupts

Interrupt	Offset[1]	Vector[1]	Priority[1]	Source	Description
C[7:4]F	—	—	—	Timer Channel 7–4	Active high timer channel interrupts 7–4
PAOVI	—	—	—	Pulse Accumulator Input	Active high pulse accumulator input interrupt
PAOVF	—	—	—	Pulse Accumulator Overflow	Pulse accumulator overflow interrupt
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

1 Chip Dependent.

The TIM16B4CV1 uses a total of 7 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

13.6.1 Channel [7:4] Interrupt (C[7:4]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 4 interrupt to be serviced by the system controller.

13.6.2 Pulse Accumulator Input Interrupt (PAOVI)

This active high output will be asserted by the module to request a timer pulse accumulator input interrupt to be serviced by the system controller.

13.6.3 Pulse Accumulator Overflow Interrupt (PAOVF)

This active high output will be asserted by the module to request a timer pulse accumulator overflow interrupt to be serviced by the system controller.

13.6.4 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt to be serviced by the system controller.

- Calculates the address of the next instruction after the CALL instruction (the return address), and pushes this 16-bit value onto the stack.
- Pushes the old PPAGE value onto the stack.
- Calculates the effective address of the subroutine, refills the queue, and begins execution at the new address on the selected page of the expansion window.

This sequence is uninterruptable; there is no need to inhibit interrupts during CALL execution. A CALL can be performed from any address in memory to any other address.

The PPAGE value supplied by the instruction is part of the effective address. For all addressing mode variations except indexed-indirect modes, the new page value is provided by an immediate operand in the instruction. In indexed-indirect variations of CALL, a pointer specifies memory locations where the new page value and the address of the called subroutine are stored. Using indirect addressing for both the new page value and the address within the page allows values calculated at run time rather than immediate values that must be known at the time of assembly.

The RTC instruction terminates subroutines invoked by a CALL instruction. RTC unstacks the PPAGE value and the return address and refills the queue. Execution resumes with the next instruction after the CALL.

During the execution of an RTC instruction, the CPU:

- Pulls the old PPAGE value from the stack
- Pulls the 16-bit return address from the stack and loads it into the PC
- Writes the old PPAGE value into the PPAGE register
- Refills the queue and resumes execution at the return address

This sequence is uninterruptable; an RTC can be executed from anywhere in memory, even from a different page of extended memory in the expansion window.

The CALL and RTC instructions behave like JSR and RTS, except they use more execution cycles. Therefore, routinely substituting CALL/RTC for JSR/RTS is not recommended. JSR and RTS can be used to access subroutines that are on the same page in expanded memory. However, a subroutine in expanded memory that can be called from other pages must be terminated with an RTC. And the RTC unstacks a PPAGE value. So any access to the subroutine, even from the same page, must use a CALL instruction so that the correct PPAGE value is in the stack.

19.4.3.2 Extended Address (XAB19:14) and $\overline{\text{ECS}}$ Signal Functionality

If the EMK bit in the MODE register is set (see MEBI block description chapter) the PIX5:0 values will be output on XAB19:14 respectively (port K bits 5:0) when the system is addressing within the physical program page window address space (0x8000–0xBFFF) and is in an expanded mode. When addressing anywhere else within the physical address space (outside of the paging space), the XAB19:14 signals will be assigned a constant value based upon the physical address space selected. In addition, the active-low emulation chip select signal, $\overline{\text{ECS}}$, will likewise function based upon the assigned memory allocation. In the cases of 48K byte and 64K byte allocated physical FLASH/ROM space, the operation of the $\overline{\text{ECS}}$ signal will additionally depend upon the state of the ROMHM bit (see Section 19.3.2.4, “Miscellaneous System Control Register (MISC)”) in the MISC register. Table 19-18, Table 19-19, Table 19-20, and

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8. Supply Current Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}	—	—	65	mA
2		Wait Supply current	I_{DDW}				mA
	P	All modules enabled		—	—	40	
	P	only RTI enabled		—	—	5	
3		Pseudo Stop Current (RTI and COP enabled) [1, 2]	I_{DDPS}				µA
	C	–40°C		—	570	—	
	C	27°C		—	600	—	
	C	70°C		—	650	—	
	C	85°C		—	750	—	
	C	105°C		—	850	—	
	C	125°C		—	1200	—	
	C	140°C		—	1500	—	
4		Pseudo Stop Current (RTI and COP disabled) [1,2]	I_{DDPS}				µA
	C	-40°C		—	370	—	
	P	27°C		—	400	500	
	C	70°C		—	450	—	
	C	85°C		—	550	—	
	P	"C" Temp Option 100°C		—	600	1600	
	C	105°C		—	650	—	
	P	"V" Temp Option 120°C		—	800	2100	
	C	125°C		—	850	—	
	P	"M" Temp Option 140°C		—	1200	5000	
5		Stop Current [2]	I_{DDS}				µA
	C	-40°C		—	12	—	
	P	27°C		—	30	100	
	C	70°C		—	100	—	
	C	85°C		—	130	—	
	P	"C" Temp Option 100°C		—	160	1200	
	C	105°C		—	200	—	
	P	"V" Temp Option 120°C		—	350	1700	
	C	125°C		—	400	—	
	P	"M" Temp Option 140°C		—	600	5000	

1 PLL off

2 At those low power dissipation levels $T_J = T_A$ can be assumed

A.6 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

A.6.1 ATD Operating Characteristics — 5V Range

The Table A-19 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-19. 5V ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted. Supply Voltage 5V-10% <= VDDA <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA/2}$	 — —	 $V_{DDA/2}$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}–V_{RL}	4.75	5.0	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[3] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5	 — — —	 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6	 — —	 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA} = 5.0 Volts)	t_{SR}	—	—	20	µs
7	P	Reference Supply current	I_{REF}	—	—	0.375	mA

1 Full accuracy is not guaranteed when differential voltage is less than 4.75V

2 The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

3 Reduced accuracy see Table A-22 and Table A-23.