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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	92
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
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MC9S12E128 Data Sheet

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MC9S12E128V1
Rev. 1.07
10/2005

freescale™
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0x0080 – 0x00AF ATD (Analog to Digital Converter 10 Bit 16 Channel) (Sheet 3 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x009E	ATDDR7H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009F	ATDDR7L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A0	ATDDR8H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A1	ATDDR8L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A2	ATDDR9H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A3	ATDDR9L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A4	ATDDR10H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A5	ATDDR10L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A6	ATDDR11H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A7	ATDDR11L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A8	ATDDR12H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A9	ATDDR12L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00AA	ATDDR13H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AB	ATDDR13L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00AC	ATDDR14H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AD	ATDDR14L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00AE	ATDDR15H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AF	ATDDR15L	R	Bit7	Bit6	0	0	0	0	0	0
		W								

[1] WRAP0–3 bits are available in version V04 of ATD10B16C

[2] ETRIGSEL and ETRIGCH0–3 bits are available in version V04 of ATD10B16C

0x0180 – 0x01AF TIM2 (Timer 16 Bit 4 Channels) (Sheet 2 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0189	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x018A	TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		W								
0x018B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x018C	TIE	R	C7I	C6I	C5I	C4I	0	0	0	0
		W								
0x018D	TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
		W								
0x018E	TFLG1	R	C7F	C6F	C5F	C4F	0	0	0	0
		W								
0x018F	TFLG2	R	TOF	0	0	0	0	0	0	0
		W								
0x0190	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0191	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0192	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0193	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0194	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0195	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0196	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0197	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0198	TC4 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0199	TC4 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x015A	TC5 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x019B	TC5 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x019C	TC6 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								

Table 2-2. Flash Array Memory Map Summary

MCU Address Range	PPAGE	Protectable Low Range	Protectable High Range	Array Relative Address[1]
0x0000–0x3FFF[2]	Unpaged (0x3D)	N.A.	N.A.	0x14000–0x17FFF
0x4000–0x7FFF	Unpaged (0x3E)	0x4000–0x43FF 0x4000–0x47FF 0x4000–0x4FFF 0x4000–0x5FFF	N.A.	0x18000–0x1BFFF
0x8000–0xBFFF	0x38	N.A.	N.A.	0x00000–0x03FFF
	0x39	N.A.	N.A.	0x04000–0x07FFF
	0x3A	N.A.	N.A.	0x08000–0x0BFFF
	0x3B	N.A.	N.A.	0x0C000–0x0FFFF
	0x3C	N.A.	N.A.	0x10000–0x13FFF
	0x3D	N.A.	N.A.	0x14000–0x17FFF
	0x3E	0x8000–0x83FF 0x8000–0x87FF 0x8000–0x8FFF 0x8000–0x9FFF	N.A.	0x18000–0x1BFFF
	0x3F	N.A.	0xB800–0xBFFF 0xB000–0xBFFF 0xA000–0xBFFF 0x8000–0xBFFF	0x1C000–0x1FFFF
0xC000–0xFFFF	Unpaged (0x3F)	N.A.	0xF800–0xFFFF 0xF000–0xFFFF 0xE000–0xFFFF 0xC000–0xFFFF	0x1C000–0x1FFFF

1 Inside Flash block.

2 If allowed by MCU.

2.4.1.3 Valid Flash Commands

Table 2-16 summarizes the valid Flash commands along with the effects of the commands on the Flash array.

Table 2-16. Valid Flash Commands

FCMD	Meaning	Function on Flash Array
0x05	Erase Verify	Verify all bytes in the Flash array are erased. If the Flash array is erased, the BLANK bit will set in the FSTAT register upon command completion.
0x20	Program	Program a word (2 bytes) in the Flash array.
0x40	Sector Erase	Erase all 1024 bytes in a sector of the Flash array.
0x41	Mass Erase	Erase all bytes in the Flash array. A mass erase of the full Flash array is only possible when FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register are set prior to launching the command.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

3.2 External Signal Description

This section lists and describes the signals that connect off chip.

Table 3-1 shows all the pins and their functions that are controlled by the PIM9E128V1. The order in which the pin functions are listed represents the functions priority (top – highest priority, bottom – lowest priority).

Table 3-1. Detailed Signal Descriptions (Sheet 1 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
—	BKGD	MODC	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		BKGD	Refer to the BDM block description chapter	
		$\overline{\text{TAGHI}}$	Refer to the MEBI block description chapter	
Port A	PA7	ADDR15/DATA15	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		GPIO	General-purpose I/O	
	PA6	ADDR14/DATA14	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA5	ADDR13/DATA13	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA4	ADDR12/DATA12	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA3	ADDR11/DATA11	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA2	ADDR10/DATA10	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA1	ADDR9/DATA9	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PA0	ADDR8/DATA8	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
Port B	PB7	ADDR7/DATA7	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		GPIO	General-purpose I/O	
	PB6	ADDR6/DATA6	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB5	ADDR5/DATA5	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB4	ADDR4/DATA4	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB3	ADDR3/DATA3	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB2	ADDR2/DATA2	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB1	ADDR1/DATA1	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PB0	ADDR0/DATA0	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	

3.3.2.5 Port M Pull Device Enable Register (PERM)

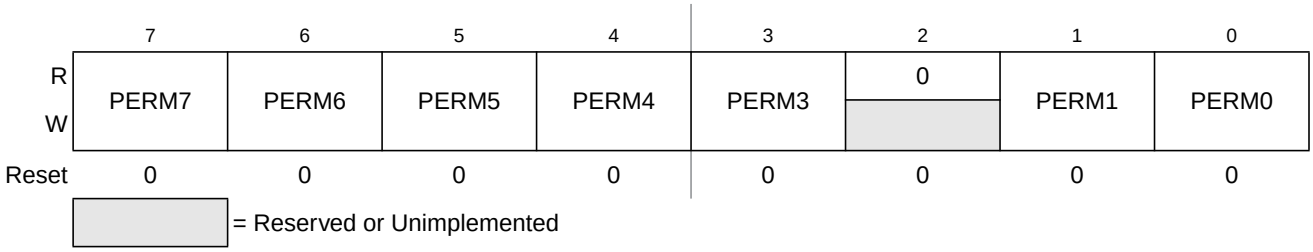


Figure 3-14. Port M Pull Device Enable Register (PERM)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input or wired-or output pins. If a pin is configured as push-pull output, the corresponding Pull Device Enable Register bit has no effect.

Table 3-11. PERM Field Descriptions

Field	Description
7:3, 1:0 PERM[7:3, 1:0]	**Pull Device Enable Port M** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

3.3.2.6 Port M Polarity Select Register (PPSM)

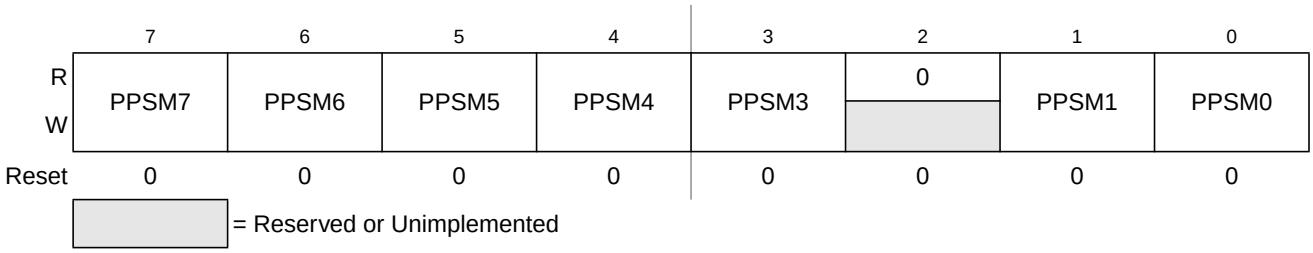


Figure 3-15. Port M Polarity Select Register (PPSM)

Read: Anytime. Write: Anytime.

The Port M Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port M Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 3-12. PPSM Field Descriptions

Field	Description
7:3, 1:0 PPSM[7:3, 1:0]	**Pull Select Port M** 0 A pull-up device is connected to the associated port M pin. 1 A pull-down device is connected to the associated port M pin.

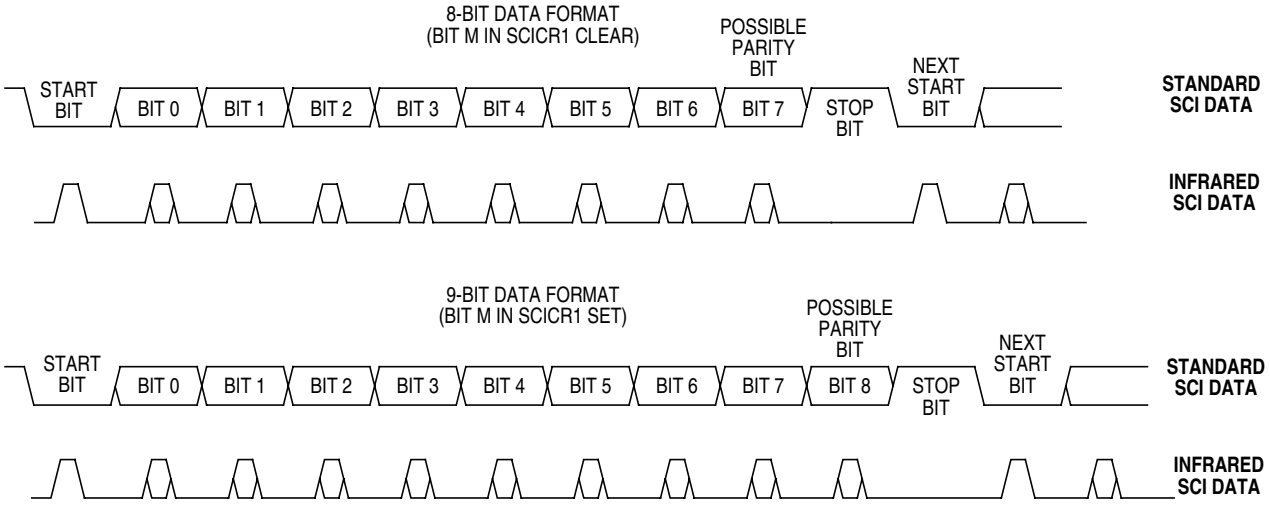


Figure 8-12. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits

Table 8-11. Example of 8-bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 8.4.5.6, “Receiver Wakeup”.

When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 8-12. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 8.4.5.6, “Receiver Wakeup”.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCIDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCIDRH/L.

8.4.4.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCICR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCICR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be. Receiving a break character has these effects on SCI registers:

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers (SCIDRH/L)
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see Section 8.3.2.4, “SCI Status Register 1 (SCISR1)” and Section 8.3.2.5, “SCI Status Register 2 (SCISR2)”).

8.4.4.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the

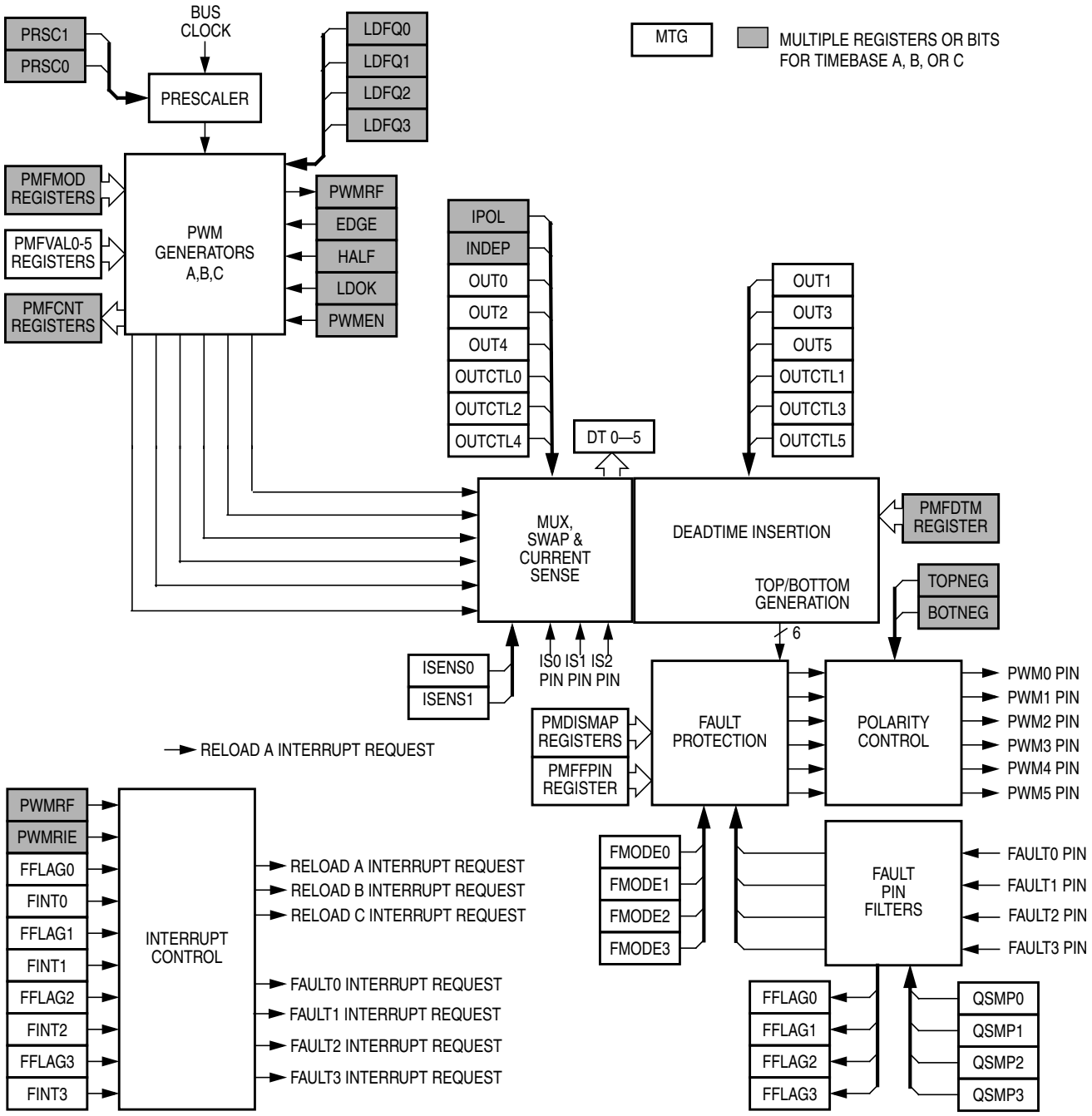


Figure 11-1. PMF Block Diagram

Setting the OUTCTLx bits do not disable the PWM generators and current status sensing circuitry. They continue to run, but no longer control the output pins. When the OUTCTLx bits are cleared, the outputs of the PWM generator become the inputs to the deadtime generators at the beginning of the next PWM cycle. Software can drive the PWM outputs even when PWM enable bit (PWMEN) is set to zero.

NOTE

Avoid an unexpected deadtime insertion by clearing the OUTx bits before setting and after clearing the OUTCTLx bits.

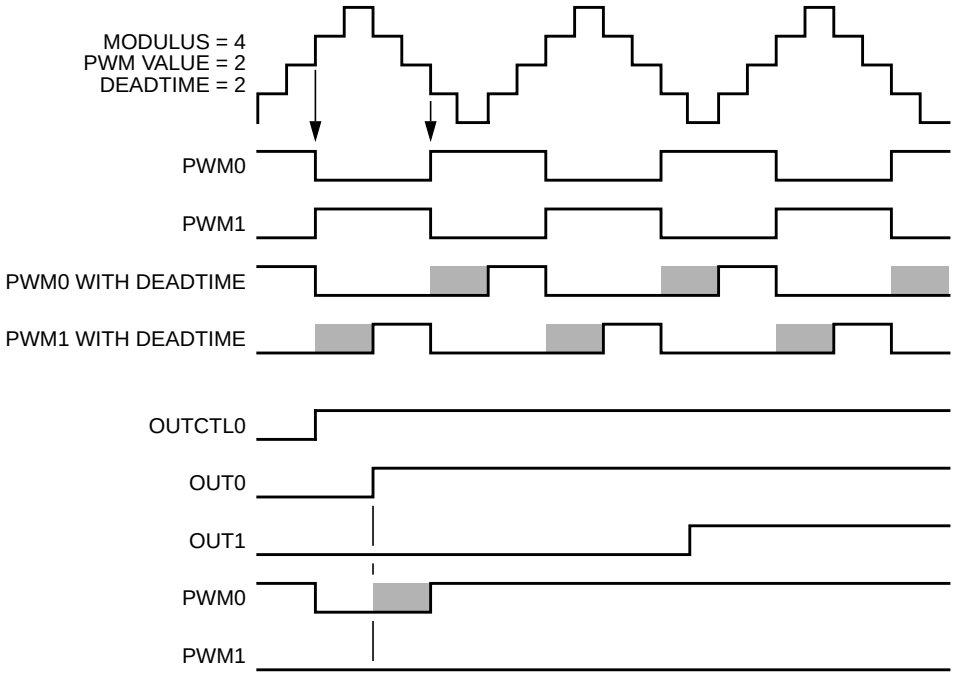


Figure 11-62. Setting OUT0 with OUTCTL Set in Complementary Mode

13.3.2.9 Timer Control Register 3 (TCTL3)

	7	6	5	4	3	2	1	0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
Reset	0	0	0	0	0	0	0	0

Figure 13-15. Timer Control Register 3 (TCTL3)

Read: Anytime

Write: Anytime.

Table 13-10. TCTL3/TCTL4 Field Descriptions

Field	Description
7:0 EDGnB EDGnA	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits.

Table 13-11. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

The minimum pulse width for the PAI input is greater than two bus clocks.

13.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

13.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

13.5 Resets

The reset state of each individual bit is listed within Section 13.3, “Memory Map and Register Definition” which details the registers and their bit fields.

The regulator is a linear series regulator with a bandgap reference in its full-performance mode and a voltage clamp in reduced-power mode. All load currents flow from input V_{DDR} to V_{SS} or V_{SSPLL}, the reference circuits are connected to V_{DDA} and V_{SSA}.

14.4.2 Full-Performance Mode

In full-performance mode, a fraction of the output voltage (V_{DD}) and the bandgap reference voltage are fed to an operational amplifier. The amplified input voltage difference controls the gate of an output driver which basically is a large NMOS transistor connected to the output.

14.4.3 Reduced-Power Mode

In reduced-power mode, the driver gate is connected to a buffered fraction of the input voltage (V_{DDR}). The operational amplifier and the bandgap are disabled to reduce power consumption.

14.4.4 LVD — Low-Voltage Detect

sub-block LVD is responsible for generating the low-voltage interrupt (LVI). LVD monitors the input voltage (V_{DDA}–V_{SSA}) and continuously updates the status flag LVDS. Interrupt flag LVIF is set whenever status flag LVDS changes its value. The LVD is available in FPM and is inactive in reduced-power mode and shutdown mode.

14.4.5 POR — Power-On Reset

This functional block monitors output V_{DD}. If V_{DD} is below V_{PORD}, signal POR is high, if it exceeds V_{PORD}, the signal goes low. The transition to low forces the CPU in the power-on sequence.

Due to its role during chip power-up this module must be active in all operating modes of VREG3V3V2.

14.4.6 LVR — Low-Voltage Reset

Block LVR monitors the primary output voltage V_{DD}. If it drops below the assertion level (V_{LVRA}) signal LVR asserts and when rising above the deassertion level (V_{LVRD}) signal LVR negates again. The LVR function is available only in full-performance mode.

14.4.7 CTRL — Regulator Control

This part contains the register block of VREG3V3V2 and further digital functionality needed to control the operating modes. CTRL also represents the interface to the digital core logic.

18.3.2.6 Port E Data Register (PORTE)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	u	u
Alternate Pin Function	NOACC	MODB or IPIPE1 or CLKTO	MODA or IPIPE0	ECLK	$\overline{\text{LSTRB}}$ or $\overline{\text{TAGLO}}$	R/$\overline{\text{W}}$	$\overline{\text{IRQ}}$	$\overline{\text{XIRQ}}$

= Unimplemented or Reserved u = Unaffected by reset

Figure 18-10. Port E Data Register (PORTE)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Port E is associated with external bus control signals and interrupt inputs. These include mode select (MODB/IPIPE1, MODA/IPIPE0), E clock, size ($\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$), read/write (R/$\overline{\text{W}}$), $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$. When not used for one of these specific functions, port E pins 7:2 can be used as general-purpose I/O and pins 1:0 can be used as general-purpose input. The port E assignment register (PEAR) selects the function of each pin and DDRE determines whether each pin is an input or output when it is configured to be general-purpose I/O. DDRE also determines the source of data for a read of PORTE.

Some of these pins have software selectable pull resistors. $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$ can only be pulled up whereas the polarity of the PE7, PE4, PE3, and PE2 pull resistors are determined by chip integration. Please refer to the device overview chapter (Signal Property Summary) to determine the polarity of these resistors. A single control bit enables the pull devices for all of these pins when they are configured as inputs.

This register is not in the on-chip map in special peripheral mode or in expanded modes when the EME bit is set. Therefore, these accesses will be echoed externally.

NOTE

It is unwise to write PORTE and DDRE as a word access. If you are changing port E pins from being inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTE before enabling as outputs.

NOTE

To ensure that you read the value present on the PORTE pins, always wait at least one cycle after writing to the DDRE register before reading from the PORTE register.

19.3.2.5 Reserved Test Register 0 (MTST0)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-7. Reserved Test Register 0 (MTST0)

Read: Anytime

Write: No effect — this register location is used for internal test purposes.

19.3.2.6 Reserved Test Register 1 (MTST1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Figure 19-8. Reserved Test Register 1 (MTST1)

Read: Anytime

Write: No effect — this register location is used for internal test purposes.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the internal logic.

VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDD1 and VDD2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE

In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.

IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.

VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.

IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 3.3V/5V I/O Pins

Those I/O pins have a nominal level of 3.3V or 5V depending on the application operating point. This group of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of all those pins is identical, however some of the functionality may be disabled.

A.1.3.2 Analog Reference

This group of pins is comprised of the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the

Table A-7. Preliminary 3.3V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	—	—	V
	T	Input High Voltage	V_{IH}	—	—	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	—	—	0.35*V_{DD5}	V
	T	Input Low Voltage	V_{IL}	V_{SS5} – 0.3	—	—	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1.0	—	1.0	µA
5	C	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA	V_{OH}	V_{DD5} – 0.4	—	—	V
6	P	Output High Voltage (pins in output mode) Full Drive I_{OH} = –4mA	V_{OH}	V_{DD5} – 0.4	—	—	V
7	C	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA	V_{OL}	—	—	0.4	V
8	P	Output Low Voltage (pins in output mode) Full Drive I_{OL} = +4.75mA	V_{OL}	—	—	0.4	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	—	—	–60	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–6	—	—	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	—	—	60	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	—	—	µA
13	D	Input Capacitance	C_{in}	—	6	—	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	–2.5 –25	— —	2.5 25	mA
15	P	Port AD Interrupt Input Pulse filtered[3]	t_{PIGN}	—	—	3	µs
16	P	Port AD Interrupt Input Pulse passed[3]	t_{PVAL}	10	—	—	µs

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C

2 Refer to Section A.1.4, “Current Injection”, for more details

3 Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.4.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

A.4.1.5 Blank Check

The time it takes to perform a blank check on the Flash is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-14. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5	—	50[1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1	—		MHz
3	D	Operating Frequency	f_{NVMOP}	150	—	200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46[2]	—	74.5[3]	µs
5	D	Flash Burst Programming consecutive word	t_{bwpgm}	20.4[2]	—	31[3]	µs
6	D	Flash Burst Programming Time for 64 Word row	t_{brpgm}	1331.2[2]	—	2027.5[3]	µs
7	P	Sector Erase Time	t_{era}	20[4]	—	26.7[3]	ms
8	P	Mass Erase Time	t_{mass}	100[4]	—	133[3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11[5]	—	65546[6]	[7] t_{cyc}

1 Restrictions for oscillator in crystal mode apply!

2 Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f bus. Refer to formulae in Sections A.3.1.1 - A.3.1.4 for guidance.

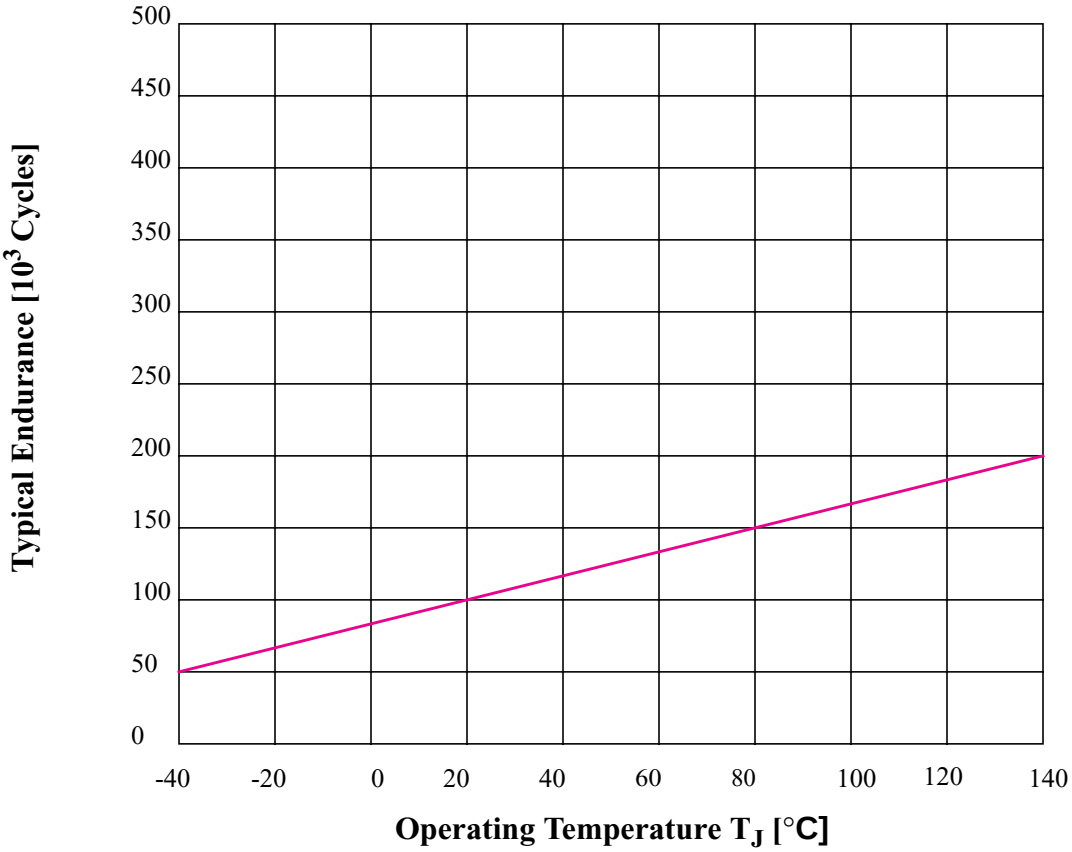
4 Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}

5 Minimum time, if first word in the array is not blank

6 Maximum time to complete check on an erased block

7 Where t_{cyc} is the system bus clock period.

Typical Endurance



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