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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12e64vfue16r

0x0180 – 0x01AF TIM2 (Timer 16 Bit 4 Channels) (Sheet 3 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x019D	TC6 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x019E	TC7 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x019F	TC7 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x01A0	PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		W								
0x01A1	PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
		W								
0x01A2	PACNT (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x01A3	PACNT (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x01A4	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01A5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01A6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01A7	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01A8	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01A9	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AA	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AD	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01AF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0200 – 0x023F PMF (Pulse width Modulator with Fault protection) (Sheet 4 of 4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0239	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023D	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0240 – 0x027F PIM (Port Interface Module) (Sheet 1 of 4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0241	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0242	DDRT	R	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0243	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0247	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0248	PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		W								
0x0249	PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		W								

also be configured as Keypad Wake-up pins (KWU) and generate interrupts causing the MCU to exit STOP or WAIT mode. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the ATD_10B16C block description chapter for information about pin configurations.

1.4.20 PM7 / SCL — Port M I/O Pin 7

PM7 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (SCL) for the IIC module (IIC). While in reset and immediately out of reset the PM7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the IIC block description chapter for information about pin configurations.

1.4.21 PM6 / SDA — Port M I/O Pin 6

PM6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (SDL) for the IIC module (IIC). While in reset and immediately out of reset the PM6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the IIC block description chapter for information about pin configurations.

1.4.22 PM5 / TXD2 — Port M I/O Pin 5

PM5 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) transmitter is enabled the PM5 pin is configured as the transmit pin TXD2 of SCI2. While in reset and immediately out of reset the PM5 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the SCI block description chapter for information about pin configurations.

1.4.23 PM4 / RXD2 — Port M I/O Pin 4

PM4 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) receiver is enabled the PM4 pin is configured as the receive pin RXD2 of SCI2. While in reset and immediately out of reset the PM4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter and the SCI block description chapter for information about pin configurations.

1.4.24 PM3 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. While in reset and immediately out of reset the PM3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 block description chapter for information about pin configurations.

1.4.25 PM1 / DAO1 — Port M I/O Pin 1

PM1 is a general purpose input or output pin. When the Digital to Analog module 1 (DAC1) is enabled the PM1 pin is configured as the analog output DA01 of DAC1. While in reset and immediately out of reset the PM1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM)

NOTE: Oscillator in Colpitts mode.

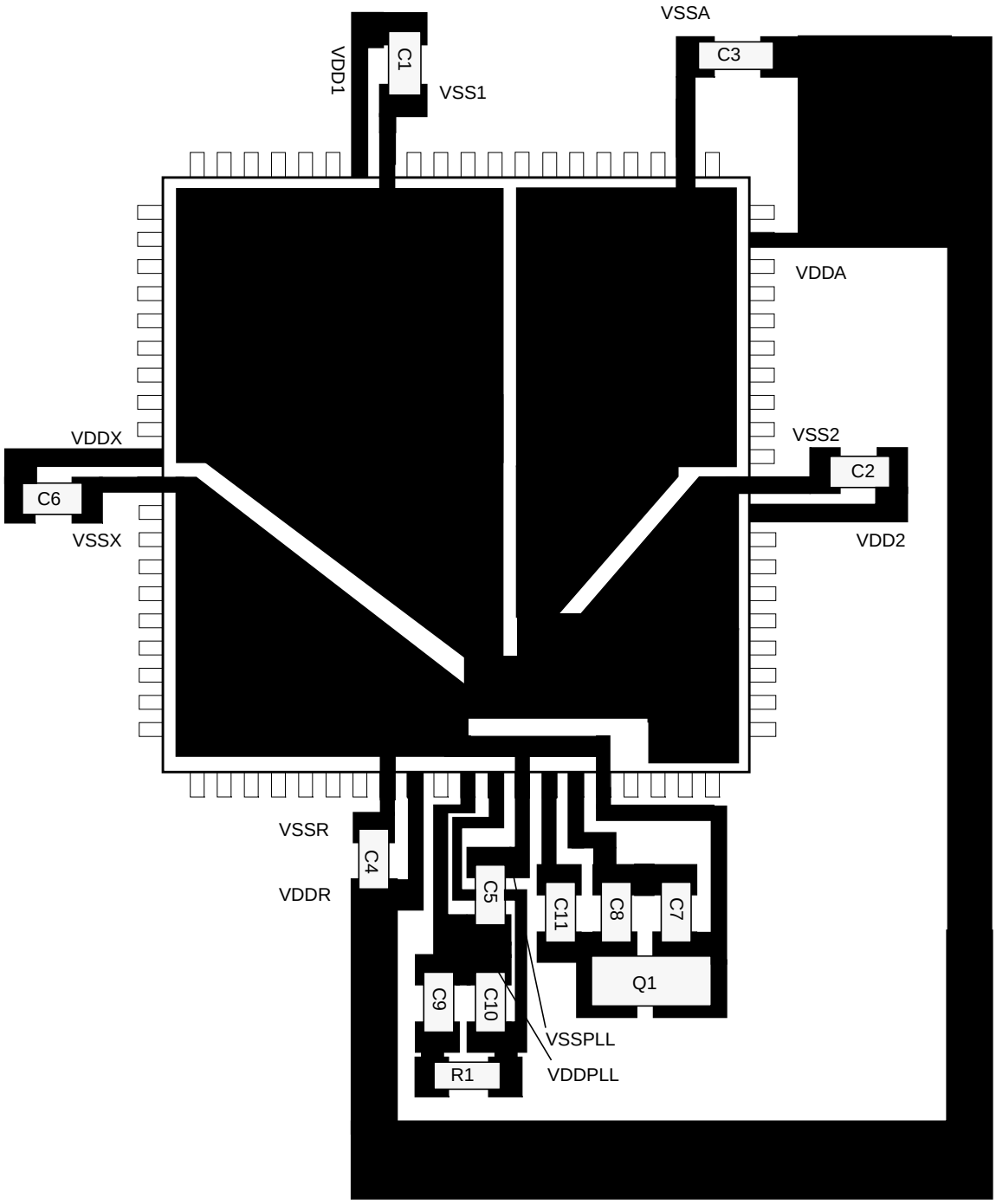

Figure 1-12. Recommended PCB Layout (80-QFP)

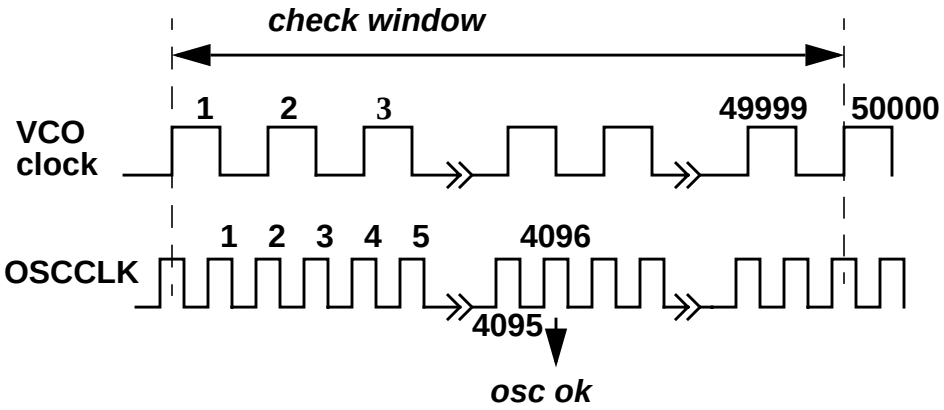

Figure 4-19. Check Window Example

The sequence for clock quality check is shown in Figure 4-20.

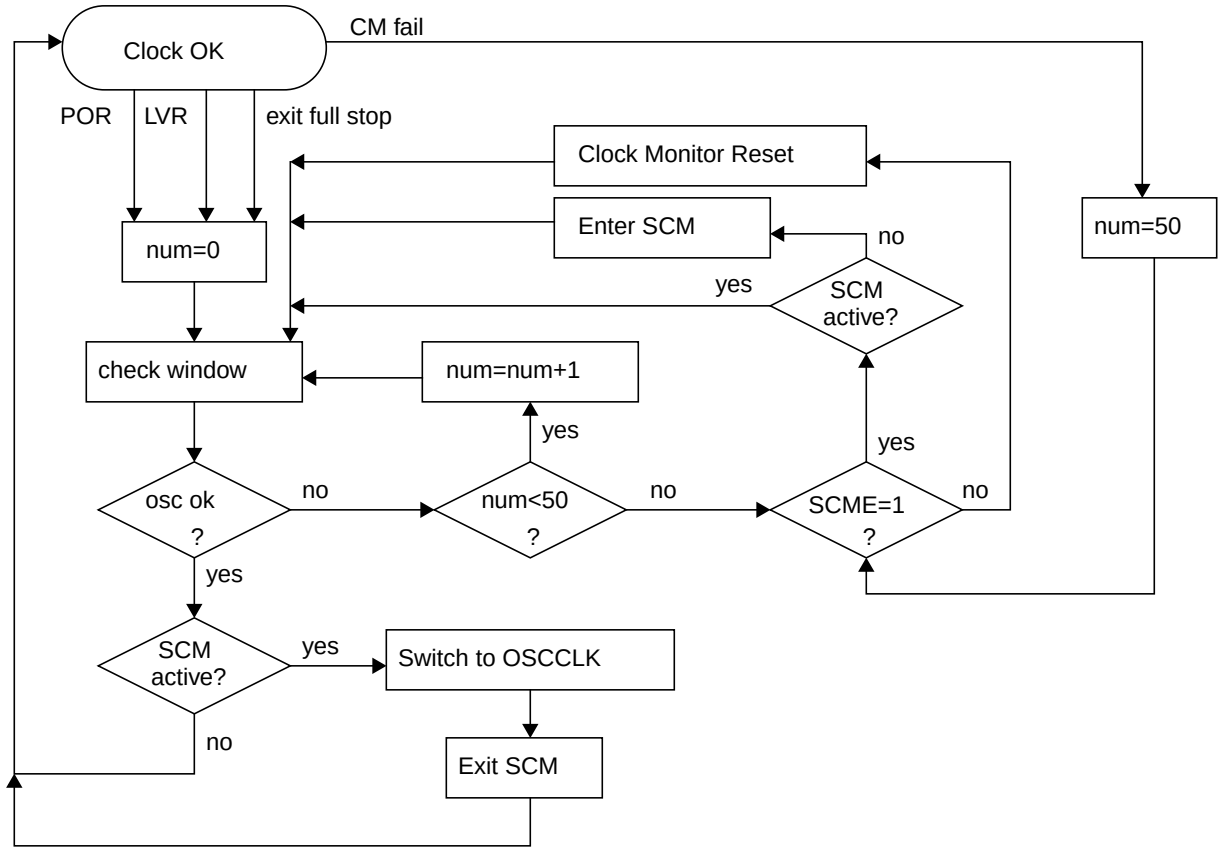

Figure 4-20. Sequence for Clock Quality Check

NOTE

Remember that in parallel to additional actions caused by self-clock mode or clock monitor reset[1] handling the clock quality checker **continues** to check the OSCCLK signal.

1. A Clock Monitor Reset will always set the SCME bit to logical'1'

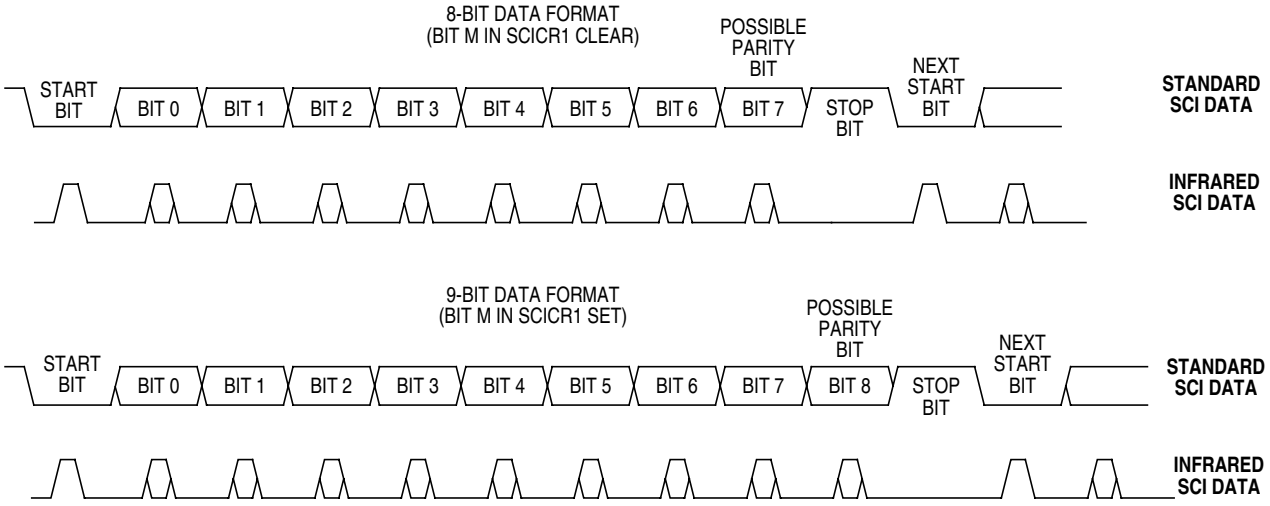

Figure 8-12. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits

Table 8-11. Example of 8-bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 8.4.5.6, “Receiver Wakeup”.

When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 8-12. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 8.4.5.6, “Receiver Wakeup”.

8.4.5.5.2 Fast Data Tolerance

Figure 8-23 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but continues to be sampled at RT8, RT9, and RT10.

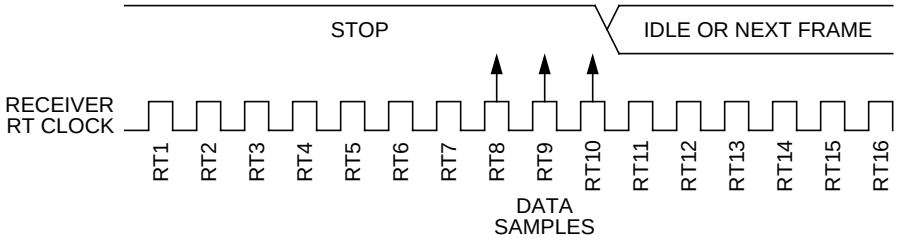

Figure 8-23. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 10 RTr cycles = 154 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 8-23, the receiver counts 154 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 154) / 160) x 100 = 3.75%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 10 RTr cycles = 170 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 8-23, the receiver counts 170 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 170) / 176) x 100 = 3.40%

8.4.5.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will continue to load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCI control register 1 (SCICR1) determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

10.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Table 10-1. IIC Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
	W								
IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
	W								
IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
	W						RSTA		
IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
	W								
IBDR	R	D7	D6	D5	D4	D3	D2	D1	D0
	W								

= Unimplemented or Reserved

10.3.2.1 IIC Address Register (IBAD)

	7	6	5	4	3	2	1	0
R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-2. IIC Bus Address Register (IBAD)

Read and write anytime

This register contains the address the IIC bus will respond to when addressed as a slave; note that it is not the address sent on the bus during the address transfer.

Table 10-2. IBAD Field Descriptions

Field	Description
7:1 ADR[7:1]	**Slave Address** — Bit 1 to bit 7 contain the specific slave address to be used by the IIC bus module.The default mode of IIC bus is slave mode for an address match on the bus.
0 Reserved	Reserved — Bit 0 of the IBAD is reserved for future compatibility. This bit will always read 0.

Table 10-6. IIC Divider and Hold Values (Sheet 5 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
A8	1280	132	632	644
A9	1536	132	760	772
AA	1792	260	888	900
AB	2048	260	1016	1028
AC	2304	388	1144	1156
AD	2560	388	1272	1284
AE	3072	516	1528	1540
AF	3840	516	1912	1924
B0	2560	260	1272	1284
B1	3072	260	1528	1540
B2	3584	516	1784	1796
B3	4096	516	2040	2052
B4	4608	772	2296	2308
B5	5120	772	2552	2564
B6	6144	1028	3064	3076
B7	7680	1028	3832	3844
B8	5120	516	2552	2564
B9	6144	516	3064	3076
BA	7168	1028	3576	3588
BB	8192	1028	4088	4100
BC	9216	1540	4600	4612
BD	10240	1540	5112	5124
BE	12288	2052	6136	6148
BF	15360	2052	7672	7684

10.3.2.3 IIC Control Register (IBCR)

	7	6	5	4	3	2	1	0
R	IBEN	IBIE	MS/SL	Tx/Rx	TXAK	0	0	IBSWAI
W						RSTA		
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-5. IIC Bus Control Register (IBCR)

Read and write anytime

11.3.2.3 PMF Configure 2 Register (PMFCFG2)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-6. PMF Configure 2 Register (PMFCFG2)

Read and write anytime.

Table 11-4. PMFCFG2 Field Descriptions

Field	Description
5–0 MSK[5:0]	**Mask PWMx**— Where x is 0, 1, 2, 3, 4, and 5. 0 PWMx is unmasked. 1 PWMx is masked and the channel is set to a value of 0 percent duty cycle. **Note:** **WARNING** When using the TOPNEG/BOTNEG bits and the MSKx bits at the same time, when in complementary mode, it is possible to have both pmf channel outputs of a channel pair set to one.

In complementary channel operation, there are three additional features:

- Deadtime insertion
- Separate top and bottom pulse width correction for distortions are caused by deadtime inserted and the motor drive characteristics
- Separate top and bottom output polarity control
- Swap functionality

11.4.5 Deadtime Generators

While in the complementary mode, each PWM pair can be used to drive top/bottom transistors, as shown in Figure 11-49. Ideally, the PWM pairs are an inversion of each other. When the top PWM channel is active, the bottom PWM channel is inactive, and vice versa.

NOTE

To avoid a short-circuit on the DC bus and endangering the transistor, there must be no overlap of conducting intervals between top and bottom transistor. But the transistor's characteristics make its switching-off time longer than switching-on time. To avoid the conducting overlap of top and bottom transistors, deadtime needs to be inserted in the switching period.

Deadtime generators automatically insert software-selectable activation delays into each pair of PWM outputs. The deadtime register (PMFDTMx) specifies the number of PWM clock cycles to use for deadtime delay. Every time the deadtime generator inputs changes state, deadtime is inserted. Deadtime forces both PWM outputs in the pair to the inactive state.

A method of correcting this, adding to or subtracting from the PWM value used, is discussed next.

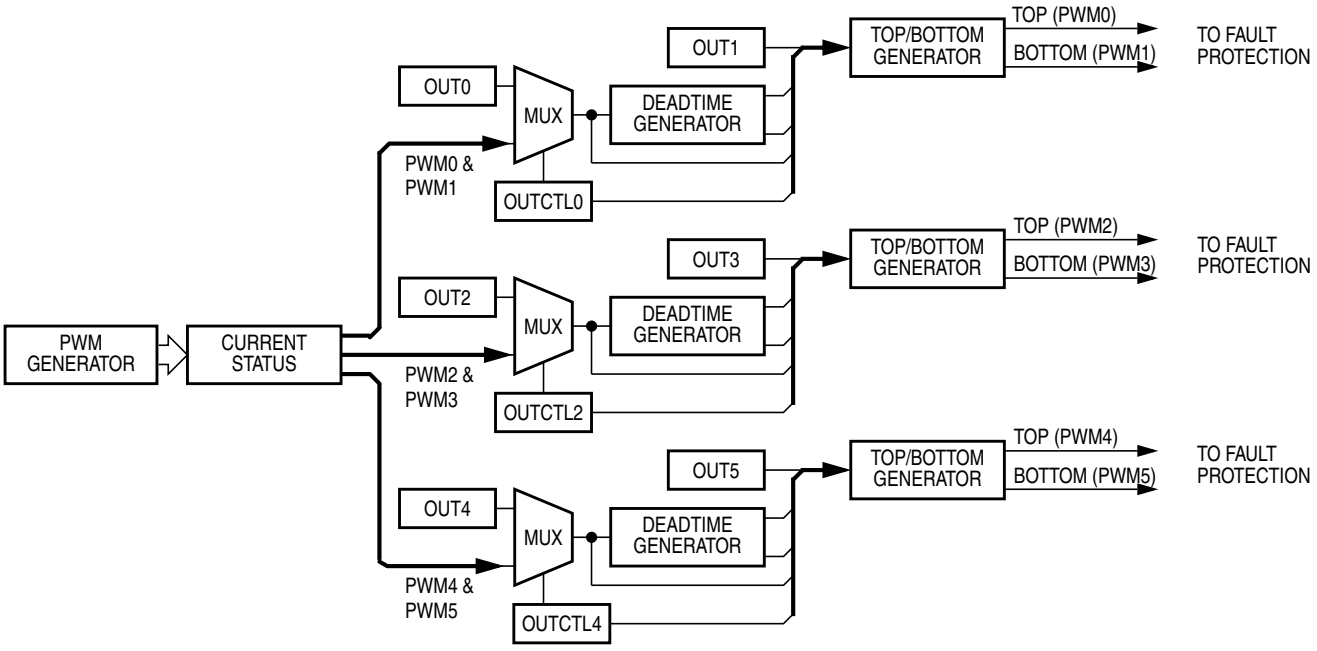

Figure 11-49. Deadtime Generators

Setting the OUTCTLx bits do not disable the PWM generators and current status sensing circuitry. They continue to run, but no longer control the output pins. When the OUTCTLx bits are cleared, the outputs of the PWM generator become the inputs to the deadtime generators at the beginning of the next PWM cycle. Software can drive the PWM outputs even when PWM enable bit (PWMEN) is set to zero.

NOTE

Avoid an unexpected deadtime insertion by clearing the OUTx bits before setting and after clearing the OUTCTLx bits.

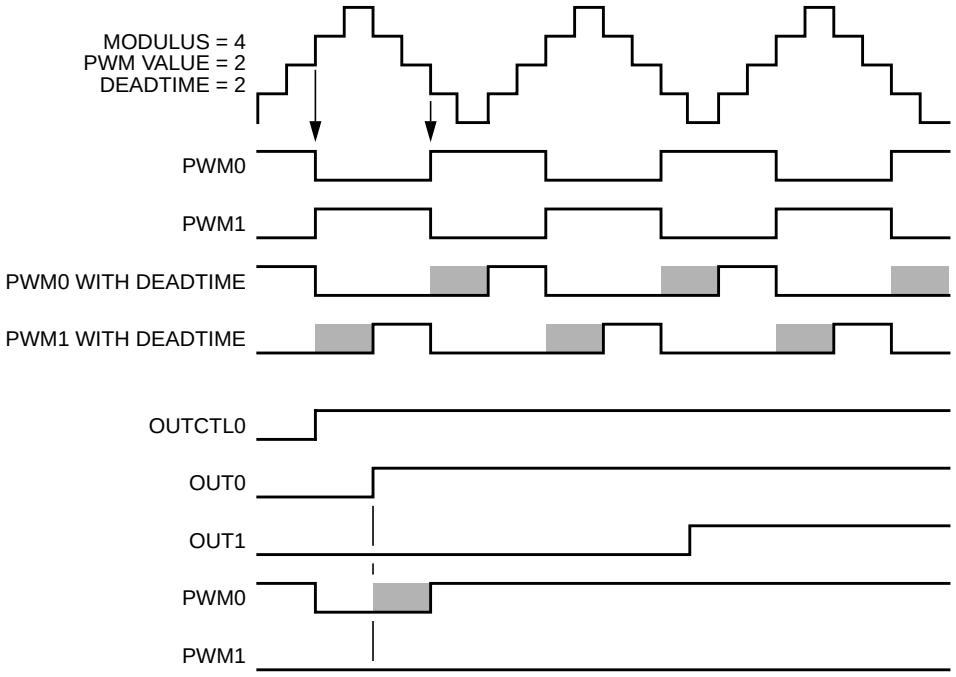

Figure 11-62. Setting OUT0 with OUTCTL Set in Complementary Mode

13.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

13.3.1 Module Memory Map

The memory map for the TIM16B4CV1 module is given below in Table 13-1. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B4CV1 module and the address offset for each register.

Table 13-1. TIM16B4CV1 Memory Map

Address Offset	Use	Access
0x0000	Timer Input Capture/Output Compare Select (TIOS)	R/W
0x0001	Timer Compare Force Register (CFORC)	R/W[1]
0x0002	Output Compare 7 Mask Register (OC7M)	R/W
0x0003	Output Compare 7 Data Register (OC7D)	R/W
0x0004	Timer Count Register (TCNT(hi))	R/W[2]
0x0005	Timer Count Register (TCNT(lo))	R/W[2]
0x0006	Timer System Control Register1 (TSCR1)	R/W
0x0007	Timer Toggle Overflow Register (TTOV)	R/W
0x0008	Timer Control Register1 (TCTL1)	R/W
0x0009	Reserved	—[3]
0x000A	Timer Control Register3 (TCTL3)	R/W
0x000B	Reserved	—[3]
0x000C	Timer Interrupt Enable Register (TIE)	R/W
0x000D	Timer System Control Register2 (TSCR2)	R/W
0x000E	Main Timer Interrupt Flag1 (TFLG1)	R/W
0x000F	Main Timer Interrupt Flag2 (TFLG2)	R/W
0x0010 - 0x0017	Reserved	—[3]
0x0018	Timer Input Capture/Output Compare Register4 (TC4(hi))	R/W[4]
0x0019	Timer Input Capture/Output Compare Register 4 (TC4(lo))	R/W[4]
0x001A	Timer Input Capture/Output Compare Register 5 (TC5(hi))	R/W[4]
0x001B	Timer Input Capture/Output Compare Register 5 (TC5(lo))	R/W[4]
0x001C	Timer Input Capture/Output Compare Register 6 (TC6(hi))	R/W[4]
0x001D	Timer Input Capture/Output Compare Register 6 (TC6(lo))	R/W[4]
0x001E	Timer Input Capture/Output Compare Register 7 (TC7(hi))	R/W[4]
0x001F	Timer Input Capture/Output Compare Register 7 (TC7(lo))	R/W[4]
0x0020	16-Bit Pulse Accumulator Control Register (PACTL)	R/W
0x0021	Pulse Accumulator Flag Register (PAFLG)	R/W
0x0022	Pulse Accumulator Count Register (PACNT(hi))	R/W
0x0023	Pulse Accumulator Count Register (PACNT(lo))	R/W
0x0024 – 0x002C	Reserved	—[3]
0x002D	Timer Test Register (TIMTST)	R/W[2]
0x002E – 0x002F	Reserved	—[3]

1 Always read 0x0000.

2 Only writable in special modes (test_mode = 1).
3 Write has no effect; return 0 on read
4 Write to these registers have no meaning or effect during input capture.

13.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x0002 OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
	W								
0x0003 OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
	W								
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR2	R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
	W								
0x0007 TTOV	R	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
	W								
0x0009 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000A TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
	W								

= Unimplemented or Reserved

Figure 13-5. TIM16B4CV1 Register Summary

The BDM hardware commands are listed in Table 15-5.

Table 15-5. Hardware Commands

Command	Opcode (hex)	Data	Description
BACKGROUND	90	None	Enter background mode if firmware is enabled. If enabled, an ACK will be issued when the part enters active background mode.
ACK_ENABLE	D5	None	Enable handshake. Issues an ACK pulse after the command is executed.
ACK_DISABLE	D6	None	Disable handshake. This command does not issue an ACK pulse.
READ_BD_BYTE	E4	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
READ_BD_WORD	EC	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Must be aligned access.
READ_BYTE	E0	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
READ_WORD	E8	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Must be aligned access.
WRITE_BD_BYTE	C4	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
WRITE_BD_WORD	CC	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Must be aligned access.
WRITE_BYTE	C0	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
WRITE_WORD	C8	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Must be aligned access.

NOTE:
If enabled, ACK will occur when data is ready for transmission for all BDM READ commands and will occur after the write is complete for all BDM WRITE commands.

The READ_BD and WRITE_BD commands allow access to the BDM register locations. These locations are not normally in the system memory map but share addresses with the application in memory. To distinguish between physical memory locations that share the same address, BDM memory resources are enabled just for the READ_BD and WRITE_BD access cycle. This allows the BDM to access BDM locations unobtrusively, even if the addresses conflict with the application memory map.

15.4.4 Standard BDM Firmware Commands

Firmware commands are used to access and manipulate CPU resources. The system must be in active BDM to execute standard BDM firmware commands, see Section 15.4.2, “Enabling and Activating BDM.” Normal instruction execution is suspended while the CPU executes the firmware located in the standard BDM firmware lookup table. The hardware command BACKGROUND is the usual way to activate BDM.

As the system enters active BDM, the standard BDM firmware lookup table and BDM registers become visible in the on-chip memory map at 0xFF00–0xFFFF, and the CPU begins executing the standard BDM

Chapter 16
Debug Module (DBGV1)

16.1 Introduction

This section describes the functionality of the debug (DBG) sub-block of the HCS12 core platform.

The DBG module is designed to be fully compatible with the existing BKP_HCS12_A module (BKP mode) and furthermore provides an on-chip trace buffer with flexible triggering capability (DBG mode). The DBG module provides for non-intrusive debug of application software. The DBG module is optimized for the HCS12 16-bit architecture.

16.1.1 Features

The DBG module in BKP mode includes these distinctive features:

- Full or dual breakpoint mode
  - Compare on address and data (full)
  - Compare on either of two addresses (dual)
- BDM or SWI breakpoint
  - Enter BDM on breakpoint (BDM)
  - Execute SWI on breakpoint (SWI)
- Tagged or forced breakpoint
  - Break just before a specific instruction will begin execution (TAG)
  - Break on the first instruction boundary after a match occurs (Force)
- Single, range, or page address compares
  - Compare on address (single)
  - Compare on address 256 byte (range)
  - Compare on any 16K page (page)
- At forced breakpoints compare address on read or write
- High and/or low byte data compares
- Comparator C can provide an additional tag or force breakpoint (enhancement for BKP mode)

16.3.2.2 Debug Status and Control Register (DBGSC)

	7	6	5	4	3	2	1	0
R	AF	BF	CF	0	TRG			
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-5. Debug Status and Control Register (DBGSC)

Table 16-5. DBGSC Field Descriptions

Field	Description
7 AF	**Trigger A Match Flag** — The AF bit indicates if trigger A match condition was met since arming. This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger A did not match 1 Trigger A match
6 BF	**Trigger B Match Flag** — The BF bit indicates if trigger B match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger B did not match 1 Trigger B match
5 CF	**Comparator C Match Flag** — The CF bit indicates if comparator C match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Comparator C did not match 1 Comparator C match
3:0 TRG	**Trigger Mode Bits** — The TRG bits select the trigger mode of the DBG module as shown Table 16-6. See Section 16.4.2.5, “Trigger Modes,” for more detail.

Table 16-6. Trigger Mode Encoding

TRG Value	Meaning
0000	A only
0001	A or B
0010	A then B
0011	Event only B
0100	A then event only B
0101	A and B (full mode)
0110	A and Not B (full mode)
0111	Inside range
1000	Outside range
1001 ↓ 1111	Reserved (Defaults to A only)

control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

18.4.3.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

18.4.3.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

18.4.3.3.1 Peripheral Mode

This mode is intended for factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

18.4.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or emulation narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E, R/$\overline{W}$, and $\overline{LSTRB}$ are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{W}$ will remain high, data will maintain its previous state, and address and $\overline{LSTRB}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

injection current may flow out of VDD5 and could result in external power supply going out of regulation. Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1. Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	–0.3	6.5	V
2	Internal Logic Supply Voltage[1]	V_{DD}	–0.3	3.0	V
3	PLL Supply Voltage [1]	V_{DDPLL}	–0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	–0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	–0.3	6.5	V
7	Analog Reference	V_{RH}, V_{RL}	–0.3	6.5	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	3.0	V
9	TEST input	V_{TEST}	–0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [2]	I_D	–25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[3]	I_{DL}	–25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST[4]	I_{DT}	–0.25	0	mA
13	Operating Temperature Range (packaged)	T_A	– 40	125	°C
14	Operating Temperature Range (junction)	T_J	– 40	140	°C
15	Storage Temperature Range	T_{stg}	– 65	155	°C

1 The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.

2 All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.

3 These pins are internally clamped to V_{SSPLL} and V_{DDPLL}

4 This pin is clamped low to V_{SSR}, but not clamped high. This pin must be tied low in applications.