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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SSU
Peripherals	POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71364ad80fpv

Related Manuals: The latest versions of all related manuals are available from our web site.
Please ensure you have the latest versions of all documents you require.
http://www.renesas.com/

SH7131, SH7132, SH7136, and SH7137 Group manuals:

Document Title	Document No.
SH7137 Group Hardware Manual	This manual
SH-1/SH-2/SH-DSP Software Manual	REJ09B0171

User's manuals for development tools:

Document Title	Document No.
SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package V.9.00 User's Manual	REJ10B0152
SuperH™ RISC engine High-performance Embedded Workshop 3 User's Manual	REJ10B0025
SuperH RISC engine High-performance Embedded Workshop 3 Tutorial	REJ10B0023

Application note:

Document Title	Document No.
SuperH RISC engine C/C++ Compiler Package Application Note	REJ05B0463

7.3.8 Break Data Register B (BDRB)

BDRB is a 32-bit readable/writable register. The control bits CDB1 and CDB0 in BBRB select one of the two data buses for break condition B.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BDB31	BDB30	BDB29	BDB28	BDB27	BDB26	BDB25	BDB24	BDB23	BDB22	BDB21	BDB20	BDB19	BDB18	BDB17	BDB16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BDB15	BDB14	BDB13	BDB12	BDB11	BDB10	BDB9	BDB8	BDB7	BDB6	BDB5	BDB4	BDB3	BDB2	BDB1	BDB0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BDB31 to BDB0	All 0	R/W	Break Data Bit B Stores data which specifies a break condition in channel B. If the I bus is selected in BBRB, the break data on IDB is set in BDB31 to BDB0. If the L bus is selected in BBRB, the break data on LDB is set in BDB31 to BDB0.

Notes: 1. Specify an operand size when including the value of the data bus in the break condition.
2. When the byte size is selected as a break condition, the same byte data must be set in bits 15 to 8 and 7 to 0 in BDRB as the break data.

9.4.3 CSn Space Wait Control Register (CSnWCR) (n = 0 and 1)

CSnWCR specifies various wait cycles for memory accesses. Specify CSnWCR before accessing the target area. CSnWCR should be modified only after CSnBCR setting is completed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	WW[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[1:0]		WR[3:0]				WM	-	-	-	-	HW[1:0]	
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	WW[2:0]	000	R/W	Number of Wait Cycles in Write Access Specify the number of cycles required for write access. 000: The same cycles as WR3 to WR0 settings (read access wait) 001: 0 cycles 010: 1 cycle 011: 2 cycles 100: 3 cycles 101: 4 cycles 110: 5 cycles 111: 6 cycles
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

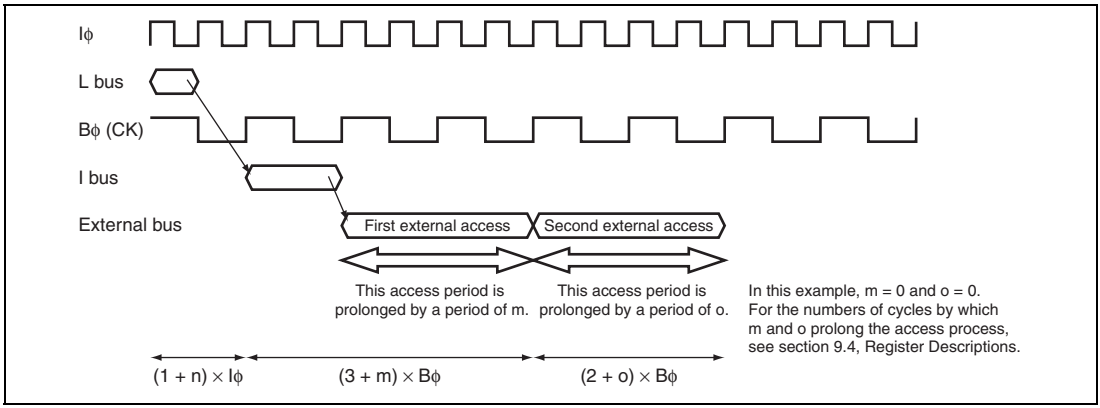


Figure 9.13 Timing of Write Access to Word Data in External Memory When Iϕ:Bϕ = 2:1 and External Bus Width is 8 Bits

Figure 9.14 shows an example of the timing of read access when the external bus width is greater than or equal to the data width and Iϕ:Bϕ = 4:1. Transfer from the L bus to the external bus is performed in the same way as for write access. In the case of reading, however, values output onto the external bus must be transferred to the CPU. Transfers from the external bus to the I bus and from the I bus to the L bus are again performed in synchronization with rising edges of the respective bus clocks. In the actual operation, transfer from the external bus to the L bus takes one ϕ period. In the case shown in the figure, where n = 2 and m = 0, access takes 3 × Iϕ + 3 × Bϕ + 1 × Iϕ.

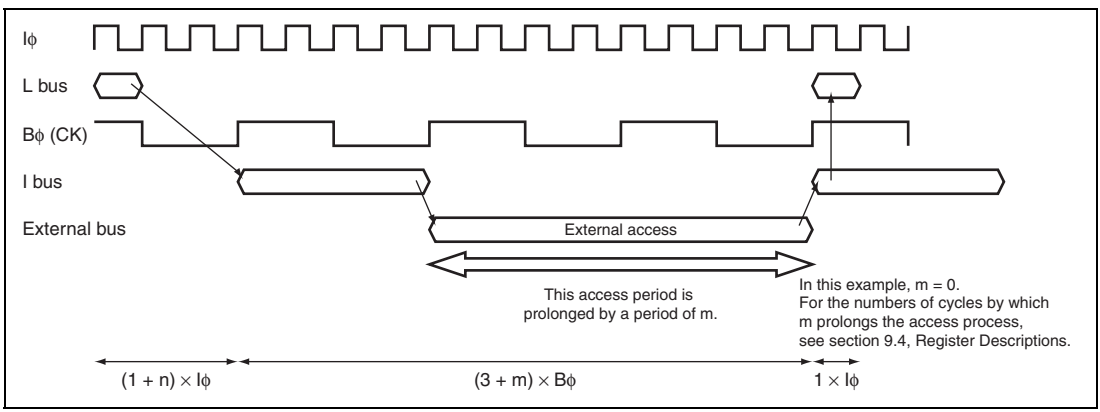
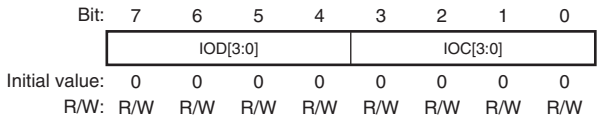


Figure 9.14 Timing of Read Access with Condition Iϕ:Bϕ = 4:1 and External Bus Width ≥ Data Width

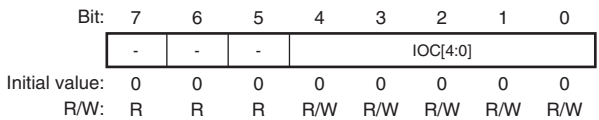
For access by the DTC, the access cycles are obtained by subtracting the cycles of Iϕ required for L-bus access from the access cycles required for access by the CPU.

- TIORL_0, TIORL_3, TIORL_4



Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IOD[3:0]	0000	R/W	I/O Control D0 to D3 Specify the function of TGRD. See the following tables. TIORL_0: Table 10.13 TIORL_3: Table 10.17 TIORL_4: Table 10.19
3 to 0	IOC[3:0]	0000	R/W	I/O Control C0 to C3 Specify the function of TGRC. See the following tables. TIORL_0: Table 10.21 TIORL_3: Table 10.25 TIORL_4: Table 10.27

- TIORU_5, TIORV_5, TIORW_5



Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	IOC[4:0]	00000	R/W	I/O Control C0 to C4 Specify the function of TGRU_5, TGRV_5, and TGRW_5. For details, see table 10.28.

Table 10.22 TIOR_1 (Channel 1)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_1 Function**	**TIOC1A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of channel 0/TGRA_0 compare match/input capture

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

10.6.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figures 10.109 and 10.110 show the timing for setting of the TGF flag in TSR on compare match, and TGI interrupt request signal timing.

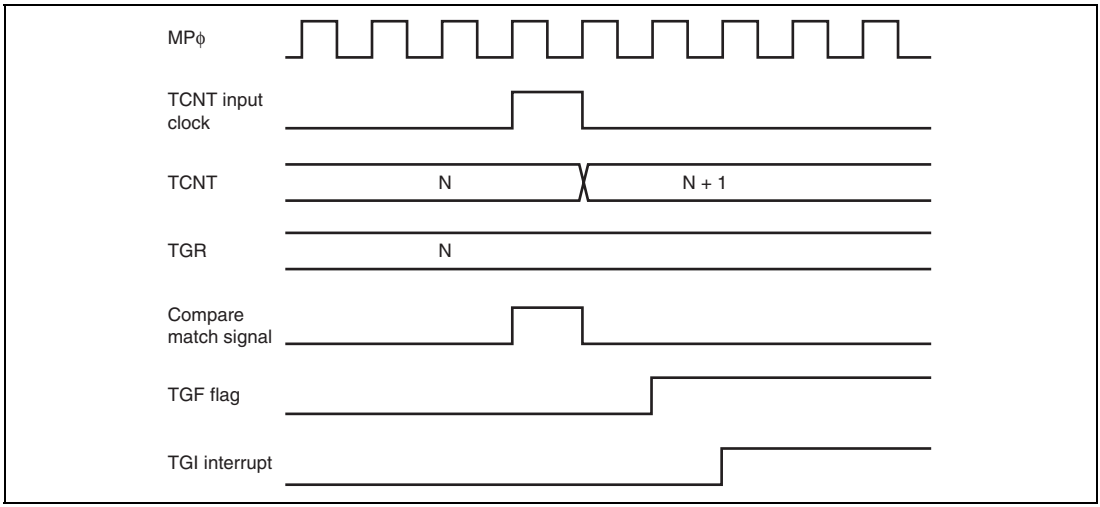


Figure 10.109 TGI Interrupt Timing (Compare Match) (Channels 0 to 4)

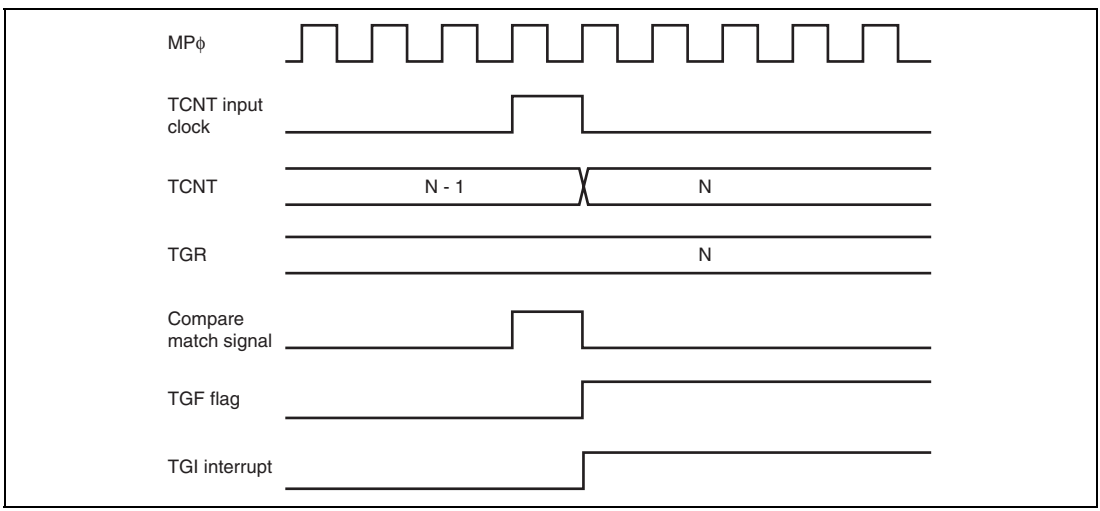


Figure 10.110 TGI Interrupt Timing (Compare Match) (Channel 5)

Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Reset-Synchronized PWM Mode: Figure 10.149 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

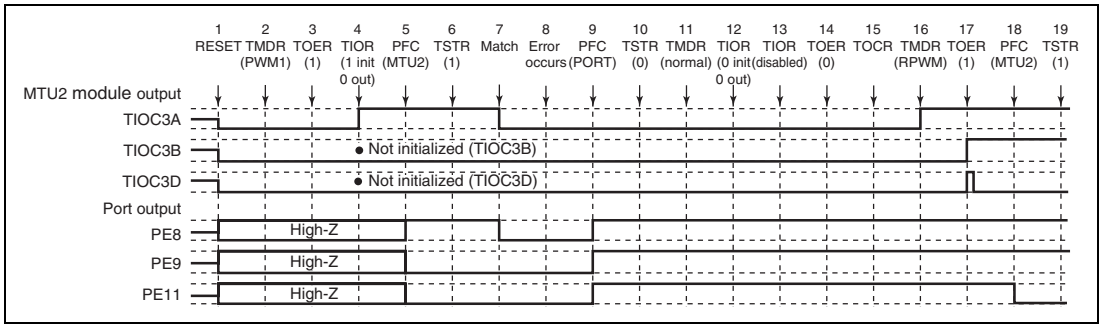


Figure 10.149 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

1 to 14 are the same as in figure 10.148.

15. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
16. Set reset-synchronized PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

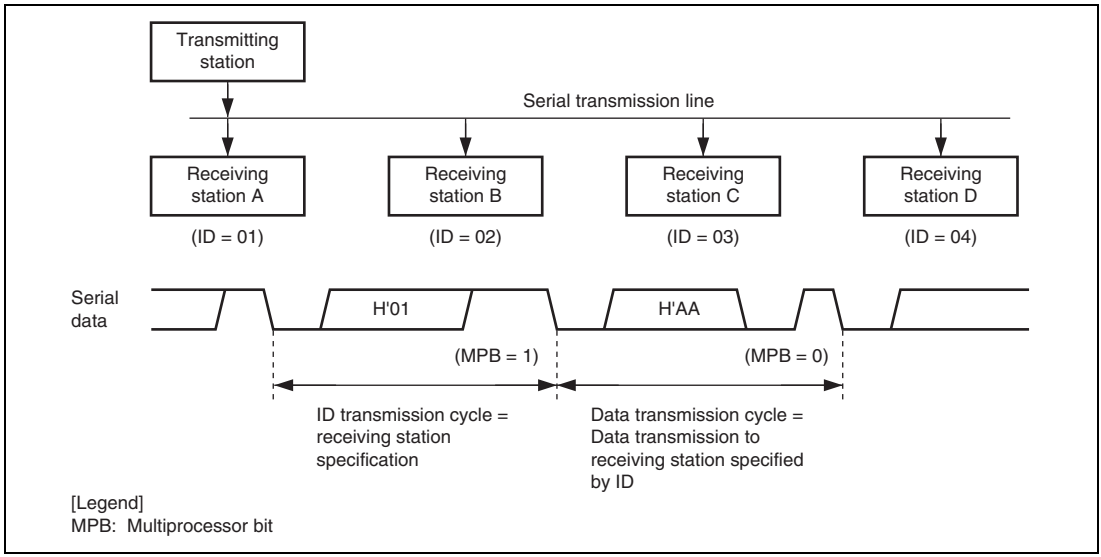


Figure 14.17 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

14.7 Usage Notes

14.7.1 SCTDR Writing and TDRE Flag

The TDRE flag in the serial status register (SCSSR) is a status flag indicating transferring of transmit data from SCTDR into SCTSR. The SCI sets the TDRE flag to 1 when it transfers data from SCTDR to SCTSR.

Data can be written to SCTDR regardless of the TDRE bit status.

If new data is written in SCTDR when TDRE is 0, however, the old data stored in SCTDR will be lost because the data has not yet been transferred to SCTSR. Before writing transmit data to SCTDR, be sure to check that the TDRE flag is set to 1.

14.7.2 Multiple Receive Error Occurrence

If multiple receive errors occur at the same time, the status flags in SCSSR are set as shown in table 14.18. When an overrun error occurs, data is not transferred from the receive shift register (SCRSR) to the receive data register (SCRDR) and the received data will be lost.

Table 14.18 SCSSR Status Flag Values and Transfer of Received Data

	SCSSR Status Flags				Receive Data Transfer from SCRSR to SCRDR
Receive Errors Generated	**RDRF**	**ORER**	**FER**	**PER**	
Overrun error	1	1	0	0	Not transferred
Framing error	0	0	1	0	Transferred
Parity error	0	0	0	1	Transferred
Overrun error + framing error	1	1	1	0	Not transferred
Overrun error + parity error	1	1	0	1	Not transferred
Framing error + parity error	0	0	1	1	Transferred
Overrun error + framing error + parity error	1	1	1	1	Not transferred

15.3.5 SS Status Register (SSSR)

SSSR is a status flag register for interrupts.

Bit:	7	6	5	4	3	2	1	0
	-	ORER	-	-	TEND	TDRE	RDRF	CE
Initial value:	0	0	0	0	0	1	0	0
R/W:	R	R/W	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	ORER	0	R/W	Overrun Error If the next data is received while RDRF = 1, an overrun error occurs, indicating abnormal termination. SSRDR stores 1-frame receive data before an overrun error occurs and loses data to be received later. While ORER = 1, consecutive serial reception cannot be continued. Serial transmission cannot be continued, either. [Setting condition] • When one byte of the next reception is completed with RDRF = 1 [Clearing condition] • When writing 0 after reading ORER = 1
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Section 17 A/D Converter (ADC)

This LSI includes a successive approximation type 12-bit A/D converter.

17.1 Features

- 12-bit resolution
- Input channels

  12 channels in SH7131/ SH7136 (two independent A/D conversion modules)

  16 channels in SH7132/SH7137 (two independent A/D conversion modules)
- Fast A/D conversion

  When operating at Pϕ = 40 MHz, conversion time is 1.25 μs per channel (A/D clock = 40 MHz and conversion done in 50 states)
- Two operating modes
  - Single-cycle scan mode: Continuous A/D conversion on one to eight channels
  - Continuous scan mode: Repetitive A/D conversion on one to eight channels
- 12-bit A/D data registers

  The SH7131 and SH7136 have four registers for A/D_0 and eight registers for A/D_1, which makes a total of twelve 16-bit A/D data registers (ADDR). The SH7132 and SH7137 have eight registers for both A/D_0 and A/D_1, which makes a total of sixteen 16-bit A/D data registers (ADDR). A/D conversion results are stored in A/D data registers (ADDR) that correspond to the input channels.
- Sample-and-hold function

  A sample-and-hold circuit is built into the A/D converter of this LSI, simplifying the configuration of the external analog input circuitry. Multiple channels can be sampled simultaneously because sample-and-hold circuits can be dedicated for channels 0 to 2 and 8 to 10.
  - Group A (GrA): Analog input pins selected from channels 0, 1, and 2 can be simultaneously sampled.
  - Group B (GrB): Analog input pins selected from channels 8, 9, and 10 can be simultaneously sampled.
- Three methods for starting conversion

  Software: Setting of the ADST bit in ADCR

  Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN from the MTU2
  TRGAN, TRG4AN, and TRG4BN from the MTU2S

  External trigger: $\overline{\text{ADTRG}}$ (LSI pin)

	Pin Name			
	On-Chip ROM Enabled (MCU Mode 2)		Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	Functions Selectable by PFC	Initial Function	Functions Selectable by PFC
58	PA9	PA9/$\overline{\text{WAIT}}$/TCLKD/$\overline{\text{POE8}}$/TXD2	PA9	PA9/TCLKD/$\overline{\text{POE8}}$/TXD2
56	PA10	PA10/A6/RXD0	PA10	PA10/RXD0
55	PA11	PA11/A7/TXD0/$\overline{\text{ADTRG}}$	PA11	PA11/TXD0/$\overline{\text{ADTRG}}$
54	PA12	PA12/A8/SCK0/$\overline{\text{SCS}}$	PA12	PA12/SCK0/$\overline{\text{SCS}}$
53	PA13	PA13/A9/SCK1/SSCK	PA13	PA13/SCK1/SSCK
52	PA14	PA14/A10/RXD1/SSI	PA14	PA14/RXD1/SSI
51	CK	PA15/CK/TXD1/SSO	PA15	PA15/TXD1/SSO
49	PB0	PB0/$\overline{\text{BACK}}$/TIC5WS	PB0	PB0//TIC5WS
47	PB1	PB1/$\overline{\text{BREQ}}$/TIC5W	PB1	PB1//TIC5W
46	PB2	PB2/A16/IRQ0/$\overline{\text{POE0}}$/TIC5VS/SCL	PB2	PB2/IRQ0/$\overline{\text{POE0}}$/TIC5VS/SCL
45	PB3	PB3/A17/IRQ1/$\overline{\text{POE1}}$/TIC5V/SDA	PB3	PB3/IRQ1/$\overline{\text{POE1}}$/TIC5V/SDA
44	PB4	PB4/A18/IRQ2/$\overline{\text{POE4}}$/TIC5US	PB4	PB4/IRQ2/$\overline{\text{POE4}}$/TIC5US
43	PB5	PB5/A19/IRQ3/$\overline{\text{POE5}}$/TIC5U	PB5	PB5/IRQ3/$\overline{\text{POE5}}$/TIC5U
42	PB6	PB6/$\overline{\text{WAIT}}$/CTx0	PB6	PB6/CTx0
41	PB7	PB7/$\overline{\text{CS1}}$/CRx0	PB7	PB7/CRx0
40	PD0	PD0/D0/RXD0	PD0	PD0/RXD0
38	PD1	PD1/D1/TXD0	PD1	PD1/TXD0
37	PD2	PD2/D2/SCK0	PD2	PD2/SCK0
35	PD3	PD3/D3/RXD1	PD3	PD3/RXD1
34	PD4	PD4/D4/TXD1	PD4	PD4/TXD1
33	PD5	PD5/D5/SCK1	PD5	PD5/SCK1
32	PD6	PD6/D6/RXD2	PD6	PD6/RXD2
31	PD7	PD7/D7/TXD2/$\overline{\text{SCS}}$	PD7	PD7/TXD2/$\overline{\text{SCS}}$
30	PD8	PD8/SCK2/SSCK	PD8	PD8/SCK2/SSCK
29	PD9	PD9/SSI	PD9	PD9/SSI
28	PD10	PD10/SSO	PD10	PD10/SSO

- Port A Control Register L1 (PACRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PA3 MD2	PA3 MD1	PA3 MD0	-	PA2 MD2	PA2 MD1	PA2 MD0	-	PA1 MD2	PA1 MD1	PA1 MD0	-	PA0 MD2	PA0 MD1	PA0 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PA3MD2	0	R/W	PA3 Mode
13	PA3MD1	0	R/W	Select the function of the PA3/IRQ1/RXD1 pin.
12	PA3MD0	0	R/W	000: PA3 I/O (port) 001: RXD1 input (SCI) 111: IRQ1 input (INTC) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PA2MD2	0	R/W	PA2 Mode
9	PA2MD1	0	R/W	Select the function of the PA2/IRQ0/$\overline{\text{POE2}}$/SCK0 pin.
8	PA2MD0	0	R/W	000: PA2 I/O (port) 001: SCK0 I/O (SCI) 011: IRQ0 input (INTC) 111: $\overline{\text{POE2}}$ input (POE) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PA1MD2	0	R/W	PA1 Mode
5	PA1MD1	0	R/W	Select the function of the PA1/$\overline{\text{POE1}}$/TXD0 pin.
4	PA1MD0	0	R/W	000: PA1 I/O (port) 001: TXD0 output (SCI) 111: $\overline{\text{POE1}}$ input (POE) Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	PB7PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
6	PB6PR	Pin state	R	
5	PB5PR	Pin state	R	
4	PB4PR	Pin state	R	
3	PB3PR	Pin state	R	
2	PB2PR	Pin state	R	
1	PB1PR	Pin state	R	
0	PB0PR	Pin state	R	

5. Note on programming the product having a 128-Kbyte user MAT

   If an attempt is made to program the product having a 128-Kbyte user MAT with more than 128 Kbytes, data programmed after the first 128 Kbytes are not guaranteed.

6. Compatibility with programming/erasing program of conventional F-ZTAT SH microcomputer

   A programming/erasing program for flash memory used in the conventional F-ZTAT SH microcomputer which does not support download of the on-chip program by a SCO transfer request cannot run in this LSI.
   Be sure to download the on-chip program to execute programming/erasing of flash memory in this LSI.

7. Monitoring runaway by WDT

   Unlike the conventional F-ZTAT SH microcomputer, no countermeasures are available for a runaway by WDT during programming/erasing by the downloaded on-chip program.
   Prepare countermeasures (e.g. use of the user branch routine and periodic timer interrupts) for WDT while taking the programming/erasing time into consideration as required.

- Command Error

Command errors are generated by undefined commands, commands sent in an incorrect order, and the inability to accept a command. For example, sending the clock-mode selection command before device selection or an inquiry command after the transition-to-programming/erasure state command generates a command error.

Error response	H'80	H'xx

— Error response H'80 (1 byte): Command error
— Command H'xx (1 byte): Received command

- Order of Commands

In the inquiry-and-selection state, commands should be sent in the following order.

1. Send the inquiry on supported devices command (H'20) to get the list of supported devices.
2. Select a device from the returned device information, and send the device selection command (H'10) to select that device.
3. Send the inquiry on clock mode command (H'21) to get the available clock modes.
4. Select a clock mode from among the returned clock modes, and send the clock-mode selection command (H'11).
5. After selection of the device and clock mode, send the commands to inquire about frequency multipliers (H'22) and operating frequencies (H'23) to get the information required to select a new bit rate.
6. Taking into account the returned information on the frequency multipliers and operating frequencies, send a new-bit-rate selection command (H'3F).
7. After the device and clock mode have been selected, get the information required for programming and erasure of the user boot MAT and user MAT by sending the commands to inquire about the user boot MAT (H'24), user MAT (H'25), erasure block (H'26), and programming size (H'27).
8. After making all necessary inquiries and the new bit rate selection, send the transition-to-programming/erasure state command (H'40) to place the boot program in the programming/erasure state.

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Deep Software Standby	Module Standby	Sleep	Module
BARA	Initialized	Retained	Retained	Initialized	Initialized	Retained	UBC
BAMRA	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BBRA	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BDRA	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BDMRA	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BARB	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BAMRB	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BBRB	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BDRB	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BDMRB	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BRCR	Initialized	Retained	Retained	Initialized	Initialized	Retained	
BRSR	Initialized	Initialized	Retained	Initialized	Initialized	Retained	
BRDR	Initialized	Initialized	Retained	Initialized	Initialized	Retained	
BETR	Initialized	Retained	Retained	Initialized	Initialized	Retained	

Notes: 1. Not initialized by a WDT power-on reset.
2. The OSCSTOP bit is not initialized by a WDT power-on reset.
3. The OSCSTOP bit is initialized.

Item	Symbol	Min.	Max.	Unit	Reference Figure
Read data hold time 1	t_{RDH1}	0	—	ns	Figures 26.11 to 26.15
Read data access time	t_{ACC} *2	$t_{Bcyc} \times (n + 1.5) - 33$ *1	—	ns	Figures 26.11 to 26.15
Access time from read strobe	t_{OE} *2	$t_{Bcyc} \times (n + 1) - 31$ *1	—	ns	Figures 26.11 to 26.15
Write strobe delay time 1	t_{WSD1}	$1/2t_{Bcyc} + 1$	$1/2t_{Bcyc} + 18$	ns	Figures 26.11 to 26.15
Write data delay time 1	t_{WDD1}	—	18	ns	Figures 26.11 to 26.15
Write data hold time 1	t_{WDH1}	1	11	ns	Figures 26.11 to 26.15
Write data hold time	t_{WRH}	0	—	ns	Figures 26.11 to 26.14
$\overline{WAIT}$ setup time	t_{WTS}	$1/2t_{Bcyc} + 17$	—	ns	Figures 26.12 to 26.15
$\overline{WAIT}$ hold time	t_{WTH}	$1/2t_{Bcyc} + 7$	—	ns	Figures 26.12 to 26.15

Notes: t_{Bcyc} indicates external bus clock period (Bϕ = CK).

1. n denotes the number of wait cycles.
2. If the access time conditions are satisfied, the t_{RDS1} condition does not need to be satisfied.