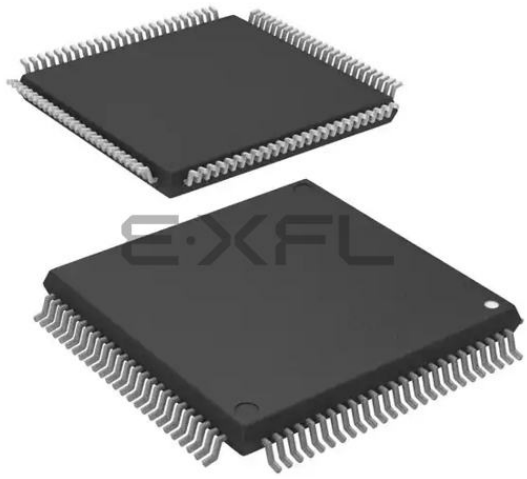

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Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SSU
Peripherals	POR, PWM, WDT
Number of I/O	57
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
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2.5.6 Branch Instructions

Table 2.15 Branch Instructions

Instruction		Operation	Code	Execution Cycles	T Bit
BF	label	If T = 0, disp × 2 + PC → PC; if T = 1, nop	10001011dddddddd	3/1*	—
BF/S	label	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, nop	10001111dddddddd	2/1*	—
BT	label	If T = 1, disp × 2 + PC → PC; if T = 0, nop	10001001dddddddd	3/1*	—
BT/S	label	Delayed branch, if T = 1, disp × 2 + PC → PC; if T = 0, nop	10001101dddddddd	2/1*	—
BRA	label	Delayed branch, disp × 2 + PC → PC	1010dddddddddddd	2	—
BRAF	Rm	Delayed branch, Rm + PC → PC	0000mmmm00100011	2	—
BSR	label	Delayed branch, PC → PR, disp × 2 + PC → PC	1011dddddddddddd	2	—
BSRF	Rm	Delayed branch, PC → PR, Rm + PC → PC	0000mmmm00000011	2	—
JMP	@Rm	Delayed branch, Rm → PC	0100mmmm00101011	2	—
JSR	@Rm	Delayed branch, PC → PR, Rm → PC	0100mmmm00001011	2	—
RTS		Delayed branch, PR → PC	0000000000001011	2	—

Note: * One cycle when the branch is not executed.

5.2 Resets

5.2.1 Types of Resets

Resets have priority over any exception source. There are two types of resets: power-on resets and manual resets. As table 5.5 shows, both types of resets initialize the internal status of the CPU. In power-on resets, all registers of the on-chip peripheral modules are initialized; in manual resets, they are not.

Table 5.5 Reset Status

	Conditions for Transition to Reset State			Internal State		
Type	$\overline{\text{RES}}$	WDT Overflow	$\overline{\text{MRES}}$	CPU, INTC	On-Chip Peripheral Module	POE, PFC, I/O Port
Power-on reset	Low	—	—	Initialized	Initialized	Initialized
	High	Overflow	High	Initialized	Initialized	Initialized
Manual reset	High	Not overflowed	Low	Initialized	Not initialized	Not initialized

5.2.2 Power-On Reset

Power-On Reset by $\overline{\text{RES}}$ Pin: When the $\overline{\text{RES}}$ pin is driven low, this LSI enters the power-on reset state. To reliably reset this LSI, the $\overline{\text{RES}}$ pin should be kept low for at least the oscillation settling time when applying the power or when in standby mode (when the clock is halted) or at least 20 tcyc when the clock is operating. During the power-on reset state, CPU internal states and all registers of on-chip peripheral modules are initialized. See appendix A, Pin States, for the status of individual pins during power-on reset mode.

In the power-on reset state, power-on reset exception handling starts when driving the $\overline{\text{RES}}$ pin high after driving the pin low for the given time. The CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception handling vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception handling vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3 to I0) of the status register (SR) are set to H'F (B'1111).
4. The values fetched from the exception handling vector table are set in PC and SP, then the program starts.

- TIER_5

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	TGIE5U	TGIE5V	TGIE5W
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TGIE5U	0	R/W	TGR Interrupt Enable 5U Enables or disables interrupt requests (TGIU_5) by the CMFU5 bit when the CMFU5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIU_5) disabled 1: Interrupt requests (TGIU_5) enabled
1	TGIE5V	0	R/W	TGR Interrupt Enable 5V Enables or disables interrupt requests (TGIV_5) by the CMFV5 bit when the CMFV5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIV_5) disabled 1: Interrupt requests (TGIV_5) enabled
0	TGIE5W	0	R/W	TGR Interrupt Enable 5W Enables or disables interrupt requests (TGIW_5) by the CMFW5 bit when the CMFW5 bit in TSR_5 is set to 1. 0: Interrupt requests (TGIW_5) disabled 1: Interrupt requests (TGIW_5) enabled

10.3.29 Timer Interrupt Skipping Counter (TITCNT)

TITCNT is an 8-bit readable/writable counter. The MTU2 has one TITCNT. TITCNT retains its value even after stopping the count operation of TCNT_3 and TCNT_4.

Bit:	7	6	5	4	3	2	1	0
	-	3ACNT[2:0]			-	4VCNT[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0.
6 to 4	3ACNT[2:0]	000	R	TGIA_3 Interrupt Counter While the T3AEN bit in TITCR is set to 1, the count in these bits is incremented every time a TGIA_3 interrupt occurs. [Clearing conditions] • When the 3ACNT2 to 3ACNT0 value in TITCNT matches the 3ACOR2 to 3ACOR0 value in TITCR • When the T3AEN bit in TITCR is cleared to 0 • When the 3ACOR2 to 3ACOR0 bits in TITCR are cleared to 0
3	—	0	R	Reserved This bit is always read as 0.
2 to 0	4VCNT[2:0]	000	R	TCIV_4 Interrupt Counter While the T4VEN bit in TITCR is set to 1, the count in these bits is incremented every time a TCIV_4 interrupt occurs. [Clearing conditions] • When the 4VCNT2 to 4VCNT0 value in TITCNT matches the 4VCOR2 to 4VCOR2 value in TITCR • When the T4VEN bit in TITCR is cleared to 0 • When the 4VCOR2 to 4VCOR2 bits in TITCR are cleared to 0

Note: To clear the TITCNT, clear the T3AEN and T4VEN bits in TITCR to 0.

— Example of Procedure for Suppressing MTU2–MTU2S Synchronous Counter Clearing

An example of the procedure for suppressing MTU2–MTU2S synchronous counter clearing is shown in figure 10.63.

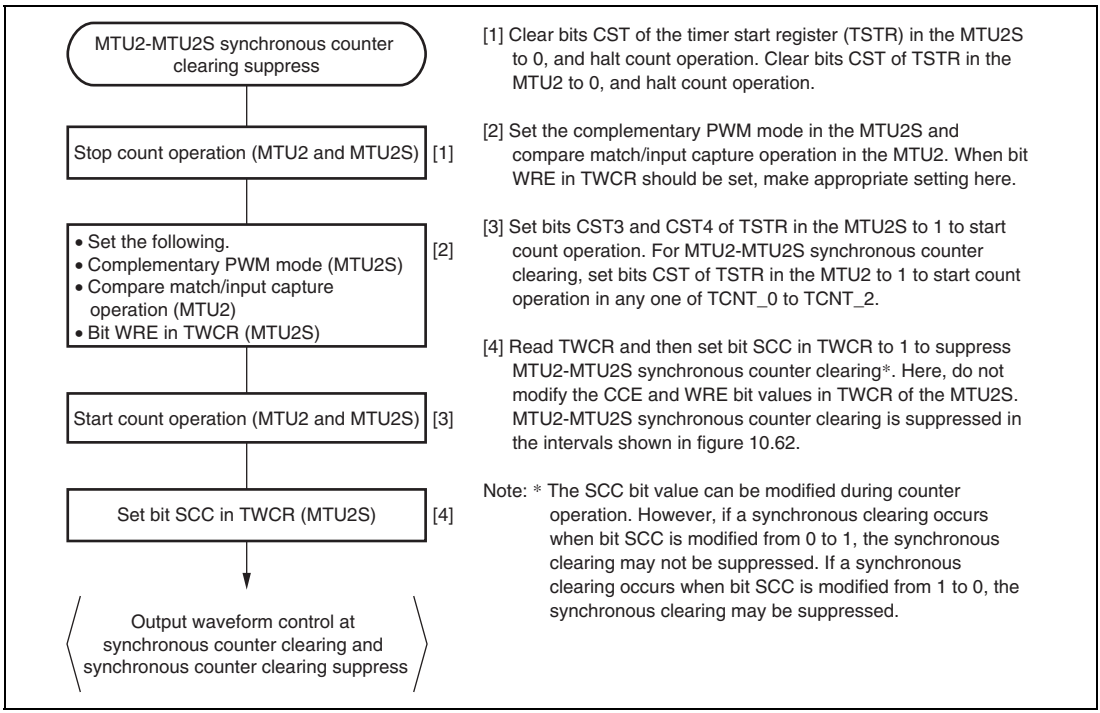


Figure 10.63 Example of Procedure for Suppressing MTU2–MTU2S Synchronous Counter Clearing

— Examples of Suppression of MTU2–MTU2S Synchronous Counter Clearing

Figures 10.64 to 10.67 show examples of operation in which the MTU2S operates in complementary PWM mode and MTU2–MTU2S synchronous counter clearing is suppressed by setting the SCC bit in TWCR in the MTU2S to 1. In the examples shown in figures 10.64 to 10.67, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in figure 10.56, respectively.

In these examples, the WRE bit in TWCR of the MTU2S is set to 1.

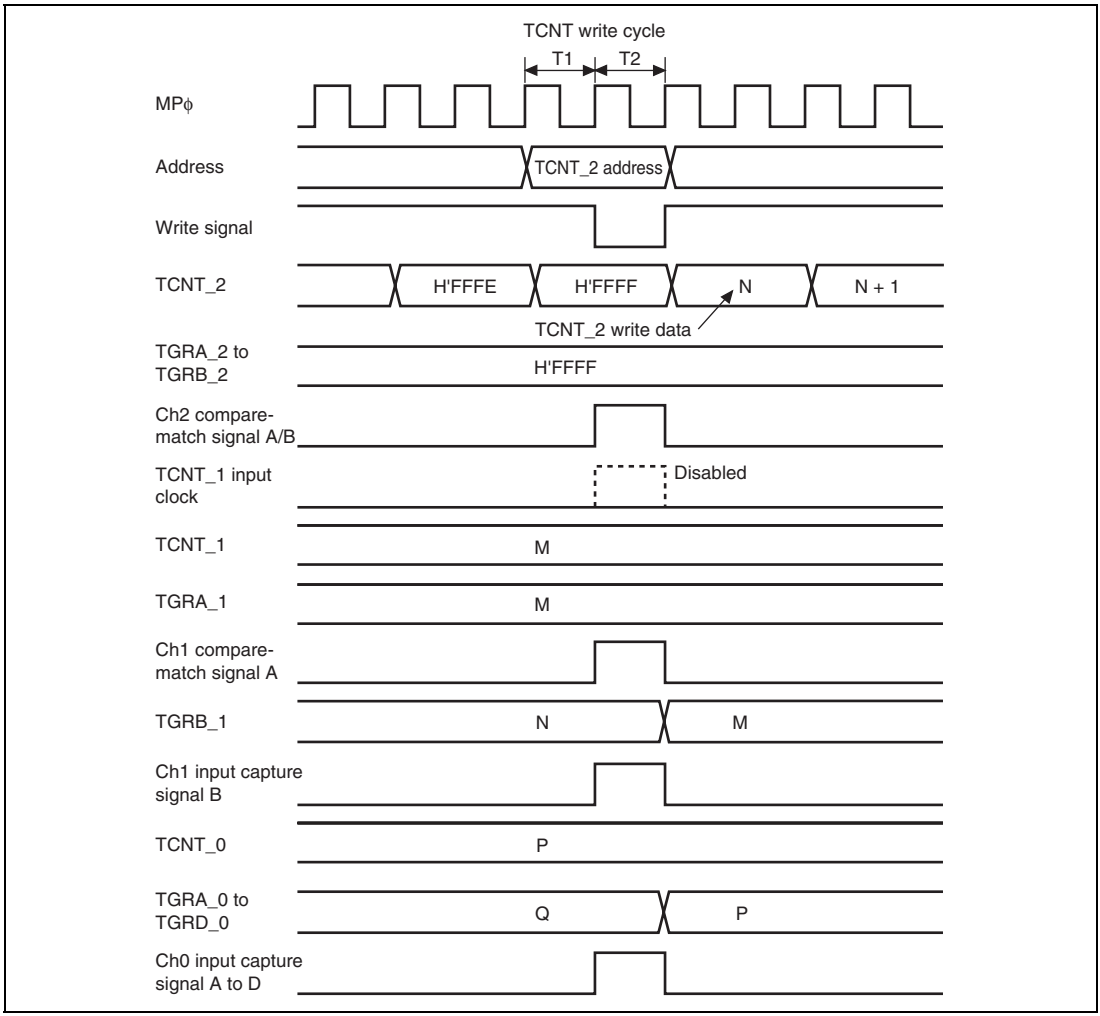


Figure 10.130 TCNT_2 Write and Overflow/Underflow Contention with Cascade Connection

Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Complementary PWM Mode: Figure 10.148 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

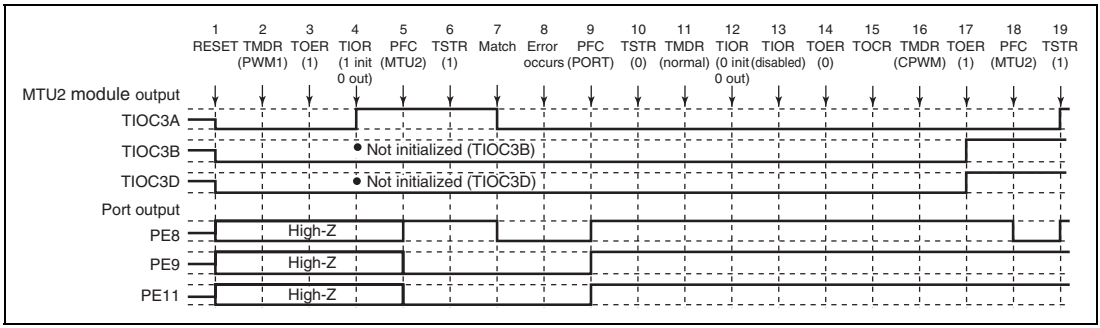


Figure 10.148 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 10.144.

11. Set normal mode for initialization of the normal mode waveform generation section.
12. Initialize the PWM mode 1 waveform generation section with TIOR.
13. Disable operation of the PWM mode 1 waveform generation section with TIOR.
14. Disable channel 3 and 4 output with TOER.
15. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
16. Set complementary PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

Figure 14.5 shows an example of the operation for transmission.

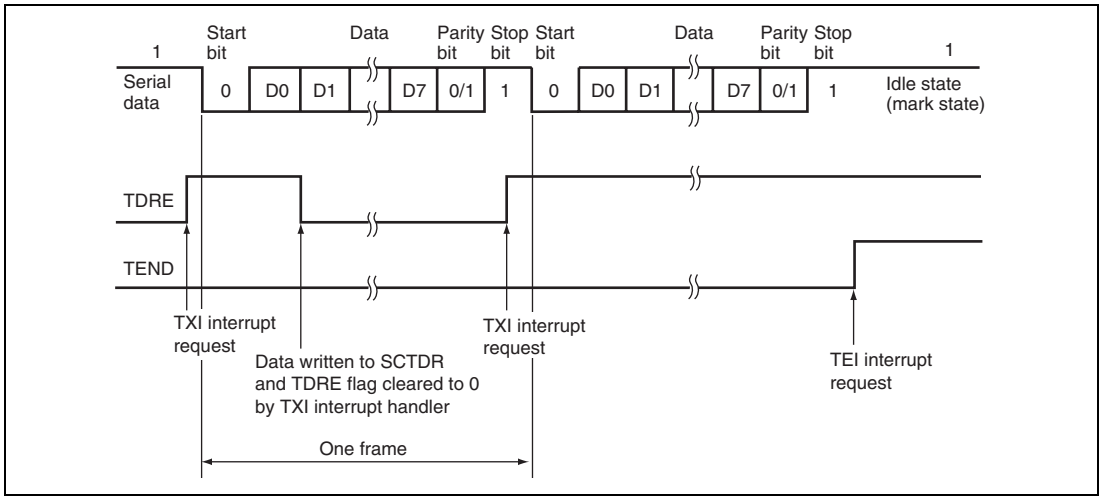
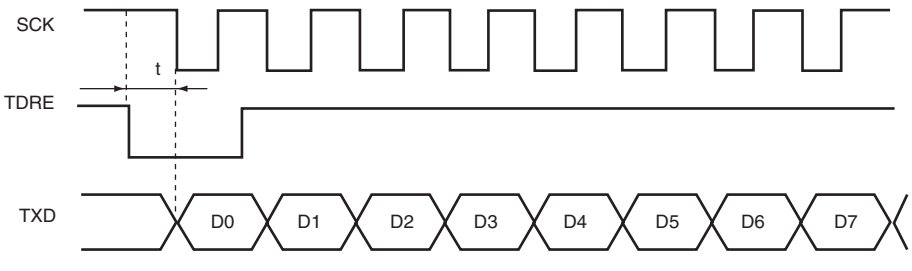


Figure 14.5 Example of Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

14.7.6 Note on Using DTC

When the external clock source is used for the clock for synchronization, input the external clock after waiting for five or more cycles of the peripheral operating clock after SCTDR is modified through the DTC. If a transmit clock is input within four cycles after SCTDR is modified, a malfunction may occur (figure 14.25).



Note: When using the external clock, t must be set to larger than 4 cycles.

Figure 14.25 Example of Clock Synchronous Transfer Using DTC

When data is written to SCTDR by activating the DTC by a TXI interrupt, the TEND flag value becomes undefined. In this case, do not use the TEND flag as the transmit end flag.

14.7.7 Note on Using External Clock in Clock Synchronous Mode

TE and RE must be set to 1 after waiting for four or more cycles of the peripheral operating clock after the SCK external clock is changed from 0 to 1.

TE and RE must be set to 1 only while the SCK external clock is 1.

14.7.8 Module Standby Mode Setting

SCI operation can be disabled or enabled using the standby control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 24, Power-Down Modes.

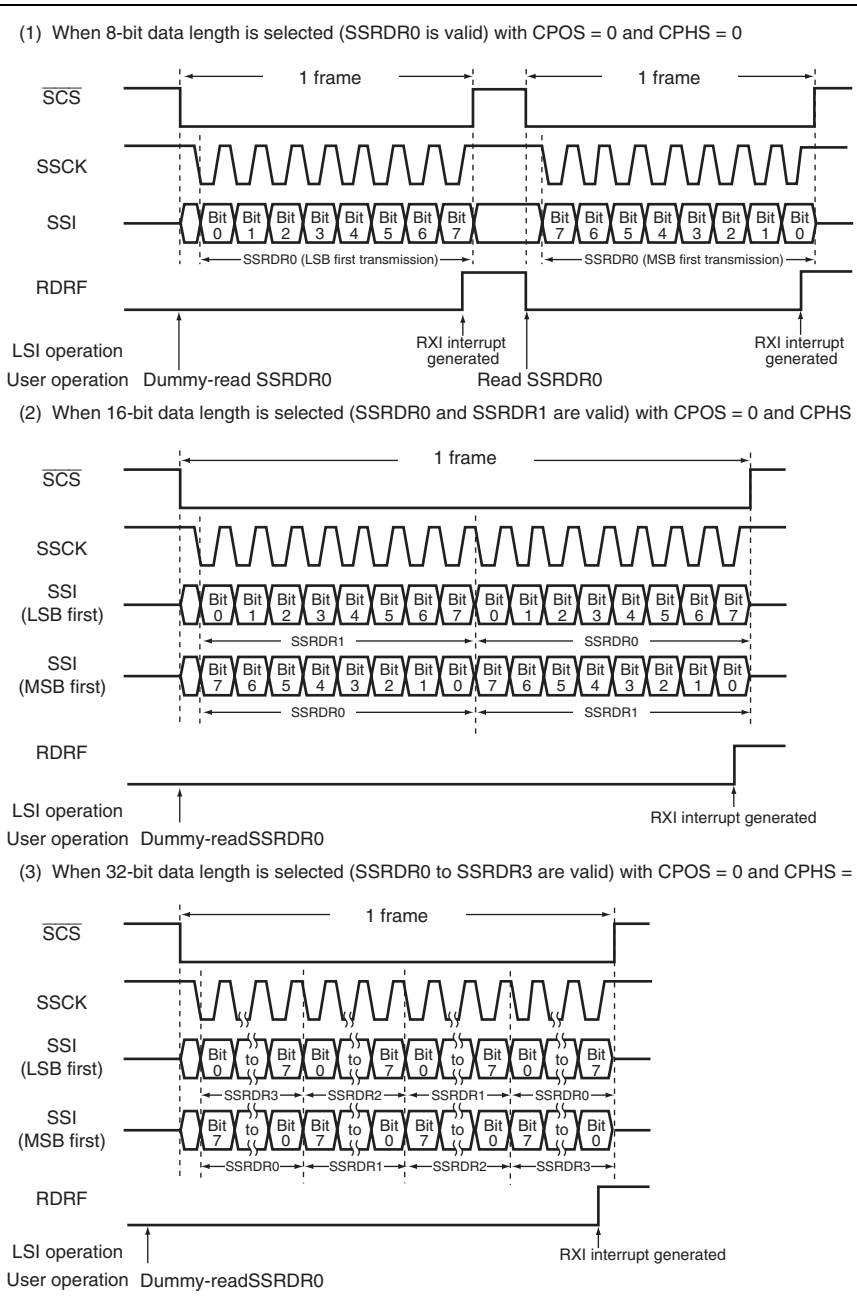


Figure 15.7 Example of Reception Operation (SSU Mode)

16.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data, while the master device outputs the receive clock and returns an acknowledge signal. For slave transmit mode operation timing, refer to figures 16.9 and 16.10.

The transmission procedure and operations in slave transmit mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS bit in ICMR and bits CKS3 to CKS0 in ICCR1. (Initial setting) Set the MST and TRS bits in ICCR1 to select slave receive mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise of the 9th clock pulse. At this time, if the 8th bit data (R/W) is 1, the TRS bit in ICCR1 and the TDRE bit in ICSR are set to 1, and the mode changes to slave transmit mode automatically. The continuous transmission is performed by writing transmit data to ICDRT every time TDRE is set.
3. If TDRE is set after writing last transmit data to ICDRT, wait until TEND in ICSR is set to 1, with TDRE = 1. When TEND is set, clear TEND.
4. Clear TRS for the end processing, and read ICDRR (dummy read). SCL is free.
5. Clear TDRE.

19.7 CAN Bus Interface

A bus transceiver IC is necessary to connect this LSI to a CAN bus. A Renesas HA13721 transceiver IC and its compatible products are recommended. Figure 19.15 shows a sample connection diagram.

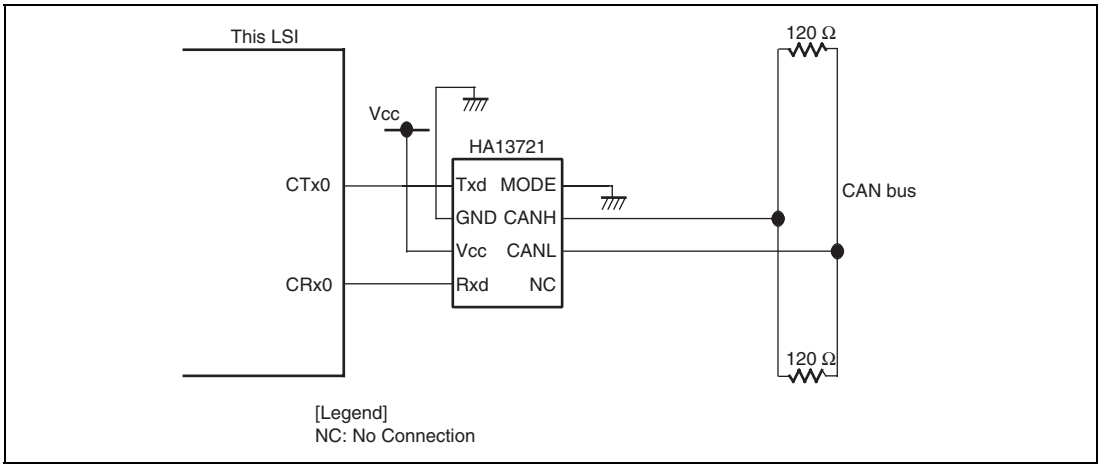


Figure 19.15 High-Speed CAN Interface Using HA13721

Bit	Bit Name	Initial Value	R/W	Description
10	PA14MD2	0*2	R/W	PA14 Mode
9	PA14MD1	0	R/W	Select the function of the PA14/A10/RXD1/SSI pin.
8	PA14MD0	0	R/W	000: PA14 I/O (port) 100: A10 output (BSC)*3 101: SSI I/O (SSU) 110: RXD1 input (SCI) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PA13MD2	0*2	R/W	PA13 Mode
5	PA13MD1	0	R/W	Select the function of the PA13/A9/SCK1/SSCK pin.
4	PA13MD0	0	R/W	000: PA13 I/O (port) 100: A9 output (BSC)*3 101: SSCK I/O (SSU) 110: SCK1 I/O (SCI) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PA12MD2	0*2	R/W	PA12 Mode
1	PA12MD1	0	R/W	Select the function of the PA12/A8/SCK0/$\overline{\text{SCS}}$ pin.
0	PA12MD0	0	R/W	000: PA12 I/O (port) 100: A8 output (BSC)*3 101: $\overline{\text{SCS}}$ I/O (SSU) 110: SCK0 I/O (SCI) Other than above: Setting prohibited

Notes: 1. The initial value is 1 in the on-chip ROM enabled/disabled external-extension mode.
2. The initial value is 1 in the on-chip ROM disabled external-extension mode.
3. This function is available only in the on-chip ROM enabled/disabled external-extension mode. Do not set to this value in single-chip mode.

22.6 Protection

There are three kinds of flash memory program/erase protection: hardware, software, and error protection.

22.6.1 Hardware Protection

Programming and erasing of flash memory is forcibly disabled or suspended by hardware protection. In this state, the downloading of an on-chip program and initialization of the flash memory are possible. However, an activated program for programming or erasure cannot program or erase locations in a user MAT, and the error in programming/erasing is reported in the FPFR parameter.

Table 22.9 Hardware Protection

		Function to be Protected	
Item	**Description**	**Download**	**Programming/ Erasure**
FWE-pin protection	The input of a low-level signal on the FWE pin clears the FWE bit of FCCS and the LSI enters a programming/erasing-protected state.	—	√
Reset/standby protection	• A power-on reset (including a power-on reset by the WDT) and entry to standby mode initializes the programming/erasing interface registers and the LSI enters a programming/erasing-protected state. • Resetting by means of the $\overline{\text{RES}}$ pin after power is initially supplied will not make the LSI enter the reset state unless the $\overline{\text{RES}}$ pin is held low until oscillation has stabilized. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width that is specified in the section on AC characteristics. If the LSI is reset during programming or erasure, data in the flash memory is not guaranteed. In this case, execute erasure and then execute programming again.	√	√

Bit	Bit Name	Initial Value	R/W	Description
2	MSTP10	1	R/W	Module Stop Bit 10 When this bit is set to 1, the clock supply to the SSU is halted. 0: SSU operates 1: Clock supply to SSU halted
1	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
0	MSTP8	1	R/W	Module Stop Bit 8 When this bit is set to 1, the clock supply to the RCAN-ET_0 is halted. 0: RCAN-ET_0 operates 1: Clock supply to RCAN-ET_0 halted

24.7 Module Standby Mode

24.7.1 Transition to Module Standby Mode

Setting the MSTP bits in the standby control registers (STBCR2 to STBCR5) to 1 halts the supply of clocks to the corresponding on-chip peripheral modules. This function can be used to reduce the power consumption in normal mode.

Do not access registers of an on-chip peripheral module which has been set to enter module standby mode. For details on the states of on-chip peripheral module registers in module standby mode, refer to section 25.3, Register States in Each Operating Mode.

24.7.2 Canceling Module Standby Function

The module standby function can be canceled by clearing the MSTP bits in STBCR2 to STBCR5 to 0. The module standby function can be canceled by a power-on reset for modules whose MSTP bit has an initial value of 0.

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access Cycles	Connected Bus Width
Timer counter_0	TCNT_0	16	H'FFFFC306	MTU2	16	MPϕ (reference clock)	16 bits
Timer general register A_0	TGRA_0	16	H'FFFFC308		16, 32	B: 2	
Timer general register B_0	TGRB_0	16	H'FFFFC30A		16	W: 2	
Timer general register C_0	TGRC_0	16	H'FFFFC30C		16, 32	L: 4	
Timer general register D_0	TGRD_0	16	H'FFFFC30E		16		
Timer general register E_0	TGRE_0	16	H'FFFFC320		16, 32		
Timer general register F_0	TGRF_0	16	H'FFFFC322		16		
Timer interrupt enable register 2_0	TIER2_0	8	H'FFFFC324		8, 16		
Timer status register 2_0	TSR2_0	8	H'FFFFC325		8		
Timer buffer operation transfer mode register_0	TBTM_0	8	H'FFFFC326		8		
Timer control register_1	TCR_1	8	H'FFFFC380		8, 16		
Timer mode register_1	TMDR_1	8	H'FFFFC381		8		
Timer I/O control register_1	TIOR_1	8	H'FFFFC382		8		
Timer interrupt enable register_1	TIER_1	8	H'FFFFC384		8, 16, 32		
Timer status register_1	TSR_1	8	H'FFFFC385		8		
Timer counter_1	TCNT_1	16	H'FFFFC386		16		
Timer general register A_1	TGRA_1	16	H'FFFFC388		16, 32		
Timer general register B_1	TGRB_1	16	H'FFFFC38A		16		
Timer input capture control register	TICCR	8	H'FFFFC390		8		
Timer control register_2	TCR_2	8	H'FFFFC400		8, 16		
Timer mode register_2	TMDR_2	8	H'FFFFC401		8		
Timer I/O control register_2	TIOR_2	8	H'FFFFC402		8		
Timer interrupt enable register_2	TIER_2	8	H'FFFFC404		8, 16, 32		
Timer status register_2	TSR_2	8	H'FFFFC405		8		
Timer counter_2	TCNT_2	16	H'FFFFC406		16		
Timer general register A_2	TGRA_2	16	H'FFFFC408		16, 32		
Timer general register B_2	TGRB_2	16	H'FFFFC40A		16		

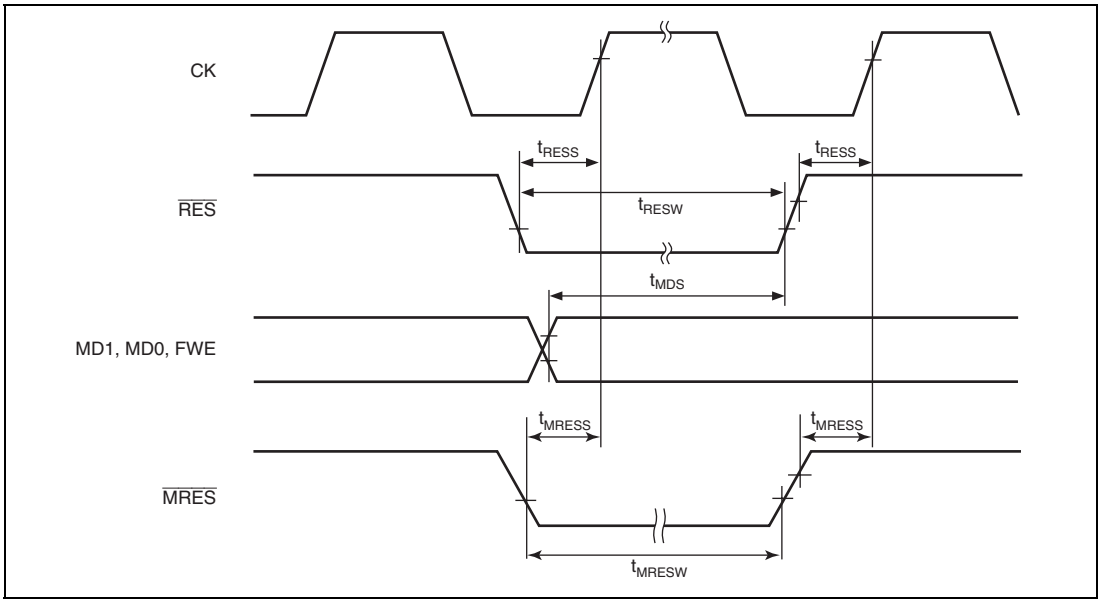


Figure 26.6 Reset Input Timing

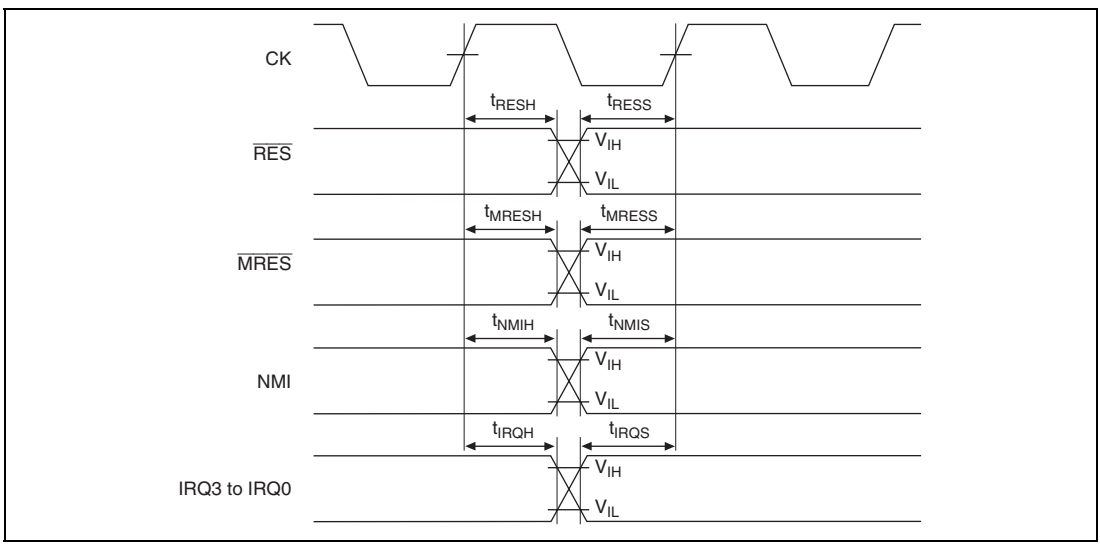


Figure 26.7 Interrupt Signal Input Timing

Item	Page	Revision (See Manual for Details)
1.4 Pin Functions Table 1.2 Pin Functions	15	Table amended

Classification	Symbol	I/O	Name	Function
User break controller (UBC)	$\overline{\text{UBCTRG}}$	O	User break trigger output	Trigger output pin for UBC condition match Available only in the SH7136/ SH7137.
User debugging interface (H-UDI) (SH7136 and SH7137 only)	TCK	I	Test clock	Test-clock input pin.
	TMS	I	Test mode select	Inputs the test-mode select signal.
	TDI	I	Test data input	Serial input pin for instructions and data.
	TDO	O	Test data output	Serial output pin for instructions and data.
	$\overline{\text{TRST}}$	I	Test reset	Initialization-signal input pin.

	16	Classification	Symbol	I/O	Name	Function
		E10A interface (SH7136 and SH7137 only)	$\overline{\text{ASEMDO}}$	I	ASE mode	Sets the ASE mode. When this pin is driven low, the LSI enters ASE mode, and when driven high, the LSI operates in normal mode. Emulator dedicated functions can be used in the ASE mode. When nothing is input to this pin, it is pulled up internally.
			$\overline{\text{ASEBRK}}$	I	Break request	E10A emulator break input
			$\overline{\text{ASEBRKAK}}$	O	Break mode acknowledge	Indicates the E10A emulator has entered the break mode.

3.4 Address Map Figure 3.1 Address Map for Each Operating Mode in SH7131 (128-Kbyte Flash Memory Version)	52	Figure added
Figure 3.2 Address Map for Each Operating Mode in SH7131 and SH7136 (256-Kbyte Flash Memory Version)	53	Figure title amended
Figure 3.3 Address Map for Each Operating Mode in SH7132 (128-Kbyte Flash Memory Version)	54	Figure added
Figure 3.4 Address Map for Each Operating Mode in SH7132 and SH7137 (256-Kbyte Flash Memory Version)	55	Figure title amended