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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe162fn-40f80l-aa

16-Bit

Architecture

XE162FN, XE162HN

16-Bit Single-Chip

Real Time Signal Controller

XE166 Family / Value Line

Data Sheet

V1.5 2013-02

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Summary of Features

1.1 Device Types

The following XE162xN device types are available and can be ordered through Infineon's direct and/or distribution channels. The devices are available for the SAF temperature range. SAK types are available upon request only.

Table 1 Synopsis of XE162xN Device Types

Derivative	Flash Memory¹⁾	PSRAM DSRAM²⁾	Capt./Comp. Modules	ADC³⁾ Chan.	Interfaces³⁾
XE162FN-16F80L	128 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162FN-24F80L	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162FN-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162HN-16F80L	128 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.
XE162HN-24F80L	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.
XE162HN-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.

1) Specific information about the on-chip Flash memory in [Table 2](#).

2) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

3) Specific information about the available channels in [Table 4](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.2 Definition of Feature Variants

The XE162xN types are offered with several Flash memory sizes. [Table 2](#) and [Table 3](#) describe the location of the available Flash memory.

Table 2 Continuous Flash Memory Ranges

Total Flash Size	1st Range ¹⁾	2nd Range	3rd Range
320 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C4'FFFF _H	n.a.
192 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C1'FFFF _H	C4'0000 _H ... C4'FFFF _H
128 Kbytes	C0'0000 _H ... C0'FFFF _H	C4'0000 _H ... C4'FFFF _H	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0 ¹⁾	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE162xN types are offered with different interface options. [Table 4](#) lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels / Message Objects
7 ADC0 channels	CH0, CH2, CH4, CH8, CH10, CH13, CH15
2 ADC1 channels	CH0, CH4
2 CAN nodes	CAN0, CAN1 64 message objects
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XE162xN types are offered with several SRAM memory sizes. [Figure 1](#) shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input
8	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	ESR1_6	I	DA/A	ESR1 Trigger Input 6
10	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
11	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
12	V_{AREF}	-	PS/A	Reference Voltage for A/D Converters ADC0/1
13	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
14	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
15	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
19	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
28	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input
29	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input
30	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input
	ESR1_10	I	St/B	ESR1 Trigger Input 10
31	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO 0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO 1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
	ESR2_6	I	St/B	ESR2 Trigger Input 6

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
38	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2	St/B	CCU60 Channel 0 Output
	CCU60_CC60INA	I	St/B	CCU60 Channel 0 Input
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
39	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC61	O2	St/B	CCU60 Channel 1 Output
	CCU60_CC61INA	I	St/B	CCU60 Channel 1 Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input
40	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2	St/B	CCU60 Channel 2 Output
	CCU60_CC62INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
42	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input

General Device Information

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	P10.9	O0 / I	St/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLKOUT	O2	St/B	USIC0 Channel 1 Master Clock Output
	CCU60_CCP OS2A	I	St/B	CCU60 Position Input 2
	TCK_B	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	GPT12E Timer T3 Count/Gate Input
53	P10.10	O0 / I	St/B	Bit 10 of Port 10, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	U0C0_DX2C	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX1A	I	St/B	USIC0 Channel 1 Shift Clock Input
	TDI_B	IH	St/B	JTAG Test Data Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
54	P10.11	O0 / I	St/B	Bit 11 of Port 10, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	BRKOUT	O2	St/B	OCDS Break Signal Output
	U1C0_DX1D	I	St/B	USIC1 Channel 0 Shift Clock Input
	TMS_B	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

General Device Information

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XE162xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
63	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
6	V_{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
24, 41, 57	V_{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
9	V_{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

Functional Description

Table 7 XE162xN Memory Map (cont'd)¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
Reserved for DSRAM	00'8000 _H	00'9FFF _H	8 Kbytes	
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed byte-wise or word-wise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 16 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the quoted device type.

Functional Description

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

3.8 Capture/Compare Units CCU6x

The XE162xN types feature the CCU60 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

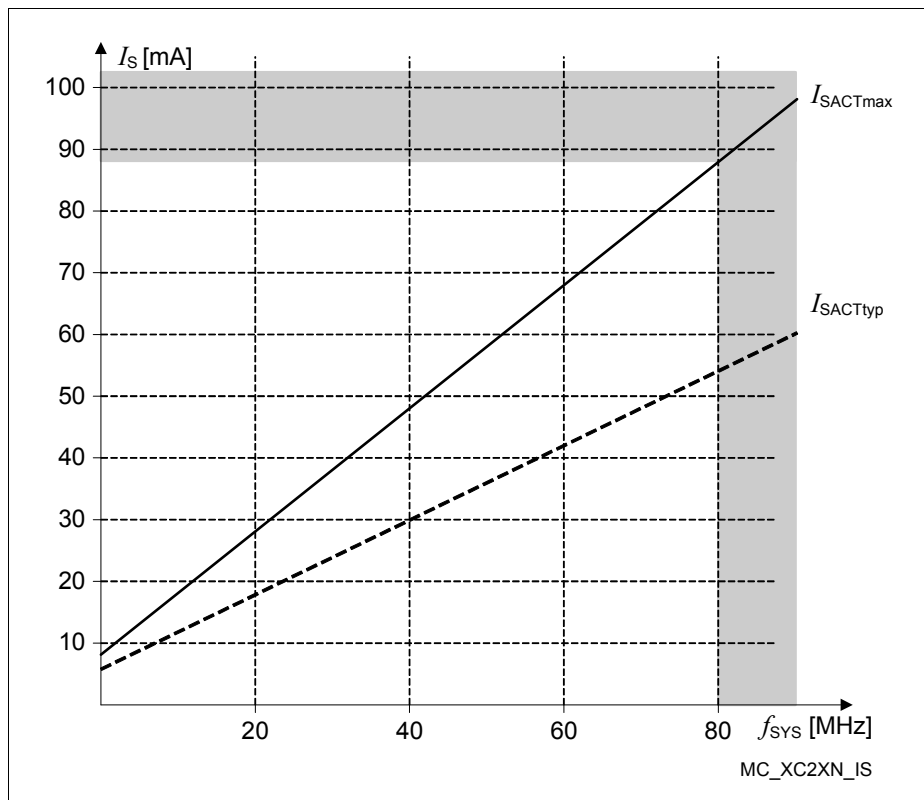


Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 18 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current ¹⁾	I_{LK1} CC	–	0.03	0.04	mA	$T_J = 25\text{ }^{\circ}\text{C}^{(1)}$
		–	0.5	1.2	mA	$T_J = 85\text{ }^{\circ}\text{C}^{(1)}$
		–	1.9	5.5	mA	$T_J = 125\text{ }^{\circ}\text{C}^{(1)}$
		–	3.9	12.2	mA	$T_J = 150\text{ }^{\circ}\text{C}^{(1)}$

¹⁾ All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at $V_{DDP} - 0.1$ V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

4.7 AC Parameters

These parameters describe the dynamic behavior of the XE162xN.

4.7.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

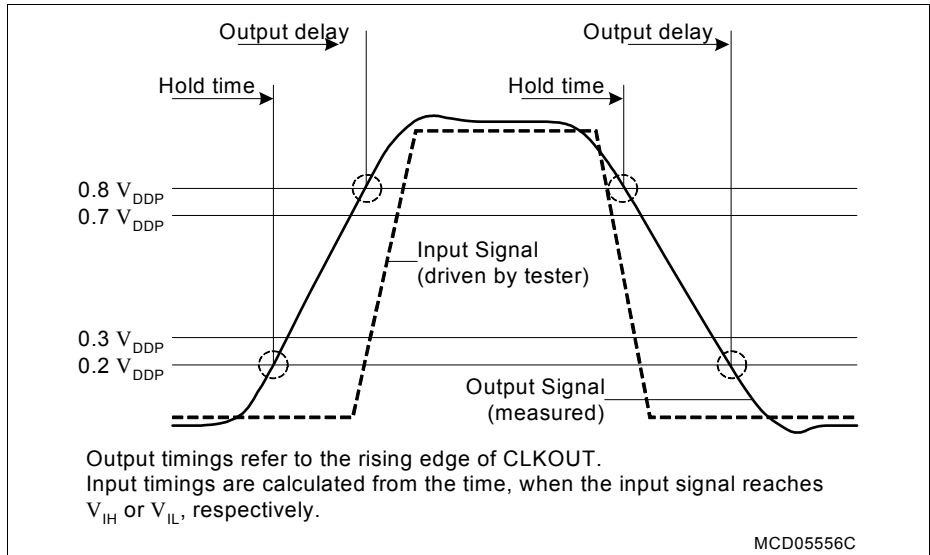


Figure 17 Input Output Waveforms

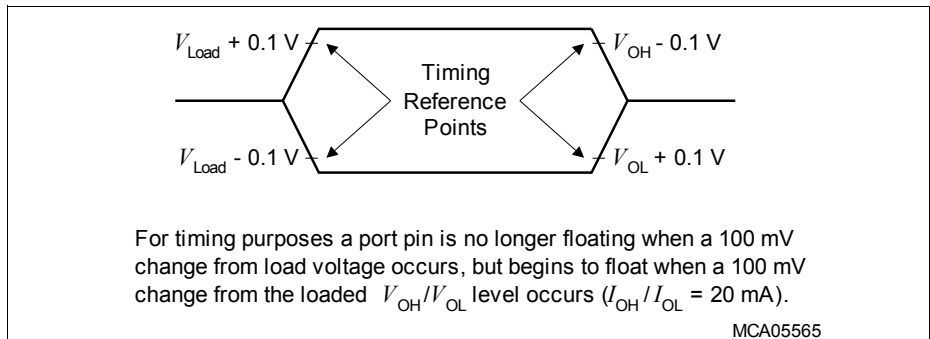


Figure 18 Floating Waveforms

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$$f_{\text{SYS}} = f_{\text{IN}}$$

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$$f_{\text{SYS}} = f_{\text{OSC}} / K1.$$

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$$f_{\text{SYS}} = f_{\text{OSC}} / 1024.$$

4.7.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{\text{SYS}} = f_{\text{IN}} \times \mathbf{F}$).

F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):

$$(\mathbf{F} = \mathbf{N} / (\mathbf{P} \times \mathbf{K2})).$$

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .

Table 25 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency	f_{VCO} CC	50	—	110	MHz	$VCOSSEL=00b$; $VCOmode=$ controlled
		10	—	40	MHz	$VCOSSEL=00b$; $VCOmode=$ free running
		100	—	160	MHz	$VCOSSEL=01b$; $VCOmode=$ controlled
		20	—	80	MHz	$VCOSSEL=01b$; $VCOmode=$ free running

4.7.2.2 Wakeup Clock

When wakeup operation is selected ($SYSCON0.CLKSEL = 00_B$), the system clock is derived from the low-frequency wakeup clock source:

$$f_{SYS} = f_{WU}$$

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.

Please refer to the Programmer's Guide.

Electrical Parameters

- 1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .
- 2) Overload conditions must not occur on pin XTAL1.

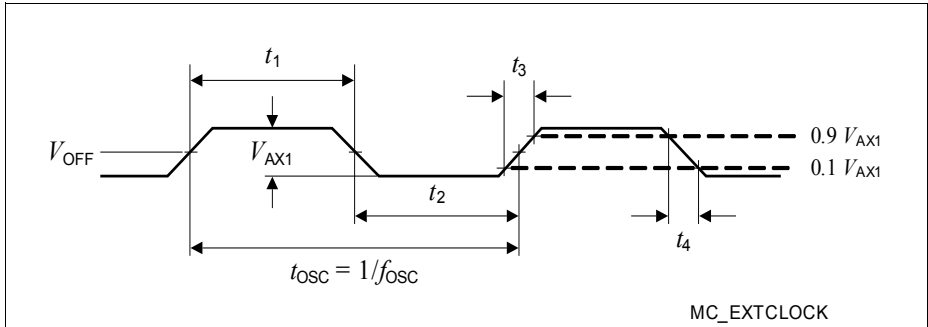


Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.

The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

4.7.4 Pad Properties

The output pad drivers of the XE162xN can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP} . Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 is valid under the following conditions: $V_{DDP} \leq 5.5 \text{ V}$; $V_{DDP\text{typ.}} 5 \text{ V}$; $V_{DDP} \geq 4.5 \text{ V}$

Table 27 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	–	–	4.0	mA	Driver_Strength = Medium
		–	–	10	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	2.5	mA	Driver_Strength = Strong
		–	–	0.1	mA	Driver_Strength = Weak

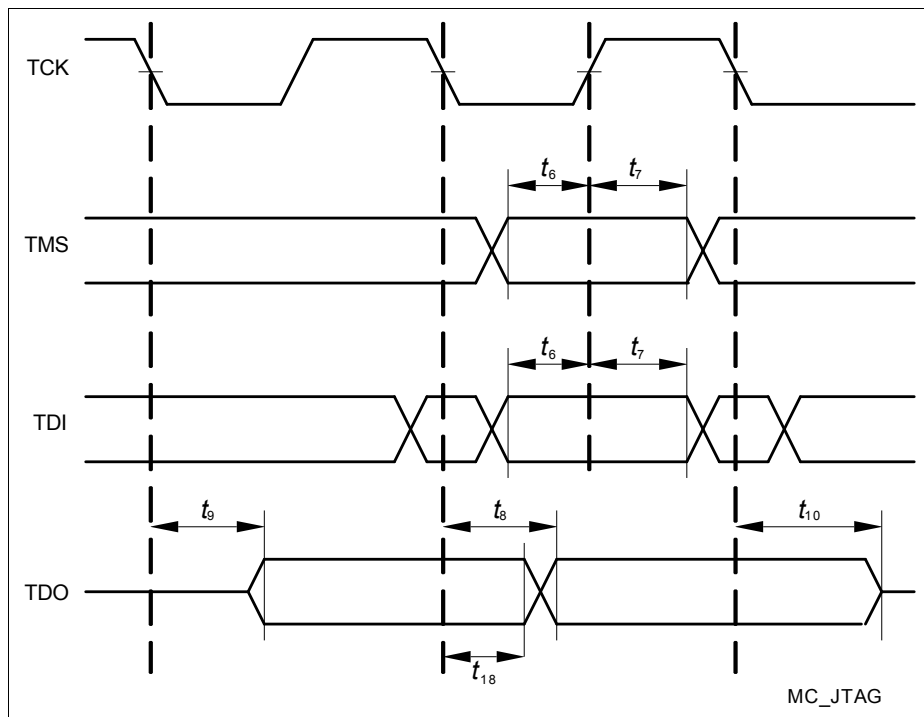


Figure 27 JTAG Timing