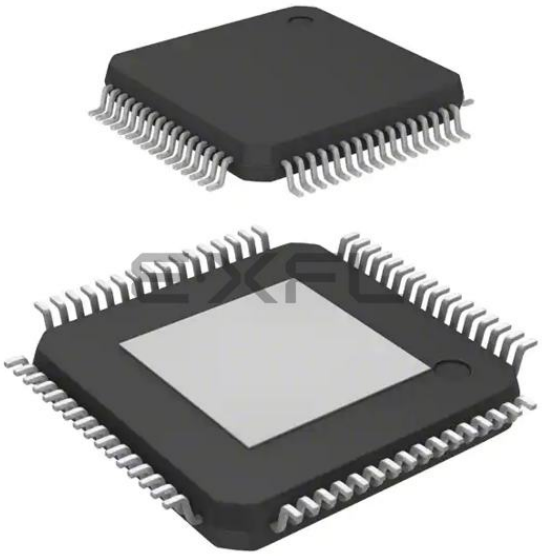
Infineon Technologies - SAK-XE162FN-16F80L AA Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xe162fn-16f80l-aa

16-Bit

Architecture

XE162FN, XE162HN

16-Bit Single-Chip
Real Time Signal Controller
XE166 Family / Value Line

Data Sheet

V1.5 2013-02

Microcontrollers

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
44	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
45	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
46	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U1C0_SELO0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_CTRAPA	I	St/B	**CCU60 Emergency Trap Input**

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

Note: The actual size of the DSRAM depends on the quoted device type.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 7**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 320 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 1 module of 256 Kbytes. Each module is organized in 4-Kbyte sectors. The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.3 Memory Protection Unit (MPU)

The XE162xN's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XE162xN's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.6 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE162xN provides a broad range of debug and emulation features. User software running on the XE162xN can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XE166 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

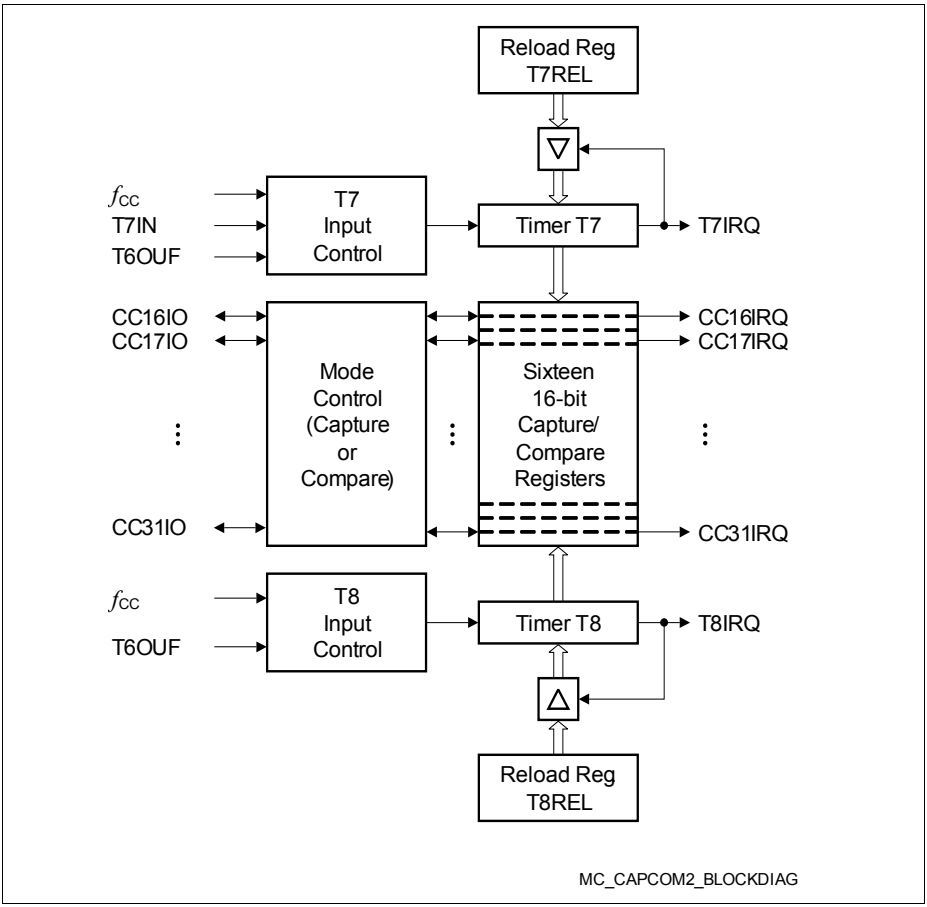


Figure 6 CAPCOM Unit Block Diagram

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction[1)]	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

4.3.3 Power Consumption

The power consumed by the XE162xN depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} and V_{DDI1} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2, Thermal Considerations**.

Note: Operating Conditions apply.

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 22 Coding of bit fields LEVxV in Register SWDCON0

Code	Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V- 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 23**.

Table 23 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Voltage Level	Notes[1)]
000_B-011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE162xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

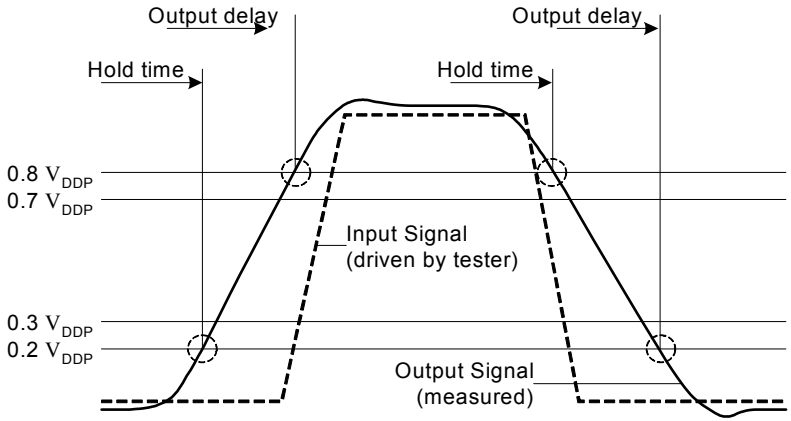
Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7 AC Parameters

These parameters describe the dynamic behavior of the XE162xN.

4.7.1 Testing Waveforms

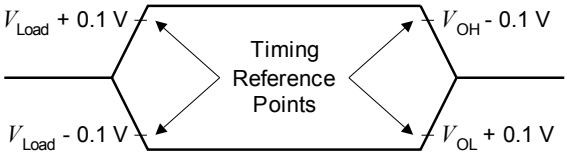
These values are used for characterization and production testing (except pin XTAL1).



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556C

Figure 17 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 18 Floating Waveforms

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of f_{SYS} is the same as the frequency of f_{IN}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN}.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

4.7.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN}. The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE162xN. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 26 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	16	MHz	Input= Crystal or Ceramic Resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	µA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1[1)]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 4 MHz; $f_{OSC} <$ 16 MHz
		0.4 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 16 MHz; $f_{OSC} <$ 25 MHz
		0.5 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 25 MHz; $f_{OSC} \leq$ 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2)]

1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
2) Overload conditions must not occur on pin XTAL1.

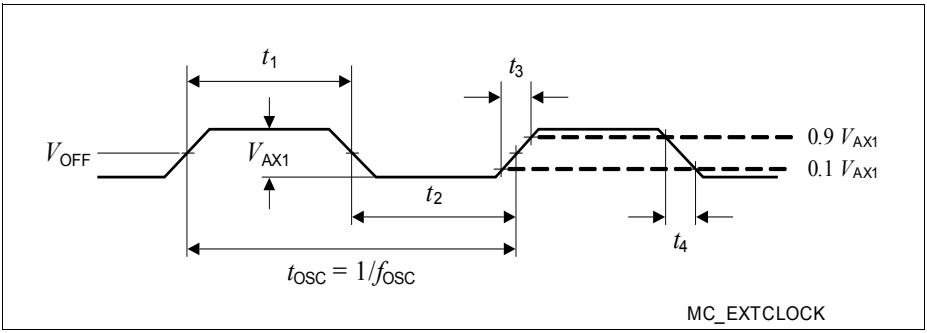


Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	23 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	11.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	4.2 + 0.14 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	20.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	212 + 1.9 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 30 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 10[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 9[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-7	–	11	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 31 is valid under the following conditions: C_L= 20 pF; SSC= slave ; voltage_range= upper

Table 31 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	

Table 31 USIC SSC Slave Mode Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 32 is valid under the following conditions: C_L= 20 pF; SSC= slave ; voltage_range= lower

Table 32 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	8	–	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

4.7.6 Debug Interface Timing

The debugger can communicate with the XE162xN either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 33 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 33 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1)]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1)]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	17	20	–	ns	

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

Table 34 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

www.infineon.com

Published by Infineon Technologies AG