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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 320KB (320K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 34K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-64-6 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe162fn40f80laafxqsa1 |

**XE162xN Data Sheet**
**Revision History: V1.5 2013-02**

Previous Versions:
V1.4, 2011-07
V1.3, 2010-04
V1.2, 2009-07
V1.1, 2009-07
V1.0, 2009-03 Preliminary

| Page | Subjects (major changes since last revision) |
|---|---|
| 26 | Added AB step marking. |
| 76 | Errata SWD_X.P002 implemented: $V_{SWD}$ tolerance boundaries for 5.5 V are changed. |
| 78 | Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”. |
| 79 | Errata FLASH_X.P001 implemented: Test Condition for Flash parameter $N_{ER}$ corrected |

**Trademarks**



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**16-Bit Single-Chip**
**Real Time Signal Controller**
**XE162xN (XE166 Family)**

# 1 Summary of Features

For a quick overview and easy reference, the features of the XE162xN are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 96 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 16 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 320 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 62 | $\overline{\text{PORST}}$ | I | In/B | **Power On Reset Input**<br>A low level at this pin resets the XE162xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns.<br>An internal pull-up device will hold this pin high when nothing is driving it. |
| 63 | $\overline{\text{ESR0}}$ | O0 / I | St/B | **External Service Request 0**<br>After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up. |
| | U1C0_DX0E | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2B | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| 6 | $V_{DDIM}$ | - | PS/M | **Digital Core Supply Voltage for Domain M**<br>Decouple with a ceramic capacitor, see Data Sheet for details. |
| 24, 41, 57 | $V_{DDI1}$ | - | PS/1 | **Digital Core Supply Voltage for Domain 1**<br>Decouple with a ceramic capacitor, see Data Sheet for details.<br>All $V_{DDI1}$ pins must be connected to each other. |
| 9 | $V_{DDPA}$ | - | PS/A | **Digital Pad Supply Voltage for Domain A**<br>Connect decoupling capacitors to adjacent $V_{DDP}/V_{SS}$ pin pairs as close as possible to the pins.<br>*Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage* $V_{DDPA}$. |

## 3.5 Interrupt System

The architecture of the XE162xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE162xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XE162xN can react quickly to the occurrence of non-deterministic events.

### Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

### External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

### Trap Processing

The XE162xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

## 3.8 Capture/Compare Units CCU6x

The XE162xN types feature the CCU60 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

### Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

### Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

### Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE162xN to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

### Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  – module capability: maximum baud rate = $f_{SYS}$ / 4
  – data frame length programmable from 1 to 63 bits
  – MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  – module capability: maximum baud rate = $f_{SYS}$ / 16
  – checksum generation under software control
  – baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  – module capability: maximum baud rate = $f_{SYS}$ / 2, limited by loop delay
  – number of data bits programmable from 1 to 63, more with explicit stop condition
  – MSB or LSB first
  – optional control of slave select signals
- **IIC** (Inter-IC Bus)
  – supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  – module capability: maximum baud rate = $f_{SYS}$ / 2

*Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).*

## 3.13 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

*Note: The number of CAN nodes and message objects depends on the selected device type.*

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

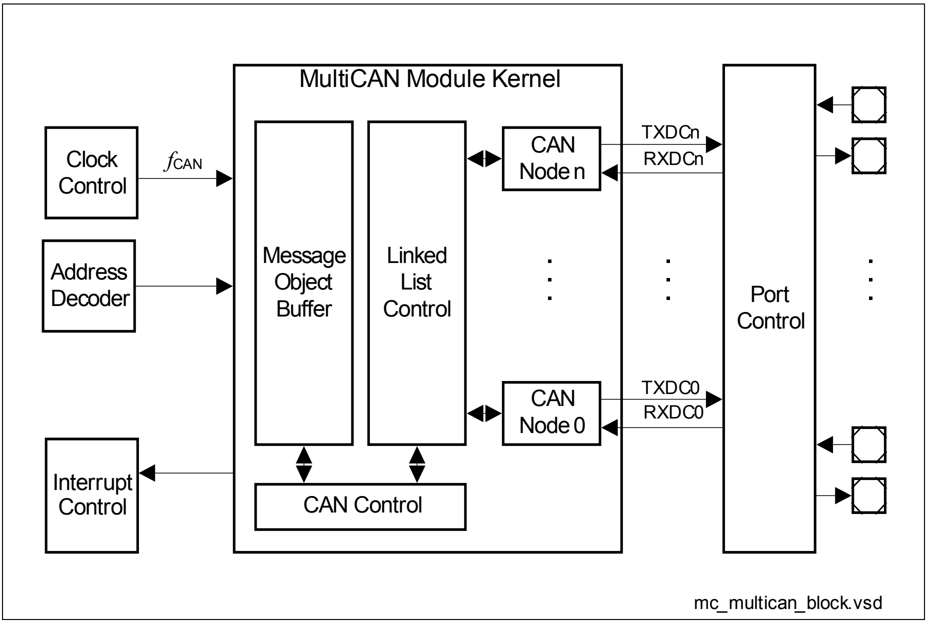


**Figure 12 Block Diagram of MultiCAN Module**

## 3.16 Clock Generation

The Clock Generation Unit can generate the system clock signal $f_{SYS}$ for the XE162xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

**Table 10 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| ROL/ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |
| JMPA/I/R | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| JB(C) | Jump relative if direct bit is set (and clear bit) | 4 |
| JNB(S) | Jump relative if direct bit is not set (and set bit) | 4 |
| CALLA/I/R | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH/POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET(P) | Return from intra-segment subroutine (and pop direct word register from system stack) | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SBRK | Software Break | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Unused instruction[1)] | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT/ENWDT | Disable/Enable Watchdog Timer | 4 |
| EINIT | End-of-Initialization Register Lock | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |

**Table 15 DC Characteristics for Upper Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output High voltage[7)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$ [8)] |
| Output Low Voltage[7)] | $V_{OL}$ CC | – | – | 0.4 | V | $I_{OL} \leq I_{OLnom}$ [8)] |
| | | – | – | 1.0 | V | $I_{OL} \leq I_{OLmax}$ |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

**Table 16 DC Characteristics for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output High voltage[7] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$ [8] |
| Output Low Voltage[7] | $V_{OL}$ CC | – | – | 0.4 | V | $I_{OL} \leq I_{OLnom}$ [8] |
| | | – | – | 1.0 | V | $I_{OL} \leq I_{OLmax}$ |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ}$ = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} <= V_{IL}$ for a pullup; $V_{PIN} >= V_{IH}$ for a pulldown.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} >= V_{IH}$ for a pullup; $V_{PIN} <= V_{IL}$ for a pulldown.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

### 4.3.3 Power Consumption

The power consumed by the XE162xN depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current $I_S$ depends on the device activity
- The leakage current $I_{LK}$ depends on the device temperature

To determine the actual power consumption, always both components, switching current $I_S$ and leakage current $I_{LK}$ must be added:

$I_{DDP} = I_S + I_{LK}$.

*Note: The power consumption values are not subject to production test. They are verified by design/characterization.*
*To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.*

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

*Note: The maximum values cover the complete specified operating range of all manufactured devices.*
*The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.*
*After a power reset, the decoupling capacitors for $V_{DDIM}$ and $V_{DDI1}$ are charged with the maximum possible current.*

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

*Note: Operating Conditions apply.*

## 4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

*Note: Operating Conditions apply.*

**Table 19 ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at an analog input | $C_{AINSW}$ CC | – | – | 4 | pF | not subject to production test [1)] |
| Total capacitance at an analog input | $C_{AINT}$ CC | – | – | 10 | pF | not subject to production test [1)] |
| Switched capacitance at the reference input | $C_{AREFSW}$ CC | – | – | 7 | pF | not subject to production test [1)] |
| Total capacitance at the reference input | $C_{AREFT}$ CC | – | – | 15 | pF | not subject to production test [1)] |
| Differential Non-Linearity Error | $\|EA_{DNL}\|$ CC | – | 0.8 | 1 | LSB | |
| Gain Error | $\|EA_{GAIN}\|$ CC | – | 0.4 | 0.8 | LSB | |
| Integral Non-Linearity | $\|EA_{INL}\|$ CC | – | 0.8 | 1.2 | LSB | |
| Offset Error | $\|EA_{OFF}\|$ CC | – | 0.5 | 0.8 | LSB | |
| Analog clock frequency | $f_{ADCI}$ SR | 0.5 | – | 16.5 | MHz | voltage_range= lower |
| | | 0.5 | – | 20 | MHz | voltage_range= upper |
| Input resistance of the selected analog channel | $R_{AIN}$ CC | – | – | 2 | kOhm | not subject to production test [1)] |
| Input resistance of the reference input | $R_{AREF}$ CC | – | – | 2 | kOhm | not subject to production test [1)] |

### 4.7.2 Definition of Internal Timing

The internal operation of the XE162xN is controlled by the internal system clock $f_{SYS}$.

Because the system clock signal $f_{SYS}$ can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate $f_{SYS}$. This must be considered when calculating the timing for the XE162xN.

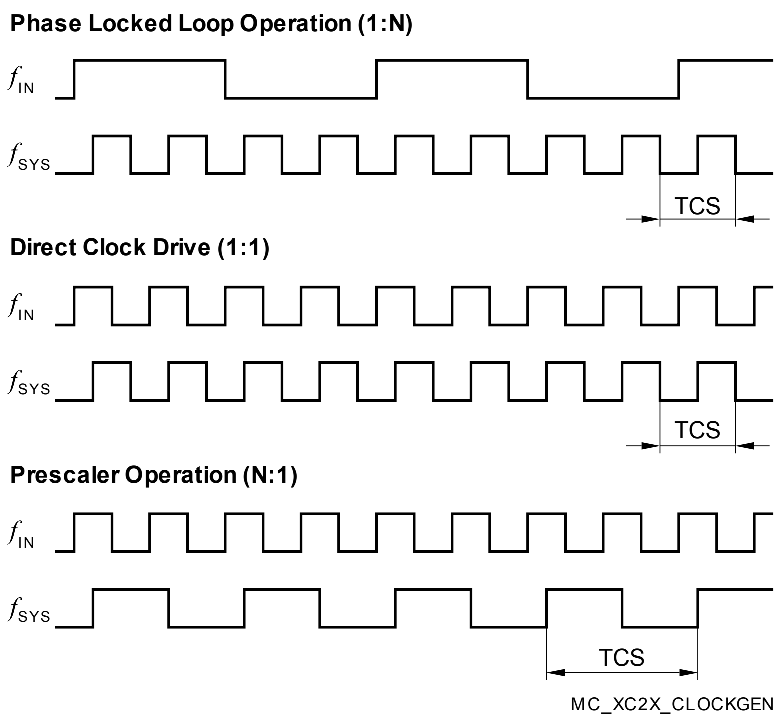


**Figure 19 Generation Mechanisms for the System Clock**

*Note: The example of PLL operation shown in **Figure 19** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

### 4.7.4 Pad Properties

The output pad drivers of the XE162xN can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage $V_{DDP}$. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 27** is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; $V_{DDP}$typ. 5 V; $V_{DDP} \geq$ 4.5 V

**Table 27 Standard Pad Parameters for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1] | $I_{Omax}$ CC | – | – | 4.0 | mA | Driver_Strength = Medium |
| | | – | – | 10 | mA | Driver_Strength = Strong |
| | | – | – | 0.5 | mA | Driver_Strength = Weak |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 1.0 | mA | Driver_Strength = Medium |
| | | – | – | 2.5 | mA | Driver_Strength = Strong |
| | | – | – | 0.1 | mA | Driver_Strength = Weak |

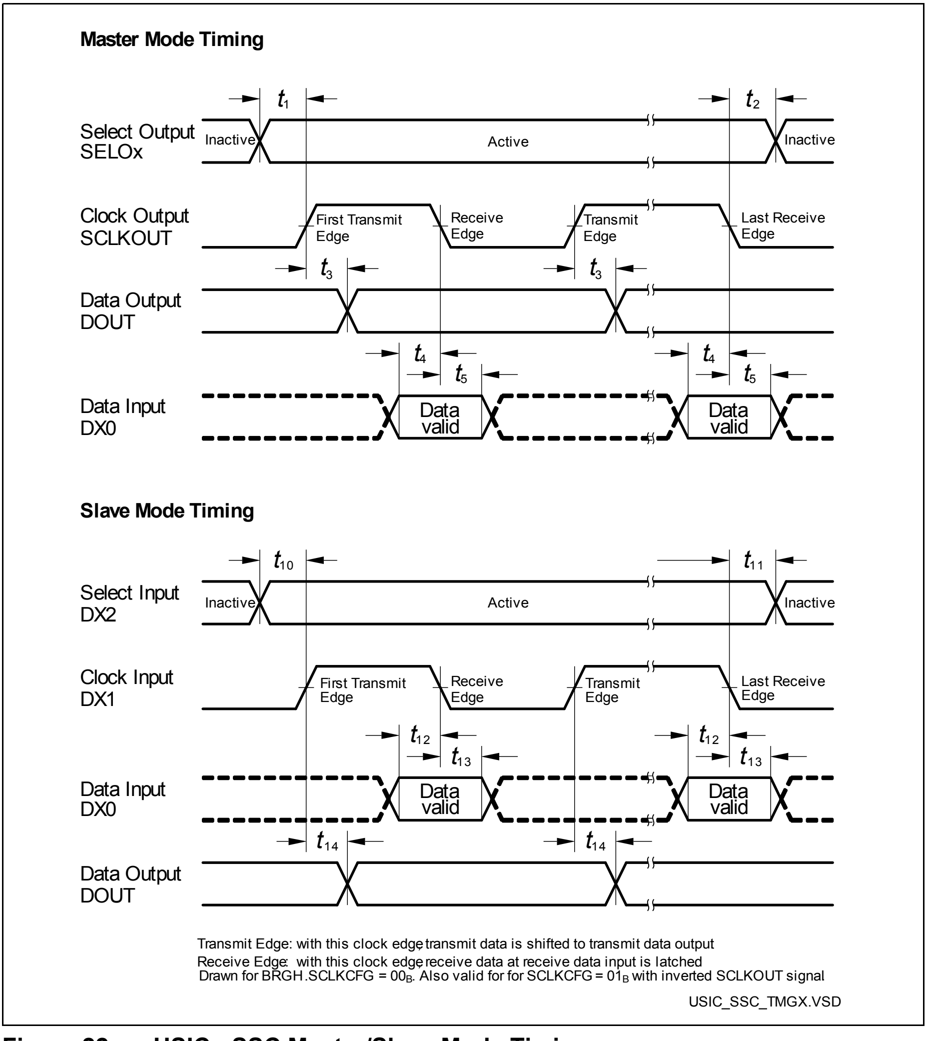


**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.*

## 5.3 Quality Declarations

The operation lifetime of the XE162xN depends on the operating temperature. The life time decreases with increasing temperature as shown in **Table 39**.

**Table 38 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | $t_{OP}$ CC | – | – | 20 | a | See **Table 39** |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | – | – | 2 000 | V | EIA/JESD22-A114-B |
| Moisture sensitivity level | MSL CC | – | – | 3 | – | JEDEC J-STD-020C |

**Table 39 Lifetime dependency from Temperature**

| Operating Time | Operating Temperature |
|---|---|
| 20 a | $T_J \leq 110°C$ |
| 95 500 h | $T_J = 120°C$ |
| 68 500 h | $T_J = 125°C$ |
| 49 500 h | $T_J = 130°C$ |
| 26 400 h | $T_J = 140°C$ |
| 14 500 h | $T_J = 150°C$ |

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