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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe162fn40f80laakxuma1

Email: info@E-XFL.COM

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General Device Information

2.1 Pin Configuration and Definition

The pins of the XE162xN are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.



Figure 3 XE162xN Pin Configuration (top view)



XE162FN, XE162HN XE166 Family / Value Line

General Device Information

Pin	Symbol	Ctrl.	Туре	Function
2, 16, 18, 32, 34, 48, 50, 64	V _{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB} .
1, 17, 33,	V _{SS}	-	PS/	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane.
49				Note: Also the exposed pad is connected internally to V_{SS} . To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

Table 5 Pin Definitions and Functions (cont'd)



3.2 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instructionfetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.



Figure 5 CPU Block Diagram



XE162FN, XE162HN XE166 Family / Value Line

Functional Description

With this hardware most XE162xN instructions are executed in a single machine cycle of 12.5 ns @ 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XE162xN instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.



3.3 Memory Protection Unit (MPU)

The XE162xN's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XE162xN's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.



3.5 Interrupt System

The architecture of the XE162xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE162xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11¹⁾ CPU clocks, the XE162xN can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE162xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

¹⁾ Depending if the jump cache is used or not.



With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE162xN to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.



MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- · Set of independent message objects (shared by the CAN nodes)
- · Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- · Flexible and powerful message transfer control and error handling capabilities
- · Full-CAN functionality for message objects:
 - Can be assigned to one of the CAN nodes
 - Configurable as transmit or receive objects, or as message buffer FIFO
 - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
 - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.14 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.15 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 μ s and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).



3.17 Parallel Ports

The XE162xN provides up to 40 I/O lines which are organized into 4 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in Table 9.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Port	Width	I/O	Connected Modules
P2	11	I/O	CAN, CC2, GPT12E, USIC, DAP/JTAG
P5	7	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	2	I/O	ADC, CAN, GPT12E
P7	1	I/O	CAN, GPT12E, SCU, DAP/JTAG, USIC
P10	16	I/O	CCU6, USIC, DAP/JTAG, CAN
P15	2	I	Analog Inputs, GPT12E

Table 9Summary of the XE162xN's Ports



3.18 Instruction Set Summary

Table 10 lists the instructions of the XE162xN.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "**Instruction Set Manual**".

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with Carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with Carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- \times 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2/4
OR(B)	Bitwise OR, (word/byte operands)	2/4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2/4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 10 Instruction Set Summary



Table 10	nstruction Set Summary (cont'd)	
Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2/4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2/4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction ¹⁾	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENW	DT Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2/4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2/4



4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance. *Note: Operating Conditions apply.*

Table 19ADC Parameters

Parameter	Symbol		Values		Unit	Note /
		Min.	Тур.	Max.		Test Condition
Switched capacitance at an analog input	C _{AINSW} CC	-	-	4	pF	not subject to production test
Total capacitance at an analog input	C _{AINT} CC	_	-	10	pF	not subject to production test
Switched capacitance at the reference input	C _{AREFSW} CC	_	-	7	pF	not subject to production test
Total capacitance at the reference input	C _{AREFT} CC	-	-	15	pF	not subject to production test
Differential Non-Linearity Error	EA _{DNL} CC	-	0.8	1	LSB	
Gain Error	$ EA_{GAIN} $ CC	-	0.4	0.8	LSB	
Integral Non-Linearity	EA _{INL} CC	-	0.8	1.2	LSB	
Offset Error	EA _{OFF} CC	-	0.5	0.8	LSB	
Analog clock frequency	$f_{\rm ADCI}{\rm SR}$	0.5	-	16.5	MHz	voltage_range= lower
		0.5	-	20	MHz	voltage_range= upper
Input resistance of the selected analog channel	R _{AIN} CC	-	_	2	kOh m	not subject to production test
Input resistance of the reference input	R _{AREF} CC	_	_	2	kOh m	not subject to production test



4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE162xN into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Short-term deviation of internal clock source frequency ¹⁾	∆f _{INT} CC	-1	-	1	%	$\Delta T_{J} \leq 10^{\circ}C$
Internal clock source frequency	$f_{\sf INT}{\sf CC}$	4.8	5.0	5.2	MHz	
Wakeup clock source	$f_{\rm WU}{ m CC}$	400	-	700	kHz	FREQSEL= 00
frequency ²⁾		210	-	390	kHz	FREQSEL= 01
		140	-	260	kHz	FREQSEL= 10
		110	-	200	kHz	FREQSEL= 11
Startup time from power- on with code execution from Flash	t _{SPO} CC	1.5	2.0	2.4	ms	∫ _{WU} = 500 kHz
Startup time from stopover mode with code execution from PSRAM	t _{SSO} CC	11 / f _{WU} ³⁾	-	12 / f _{WU} ³⁾	μs	
Core voltage (PVC) supervision level	V _{PVC} CC	V _{LV} - 0.03	V _{LV}	V _{LV} + 0.07 ⁴⁾	V	5)
Supply watchdog (SWD) supervision level	V _{SWD} CC	V _{LV} - 0.10 ⁶⁾	V _{LV}	V _{LV} + 0.15	V	voltage_range= lower ⁵⁾
		V _{LV} - 0.15	V _{LV}	V _{LV} + 0.15	V	voltage_range= upper ⁵⁾
		V _{LV} - 0.30	$V_{\rm LV}$	V _{LV} + 0.30	V	$V_{\rm LV}$ = 5.5 V ⁵⁾

Table 21Various System Parameters

 The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.



Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Code	Voltage Level	Notes ¹⁾
0000 _B	-	out of valid operation range
0001 _B	3.0 V	LEV1V: reset request
0010 _B - 0101 _B	3.1 V- 3.4 V	step width is 0.1 V
0110 _B	3.6 V	
0111 _B	4.0 V	
1000 _B	4.2 V	
1001 _B	4.5 V	LEV2V: no request
1010 _B - 1110 _B	4.6 V - 5.0 V	step width is 0.1 V
1111 _B	5.5 V	

Table 22 Coding of bit fields LEVxV in Register SWDCON0

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ± 10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in Table 23.

Table 23 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Voltage Level	Notes ¹⁾
000 _B -011 _B	-	out of valid operation range
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B - 111 _B	-	out of valid operation range

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.



Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

 $f_{\text{SYS}} = f_{\text{IN}}$.

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B , PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

 $f_{\text{SYS}} = f_{\text{OSC}} / \text{K1}.$

If a divider factor of 1 is selected, the frequency of $f_{\rm SYS}$ equals the frequency of $f_{\rm OSC}$. In this case the high and low times of $f_{\rm SYS}$ are determined by the duty cycle of the input clock $f_{\rm OSC}$ (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

 $f_{\rm SYS} = f_{\rm OSC} / 1024.$

4.7.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B , PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times F$).

F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):

 $(F = N / (P \times K2)).$

The input clock can be derived either from an external source at XTAL1 or from the onchip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

¹⁾ Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .



Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
VCO output frequency	f _{vco} CC	50	-	110	MHz	VCOSEL= 00b; VCOmode= controlled
		10	-	40	MHz	VCOSEL= 00b; VCOmode= free running
		100	-	160	MHz	VCOSEL= 01b; VCOmode= controlled
		20	-	80	MHz	VCOSEL= 01b; VCOmode= free running

Table 25 System PLL Parameters

4.7.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



Parameter	Symbol	Values			Unit	Note /								
		Min.	Тур.	Max.		Test Condition								
Rise and Fall times (10% - 90%)	t _{RF} CC	-	-	23 + 0.6 x C _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Medium								
		-	-	11.6 + 0.22 x <i>C</i> _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Strong; Driver_Edge= Medium								
		-	-	4.2 + 0.14 x <i>C</i> _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Strong; Driver_Edge= Sharp								
										-	-	20.6 + 0.22 x C _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Strong; Driver_Edge= Slow

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma - I_{OH}$) must remain below 50 mA.





Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.



Package and Reliability

Package Outlines



Figure 28 PG-LQFP-64-6 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": http://www.infineon.com/packages



Package and Reliability

5.2 Thermal Considerations

When operating the XE162xN in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}}-V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- · Reduce the system frequency
- · Reduce the number of output pins
- Reduce the load on active output drivers